

MT7620 PROGRAMMING GUIDE

Integrated 802.11n MAC/BBP and 2.4 GHz RF/FEM Router-on-a-Chip



MT7620 Overview

The MT7620 SoC includes a high performance 580 MHz MIPS24KEc CPU core and USB host controller/PHY, which is designed to enable a multitude of high performance, cost-effective IEEE 802.11n applications with a MediaTek (Ralink) client card.

Functional Block Diagram

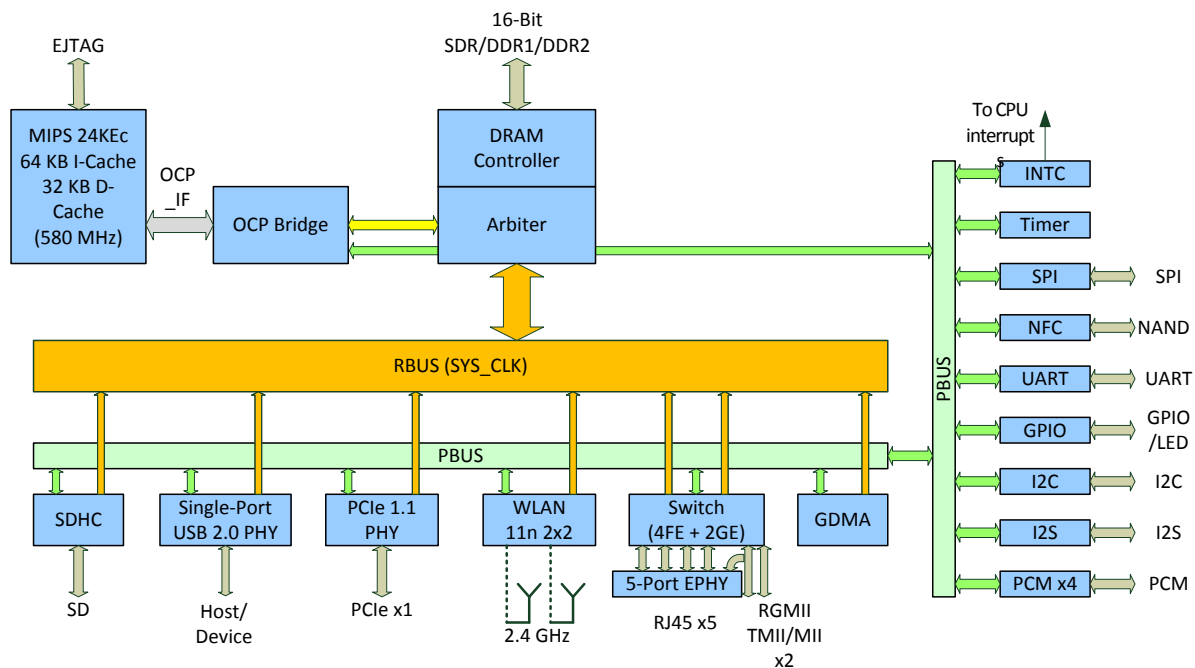


Figure 1-1 MT7620 Block Diagram

There are several masters (MIPS 24KEc, USB, PCI Express) in the MT7620 SoC on a high performance, low latency Rbus, (Ralink Bus). In addition, the MT7620 SoC supports lower speed peripherals such as UART, GPIO, and SPI via a low speed peripheral bus (Pbus). The SDRAM/DDR1/DDR2 controller is the only bus slave on the Rbus. It includes an Advanced Memory Scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

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1. MIPS 24K Processor

1.1 Features

- 8-stage pipeline
- 32-bit address paths
- 64-bit data paths to caches and external interfaces
- MIPS32-Compatible Instruction Set
 - Multiply-Accumulate and Multiply-Subtract Instructions (MADD, MADDU, MSUB, MSUBU)
 - Targeted Multiply Instruction (MUL)
 - Zero/One Detect Instructions (CLZ, CLO)
 - Wait instructions (WAIT)
 - Conditional Move instructions (MOVZ, MOVN)
 - Prefetch instructions (PREF)
- MIPS32 Enhanced Architecture (Release 2) Features
 - Vectored interrupts and support for an external interrupt controller
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - GPR shadow registers (one, three or seven additional shadows can be optionally added to minimize latency for interrupt handlers)
 - Bit field manipulation instructions
- MIPS32 Privileged Resource Architecture
 - MIPS DSP ASE
 - Fractional data types (Q15, Q31)
 - Saturating arithmetic
 - SIMD instructions operate on 2x16 b or 4x8 b simultaneously
 - 3 additional pairs of accumulator registers
- Programmable Memory Management Unit
 - 32 dual-entry JTLB with variable page sizes
 - 4-entry ITLB
 - 8-entry DTLB
 - Optional simple Fixed Mapping Translation (FMT) mechanism
- MIPS16e™ Code Compression
 - 16-bit encodings of 32-bit instructions to improve code density
 - Special PC-relative instructions for efficient loading of addresses and constants
 - SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
 - Improved support for handling 8 and 16-bit datatypes
- Programmable L1 Cache Sizes
 - Instruction cache size: 32 KB
 - Data cache size: 16 KB
- 4-Way Set Associative
 - Up to 8 outstanding load misses
 - Write-back and write-through support
 - 32-byte cache line size

1.2 Block Diagram

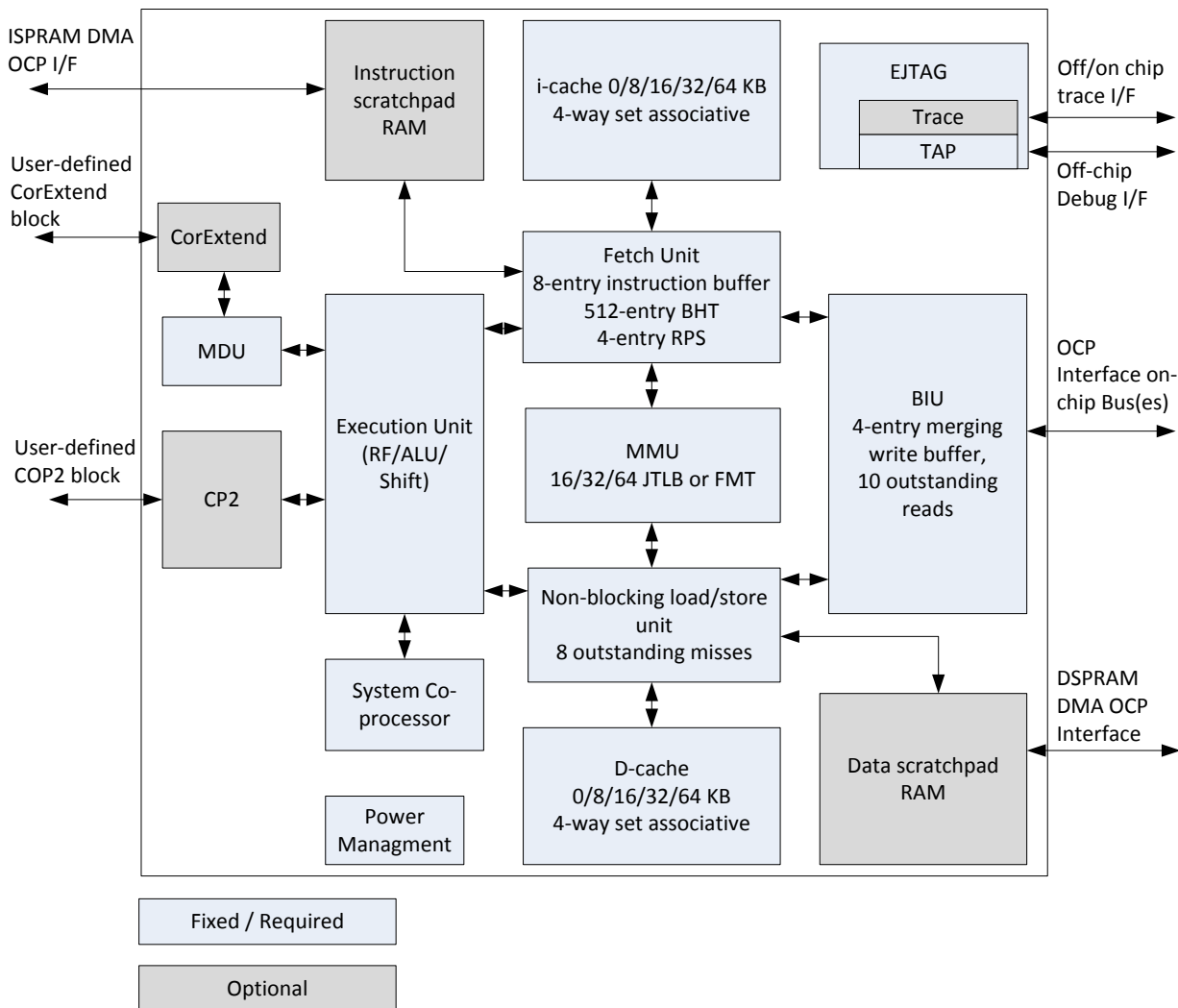


Figure 1-1 MIPS 24KEc Processor

1.3 Memory Map Summary

Start		End	Size	Description
0000.0000	-	0FFF.FFFF	256 MBytes	DDR2 256 MB/ DDR1 256 MB/SDRAM 128 MB
1000.0000	-	1000.00FF	256 Bytes	SYSCTL
1000.0100	-	1000.01FF	256 Bytes	TIMER
1000.0200	-	1000.02FF	256 Bytes	INTCTL
1000.0300	-	1000.03FF	256 Bytes	MEM_CTRL (SDR/DDR)
1000.0400	-	1000.04FF	256 Bytes	Rbus Matrix CTRL
1000.0500	-	1000.05FF	256 Bytes	UART
1000.0600	-	1000.06FF	256 Bytes	PIO
1000.0700	-	1000.07FF	256 Bytes	<<Reserved>>
1000.0800	-	1000.08FF	256 Bytes	NAND Controller
1000.0900	-	1000.09FF	256 Bytes	I2C
1000.0A00	-	1000.0AFF	256 Bytes	I2S
1000.0B00	-	1000.0BFF	256 Bytes	SPI
1000.0C00	-	1000.0CFF	256 Bytes	UARTLITE
1000.0D00	-	1000.0DFF	256 Bytes	MIPS CNT
1000.2000	-	1000.27FF	2 KBytes	PCM (up to 16 channels)
1000.2800	-	1000.2FFF	2 KBytes	Generic DMA (up to 64 channels)
1000.3000	-	1000.37FF	2 KBytes	<<Reserved>>
1000.3800	-	1000.3FFF	2 KBytes	<<Reserved>>
1000.4000	-	100F.FFFF		<<Reserved>>
1010.0000	-	1010.FFFF	64 KBytes	Frame Engine
1011.0000	-	1011.7FFF	32 KBytes	Ethernet Swtich
1011.8000		1011.FFFF	32 KBytes	ROM
1012.0000	-	1012.7FFF	32 KBytes	USB Device Control
1012.8000	-	1012.FFFF	32 KBytes	<<Reserved>>
1013.0000	-	1013.3FFF	16 KBytes	SDHC
1013.4000	-	1013.FFFF	48 KBytes	<<Reserved>>
1014.0000	-	1017.FFFF	256 KBytes	PCI Express
1018.0000	-	101B.FFFF	256 KBytes	WLAN BBP/MAC
101C.0000	-	101F.FFFF	256 KBytes	USB Host
1020.0000	-	1023.FFFF	256 KBytes	<<Reserved>>
1024.0000	-	1027.FFFF	256 KBytes	<<Reserved>>
1028.0000	-	1BFF.FFFF		<<Reserved>>
1C00.0000	-	1C00.7FFF	32 KB ROM	When the system is powered on, a 24 KB internal boot ROM is mapped.

1.4 Clock Plan

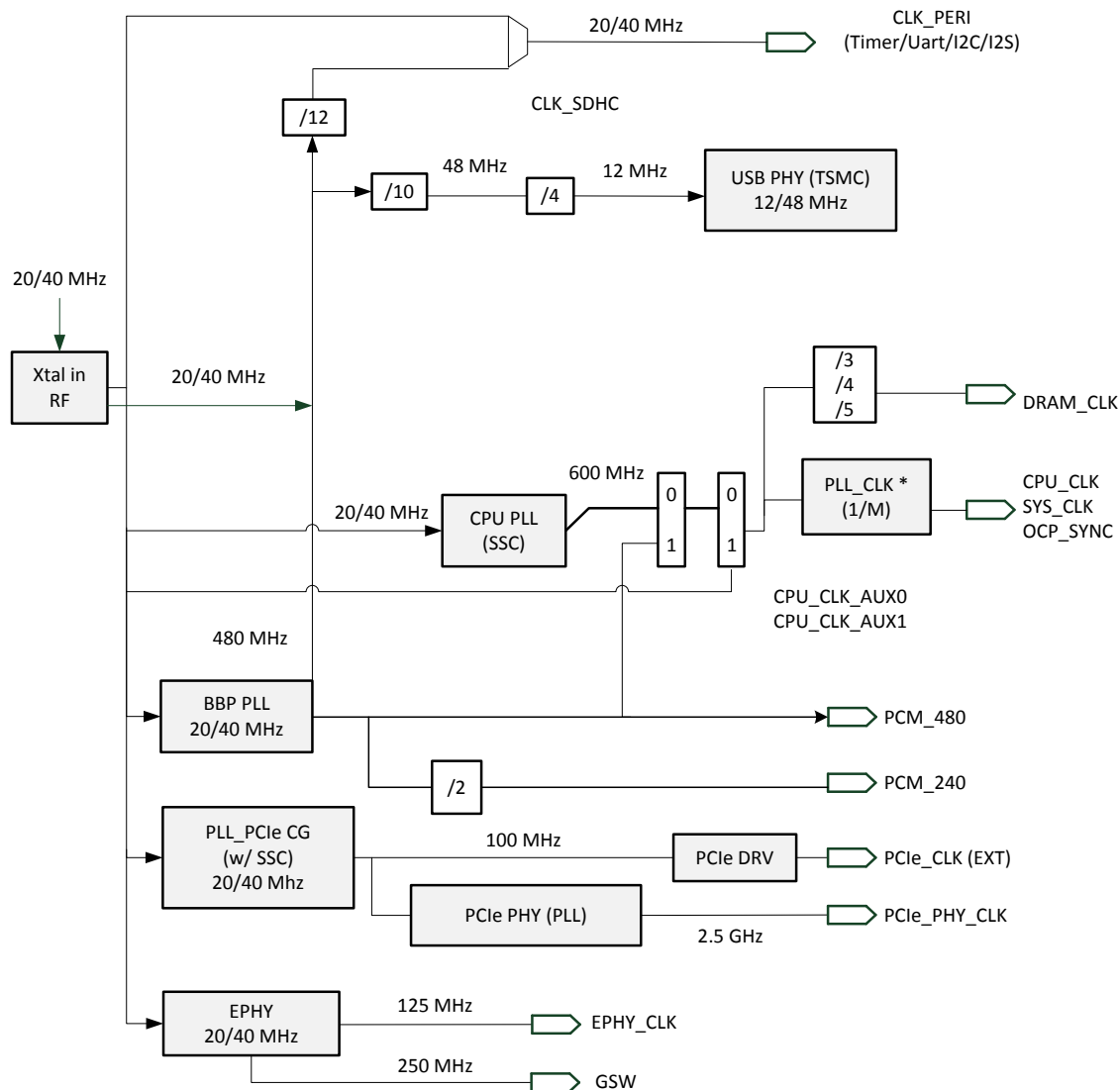


Figure 1-2 MT7620 Clock Diagram

1.5 CPU Clock Mux

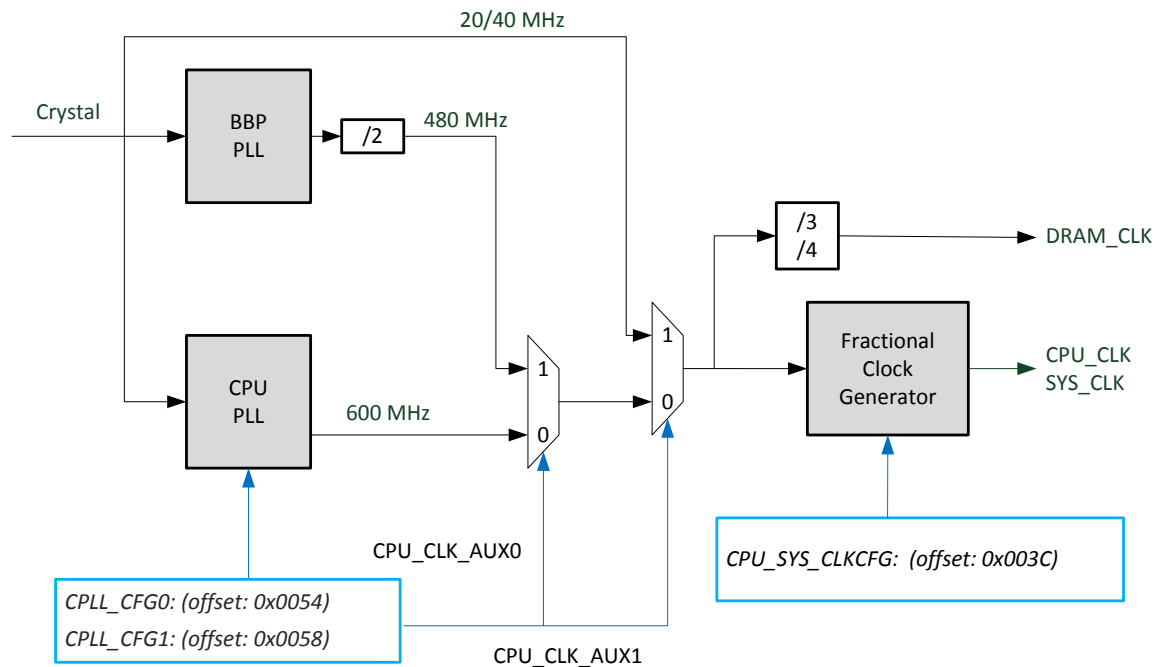


Figure 1-3 CPU Clock Mux

2. Registers

2.1 Nomenclature

The following nomenclature is used for register types:

RO	Read Only
WO	Write Only
RW	Read or Write
RC	Read Clear
W1C	Write One Clear
-	Reserved bit
X	Undefined binary value

2.2 System Control

2.2.1 Features

- Provides read-only chip revision registers
- Provides a window to access boot-strapping signals
- Supports memory remapping configurations
- Supports software reset to each platform building block
- Provides registers to determine GPIO and other peripheral pin muxing schemes
- Provides some power-on-reset only test registers for software programmers
- Combines miscellaneous registers (such as clock skew control, status register, memo registers, etc)

2.2.2 Block Diagram

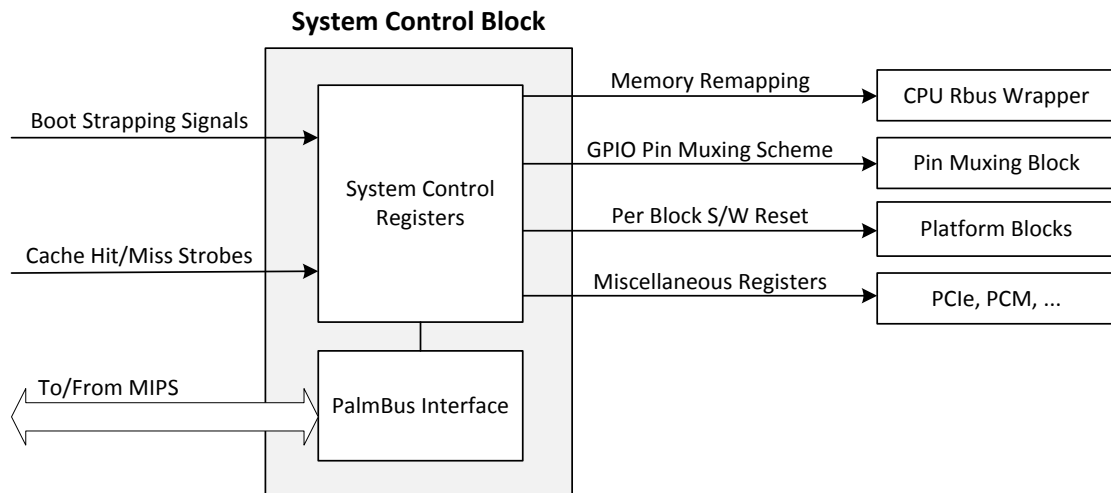


Figure 2-1 System Control Block Diagram

2.2.3 List of Registers

No.	Offset	Register Name	Description	Page
1	0x0000	CHIPID0_3	Chip ID ASCII Character 0-3	19
2	0x0004	CHIPID4_7	Chip ID ASCII Character 4-7	19
3	0x000C	REVID	Chip Revision Identification	19
4	0x0010	SYSCFG0	System Configuration Register 0	19
5	0x0014	SYSCFG1	System Configuration Register 1	20
6	0x0018	TESTSTAT	Firmware Test Status Register	22
7	0x001C	TESTSTAT2	Firmware Test Status Register 2	22
8	0x0020	Reserved	-	22
9	0x0024	Reserved	-	23
10	0x0028	Reserved	-	23
11	0x002C	CLKCFG0	Clock Configuration Register 0	23
12	0x0030	CLKCFG1	Clock Configuration Register 1	24
13	0x0034	RSTCTRL	Reset Control	25
14	0x0038	RSTSTAT	Reset Status	26
15	0x003C	CPU_SYS_CLKCFG	CPU and SYS Clock Control	27
16	0x0040	CLK_LUT_CFG	Clock Look Up Table Configuration	29
17	0x0044	CUR_CLK_STS	Current clock status	30
18	0x0048	BPLL_CFG0	BB PLL Configuration 0	31
19	0x004C	BPLL_CFG1	BB PLL Configuration 1	31
20	0x0054	CPLL_CFG0	CPU PLL Configuration 0	33
21	0x0058	CPLL_CFG1	CPU PLL Configuration 1	36
22	0x005C	USB_PHY_CFG	USB PHY control	36
23	0x0060	GPIOMODE	GPIO Purpose Select	36
24	0x0064	PCIPDMA_STAT	Control and Status of PDMA in PCIe Device	39
25	0x0088	PMU0_CFG	Power Management Unit 0 Configuration	39
26	0x008C	PMU1_CFG	Power Management Unit 1 Configuration	40
27	0x0098	PPLL_CFG0	PCIe PLL Configuration 0	41
28	0x009C	PPLL_CFG1	PCIe PLL Configuration 1	43
29	0x00A0	PPLL_DRV	PCIe Driver Configuration	44

2.2.4 Register Descriptions (base: 0x1000_0000)

1. CHIPID0_3: Chip ID ASCII Character 0-3 (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:24	RO	CHIP_ID3	ASCII CHIP Name Identification Character 3	0x36
23:16	RO	CHIP_ID2	ASCII CHIP Name Identification Character 2	0x37
15:8	RO	CHIP_ID1	ASCII CHIP Name Identification Character 1	0x54
7:0	RO	CHIP_ID0	ASCII CHIP Name Identification Character 0	0x4D

2. CHIPID4_7: Chip Name ASCII Character 4-7 (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:24	RO	CHIP_ID7	ASCII CHIP Name Identification Character 7	0x20
23:16	RO	CHIP_ID6	ASCII CHIP Name Identification Character 6	0x20
15:8	RO	CHIP_ID5	ASCII CHIP Name Identification Character 5	0x30
7:0	RO	CHIP_ID4	ASCII CHIP Name Identification Character 4	0x32

3. REVID: Chip Revision Identification (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
16	RO	PKG_ID	Package ID 0: DRQFN-148 pin 1: TFBGA-269 ball NOTE: This value is determined by the package used.	-
15:12	-	-	Reserved	0x0
11:8	RO	VER_ID	Chip Version Number	0x2
7:4	-	-	Reserved	0x0
3:0	RO	ECO_ID	Chip ECO Number	0x1

4. SYSCFG0: System Configuration Register 0 (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:24	RW	TEST_CODE	Test Code Default value is from bootstrap and can be modified by software.	0x0
23	-	-	Reserved	0x0
22:12	RO	BS_SHADOW	BS shadow register for last boot-up value Displays a backup copy of the last bootup value.	BS
11:9	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
8	RO	DRAM_FROM_EE	DRAM Configuration from EEPROM 0: DRAM/PLL configuration from EEPROM. 1: DRAM configuration from Auto Detect. For more information see the Bootstrapping Pins Description in the datasheet for this chip.	BS
7	RO	DBG_JTAG_MODE	Debug JTAG Mode 0: EPHY_LED 1: JTAG MODE	BS
6	RO	XTAL_FREQ_SEL	Xtal Frequency Select 0: 20 MHz 1: 40 MHz	BS
5:4	RO	DRAM_TYPE	DRAM Type 0: SDRAM (150 MHz) (LVTTTL 3.3 V) TSOP Package 1: DDR1 (200 MHz) TSOP Package 2: DDR2 (200 MHz) FBGA Package	BS
3:0	RO	CHIP_MODE	Chip Mode A vector to set chip function/test/debug modes in non-test/debug operation. For more information see the Bootstrapping Pins Description in the datasheet for this chip.	BS

5. SYSCFG1: System Configuration Register 0 (offset: 0x0014)

Bits	Type	Name	Description	Initial Value																									
31:30	-	-	Reserved	-																									
29:28	RW	DDR_DPIN_RXPWD	SDRAM Data Pin Receiver Circuit Power Down Control* (DQ/DQS) 0: Disable (SDR/DDR1/DDR2 default) 1: Enable 2: Enable while data pin is output mode. 3: Enable while data pin is input mode.	BS																									
27:26	RW	DDR_DPIN_ODT	SDRAM Data Pin On Die Termination Setting* (DQ/DQS) <table border="1"> <tr> <td>[27:26]</td><td>SDR (3.3 V)</td><td>SDR (2.5 V/ 1.8 V)</td><td>DDR1</td><td>DDR2</td></tr> <tr> <td>0</td><td>(Disable)</td><td>(Disable)</td><td>(Disable)</td><td>(Disable)</td></tr> <tr> <td>1</td><td>75 Ω</td><td>75 Ω</td><td>75 Ω</td><td>75 Ω</td></tr> <tr> <td>2</td><td>150 Ω</td><td>150 Ω</td><td>150 Ω</td><td>150 Ω</td></tr> <tr> <td>3</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr> </table>	[27:26]	SDR (3.3 V)	SDR (2.5 V/ 1.8 V)	DDR1	DDR2	0	(Disable)	(Disable)	(Disable)	(Disable)	1	75 Ω	75 Ω	75 Ω	75 Ω	2	150 Ω	150 Ω	150 Ω	150 Ω	3	N/A	N/A	N/A	N/A	BS
[27:26]	SDR (3.3 V)	SDR (2.5 V/ 1.8 V)	DDR1	DDR2																									
0	(Disable)	(Disable)	(Disable)	(Disable)																									
1	75 Ω	75 Ω	75 Ω	75 Ω																									
2	150 Ω	150 Ω	150 Ω	150 Ω																									
3	N/A	N/A	N/A	N/A																									

Bits	Type	Name	Description	Initial Value																									
25:24	RW	DDR_DPIN_DRV	SDRAM Data Pin Driving Setting* (DQ/DQS/DQM)	BS																									
<table border="1"> <tr> <td>[25:24]</td><td>SDR (3.3 V)</td><td>SDR (2.5 V/ 1.8 V)</td><td>DDR1</td><td>DDR2</td></tr> <tr> <td>0</td><td>N/A</td><td>10 mA</td><td>Class II</td><td>Full</td></tr> <tr> <td>1</td><td>N/A</td><td>8 mA</td><td>N/A</td><td>N/A</td></tr> <tr> <td>2</td><td>16 mA</td><td>4 mA</td><td>(Class I)</td><td>(Half)</td></tr> <tr> <td>3</td><td>(8 mA)</td><td>(2 mA)</td><td>N/A</td><td>N/A</td></tr> </table>					[25:24]	SDR (3.3 V)	SDR (2.5 V/ 1.8 V)	DDR1	DDR2	0	N/A	10 mA	Class II	Full	1	N/A	8 mA	N/A	N/A	2	16 mA	4 mA	(Class I)	(Half)	3	(8 mA)	(2 mA)	N/A	N/A
[25:24]	SDR (3.3 V)	SDR (2.5 V/ 1.8 V)	DDR1	DDR2																									
0	N/A	10 mA	Class II	Full																									
1	N/A	8 mA	N/A	N/A																									
2	16 mA	4 mA	(Class I)	(Half)																									
3	(8 mA)	(2 mA)	N/A	N/A																									
23	-	-	Reserved	-																									
22	RW	DDR_CPIN_RXPWD	SDRAM Command Pin Receiver Circuit Power Down Control* (MA/MBA/MCS_N/MWE_N/MRAS_N/ MCAS_N/ MCKE) 0: Disable power down 1: Enable power down (SDR/DDR1/DDR2 default)	BS																									
21:20	RW	DDR_CPIN_DRV	SDRAM Command Pin Driving Setting (MA/MBA/MCS_N/MWE_N/MRAS_N/ MCAS_N/ MCKE)	BS																									
<table border="1"> <tr> <td>[21:20]</td><td>SDR (3.3 V)</td><td>SDR (2.5 V/ 1.8 V)</td><td>DDR1</td><td>DDR2</td></tr> <tr> <td>0</td><td>N/A</td><td>10 mA</td><td>Class II</td><td>Full</td></tr> <tr> <td>1</td><td>N/A</td><td>8 mA</td><td>N/A</td><td>N/A</td></tr> <tr> <td>2</td><td>16 mA</td><td>4 mA</td><td>(Class I)</td><td>(Half)</td></tr> <tr> <td>3</td><td>(8 mA)</td><td>(2 mA)</td><td>N/A</td><td>N/A</td></tr> </table>					[21:20]	SDR (3.3 V)	SDR (2.5 V/ 1.8 V)	DDR1	DDR2	0	N/A	10 mA	Class II	Full	1	N/A	8 mA	N/A	N/A	2	16 mA	4 mA	(Class I)	(Half)	3	(8 mA)	(2 mA)	N/A	N/A
[21:20]	SDR (3.3 V)	SDR (2.5 V/ 1.8 V)	DDR1	DDR2																									
0	N/A	10 mA	Class II	Full																									
1	N/A	8 mA	N/A	N/A																									
2	16 mA	4 mA	(Class I)	(Half)																									
3	(8 mA)	(2 mA)	N/A	N/A																									
19	RW	DDR_PIN_MODE	SDRAM Pin Receiver Mode Selection* 0: Select pseudo-differential receiver for 2.5 V SSTL2 and 1.8 V SSTL18. (DDR1/DDR2 default) 1: Select CMOS receiver for 3.3 V LVTTTL, 2.5 V LVCMOS and 1.8 V MDDR. (SDR default)	BS																									
18:17	-	-	Reserved	0x0																									
16	RW	PULL_EN	Pad Pull High/Low Enable 0: Disable 1: Enable	0x0																									
15:14	RW	GE2_MODE	Gigabit Port #2 Mode Sets the interface mode on Gigabit port 2. 2'b00: RGMII Mode (10/100/1000 Mbps) 2'b01: MII Mode (10/100 Mbps) 2'b10: Reverse MII Mode (10/100 Mbps) 2'b11: RJ-45 Mode	0x3																									

Bits	Type	Name	Description	Initial Value															
13:12	RW	GE1_MODE	Gigabit Port #1 Mode Sets the interface mode on Gigabit port 1. 2'b00: RGMII Mode (10/100/1000 Mbps) 2'b01: MII Mode (10/100 Mbps) 2'b10: Reverse MII Mode (10/100 Mbps) 2'b11: Reserved	0x0															
11	-	-	Reserved	0x0															
10	RW	USB0_HOST_MODE	0: Set USB #0 to device mode 1: Set USB #0 to host mode.	BS															
9	-	-	Reserved	0x0															
8	RW	PCIE_RC_MODE	0: Set PCIe to EP mode 1: Set PCIe to RC mode	BS															
7:4	-	-	Reserved	0x0															
3:2	RW	GE2_PIN_DRV	RGMII2 Pin Driving Setting <table border="1"><tr><td>[1:0]</td><td>LVTTL (3.3 V)</td><td>LVC MOS (2.5 V)</td></tr><tr><td>0</td><td>N/A</td><td>10 mA</td></tr><tr><td>1</td><td>N/A</td><td>8 mA</td></tr><tr><td>2</td><td>16 mA</td><td>4 mA</td></tr><tr><td>3</td><td>(8 mA)</td><td>(2 mA)</td></tr></table>	[1:0]	LVTTL (3.3 V)	LVC MOS (2.5 V)	0	N/A	10 mA	1	N/A	8 mA	2	16 mA	4 mA	3	(8 mA)	(2 mA)	0x3
[1:0]	LVTTL (3.3 V)	LVC MOS (2.5 V)																	
0	N/A	10 mA																	
1	N/A	8 mA																	
2	16 mA	4 mA																	
3	(8 mA)	(2 mA)																	
1:0	RW	GE1_PIN_DRV	RGMII1 Pin Driving Setting <table border="1"><tr><td>[1:0]</td><td>LVTTL (3.3 V)</td><td>LVC MOS (2.5 V)</td></tr><tr><td>0</td><td>N/A</td><td>10 mA</td></tr><tr><td>1</td><td>N/A</td><td>8 mA</td></tr><tr><td>2</td><td>16 mA</td><td>4 mA</td></tr><tr><td>3</td><td>(8 mA)</td><td>(2 mA)</td></tr></table>	[1:0]	LVTTL (3.3 V)	LVC MOS (2.5 V)	0	N/A	10 mA	1	N/A	8 mA	2	16 mA	4 mA	3	(8 mA)	(2 mA)	0x3
[1:0]	LVTTL (3.3 V)	LVC MOS (2.5 V)																	
0	N/A	10 mA																	
1	N/A	8 mA																	
2	16 mA	4 mA																	
3	(8 mA)	(2 mA)																	

NOTE:

- For bits marked with an *, the default value is defined by bootstrap "DRAM_TYPE" and can be modified by software.
- Default values are marked with parentheses.

6. TESTSTAT: Firmware Test Status Register (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:0	RW	TSETSTAT	Firmware Test Status	0x0

NOTE: This register is reset only by a power-on reset.

7. TESTSTAT2: Firmware Test Status Register 2 (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:0	RW	TSETSTAT2	Firmware Test Status 2	0x0

NOTE: This register is reset only by a power-on reset.

8. Reserved (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
------	------	------	-------------	---------------

Bits	Type	Name	Description	Initial Value
31:0	RW	BOOTSRAM_BASE	Boot from SRAM base address (Test mode only) Addr_tuned = bootsram[31:0] oc_maddr[15:0]	0x10240000

9. Reserved (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:0	-	-	Reserved	0x0

10. Reserved (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:0	-	-	Reserved	0x0

11. CLKCFG0: Clock Configuration Register 0 (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:30	RW	SDRAM_CLK_SKEW	SDRAM Clock Skew 0: Zero delay 1: Delay 200 ps 2: Delay 400 ps 3: Delay 600 ps	0x1
29:24	RW	OSC_1US_DIV	Oscillator 1 μ s Divider Sets the maximum for the reference clock counter for either a 20 MHz or 40 MHz external XTAL input. The count increments each 1 μ sec (indicating 1 MHz), up to the maximum, before resetting to zero. This counts the frequency of an external XTAL. This count is used to output a 32 KHz frequency to the REFCLK0 pin. 6'b0: Automatically generates a 1 μ s system tick regardless of whether XTAL frequency is 20 MHz or 40 MHz. 6'd39: Default value for an external 40 MHz XTAL. 6'd19: Default value for an external 20 MHz XTAL. Others: Manual mode for tick generation.	0x0
23	-	-	Reserved	0x0
22:18	RW	INT_CLK_FDIV	Internal Clock Frequency Divider The frequency divider used to generate the Fraction-N clock frequency. Valid values range from 1 to 31. Fraction-N clock frequency = (INT_CLK_FFRAC/INT_CLK_FDIV)*PLL_FREQ	0x8
17	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
16:12	RW	INT_CLK_FFRAC	Internal Clock Fraction-N Frequency A parameter used in conjunction with INT_CLK_FDIV to generate the Fraction-N clock frequency. Valid values range from 0 to 31. Fraction-N clock Frequency = $(\text{INT_CLK_FFRAC}/\text{INT_CLK_FDIV}) * \text{PLL_FREQ}$	0x0
11:9	RW	REFCLK0_RATE	Reference Clock 0 Rate 0: Xtal clock 20/40 MHz 1: 12 MHz 2: 25 MHz 3: 40 MHz 4: 48 MHz 5: Internal Fraction-N_CLK/2 6: Reserved 7: CPLL_DIV8	0x0
8	-	-	Reserved	0x0
7:5	-	-	Reserved	0x0
4	RW	PERI_CLK_SEL	Peripheral Clock Source Select Sets the peripheral clock to use the 20/40 MHz frequency input from XTAL. 0: 40 MHz from 480 MHz divided by 12. 1: 20 MHz/40M Hz from XTAL input	0x0
3	RW	EPHY_USE_25M	EPHY Clock Source Select Set the EPHY clock to use the 25 MHz frequency input from the PPLL. 0: EPHY use 20/40 MHz from XTAL 1: EPHY use 25 MHz from PPLL	0x0
2	-	-	Reserved	0x0
1:0	-	-	Reserved	0x0

12. CLKCFG1: Clock Configuration Register 1 (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30	RW	SDHC_CLK_EN	SDHC clock enable	0x1
29	-	-	Reserved	0x1
28	RW	AUX_STCK_CLK_EN	Aux system tick clock enable	0x1
27	-	-	Reserved	0x0
26	RW	PCIE0_CLK_EN	PCIE0 clock enable	0x1
25	RW	UPHY0_CLK_EN	UPHY0 clock enable	0x1
24	-	-	Reserved	0x1
23	RW	ESW_CLK_EN	Ethernet switch clock enable	0x1

Bits	Type	Name	Description	Initial Value
22	-	-	Reserved	0x1
21	RW	FE_CLK_EN	FE clock enable	0x1
20	-	-	Reserved	0x0
19	RW	UARTL_CLK_EN	UART Lite clock enable	0x1
18	RW	SPI_CLK_EN	SPI clock enable	0x1
17	RW	I2S_CLK_EN	I2S clock enable	0x1
16	RW	I2C_CLK_EN	I2C clock enable	0x1
15	RW	NAND_CLK_EN	Nand flash control clock enable	0x1
14	RW	GDMA_CLK_EN	GDMA clock enable	0x1
13	RW	PIO_CLK_EN	GPIO controller clock enable	0x1
12	RW	UART_CLK_EN	UART clock enable	0x1
11	RW	PCM_CLK_EN	PCM clock enable	0x1
10	RW	MC_CLK_EN	Memory controller clock enable	0x1
9	RW	INTC_CLK_EN	Interrupt controller clock enable	0x1
8	RW	TIMER_CLK_EN	Timer clock enable	0x1
7	RW	GE2_CLK_EN	GE2 controller clock enable.	0x1
6	RW	GE1_CLK_EN	GE1 controller clock enable.	0x1
5:0	-	-	Reserved	0x0

NOTE:

0: Clock is gated.

1: Clock is enabled.

13. RSTCTRL: Reset Control Register (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31	RW	PPE_RST	Resets PPE	0x0
30	RW	SDHC_RST	Resets SD Controller.	0x0
29	-	-	Reserved	0x0
28	RW	MIPS_CNT_RST	Resets MIPS counter block.	0x0
27	-	-	Reserved	0x0
26	RW	PCIE0_RST	Resets PCIE Host Bridge, PCIE0 Controller and PHY.	0x0
25	RW	UHST0_RST	Resets USB PHY0. NOTE: USB Host controller will be reset when both UHST0_RST and UHST1_RST are set.	0x0
24	RW	EPHY_RST	Resets the Ethernet PHY block.	0x0
23	RW	ESW_RST	Resets the Ethernet switch block.	0x0
22	-	-	Reserved	0x0
21	RW	FE_RST	Resets the Frame Engine block.	0x0
20	RW	WLAN_RST-	Resets the WLAN block.	0x0
19	RW	UARTL_RST	Resets the UART Lite block.	0x0

Bits	Type	Name	Description	Initial Value
18	RW	SPI	Resets the SPI block.	0x0
17	RW	I2S	Resets the I ² S block.	0x0
16	RW	I2C	Resets the I ² C block.	0x0
15	RW	NAND	Resets the NAND block.	0x0
14	RW	DMA	Resets the DMA block.	0x0
13	RW	PIO	Resets the PIO block.	0x0
12	RW	UART_RST	Resets the UART block.	0x0
11	RW	PCM_RST	Resets the PCM block.	0x0
10	RW	MC_RST	Resets the Memory Controller block.	0x1
9	RW	INTC_RST	Resets the Interrupt Controller block.	0x0
8	RW	TIMER_RST	Resets the Timer block.	0x0
7:1	-	-	Reserved	0x0
0	W1C	SYS_RST	Resets the whole SoC.	0x0

NOTE:

0: Deassert reset

1: Reset

14. RSTSTAT: Reset Status Register (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31	RW	WDT2SYSRST_EN	Watchdog Timeout To System Reset Enable Enables watchdog timeout to trigger a system reset. 0: Disable 1: Enable	0x1
30	RW	WDT2RSTO_EN	Watchdog Timeout to Reset Output Enable Enables watchdog timeout to trigger the reset output pin. 0: Disable 1: Enable	0x1
29:16	RW	WDTRSTPD	Watchdog Reset Output Low Period Controls the WDT reset output low period. For example: If the pin share mode was set correctly and WDT2RSTO_EN=1, ▪ When WDTRSTPD= 0, you can see duration of 1 μs low on the WDT reset output pin. ▪ When WDTRSTPD= 3, you can see duration of 4 μs low on the WDT reset output pin. (unit: 1 μ s)	0x3
15:4	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
3	R/W1C	SWCPURST	Software CPU Reset Indicates when software has reset the CPU by writing to the RSTCPU bit in RSTCTL. 0: Has no effect. 1: Clears this bit. NOTE: This register is reset only by a power-on reset.	0x0
2	R/W1C	SWSYSRST	Software System Reset Indicates when software has reset the chip by writing to the RSTSYS bit in RSTCTL. 0: Has no effect. 1: Clears this bit. NOTE: This register is reset only by a power on reset.	0x0
1	R/W1C	WDRST	Watchdog Reset Indicates when the watchdog timer has reset the chip. 0: Has no effect. 1: Clears this bit. NOTE: This register is reset only by power-on reset.	0x0
0	-	-	Reserved	0x0

15. CPU_SYS_CLKCFG: CPU and SYS Clock Control (offset: 0x003C)

Bits	Type	Name	Description	Initial Value																						
31:20	-	-	Reserved	0x0																						
19:16	RW	CPU_OCP_RATIO	CPU OCP Ratio The ratio between the system bus frequency and the CPU frequency. <table border="1"><thead><tr><th>Value</th><th>Ratio (SYS : CPU)</th></tr></thead><tbody><tr><td>4'd0</td><td>1 : 1 (Reserved)</td></tr><tr><td>4'd1</td><td>1 : 1.5 (Reserved)</td></tr><tr><td>4'd2</td><td>1 : 2</td></tr><tr><td>4'd3</td><td>1 : 2.5 (Reserved)</td></tr><tr><td>4'd4</td><td>1 : 3</td></tr><tr><td>4'd5</td><td>1 : 3.5 (Reserved)</td></tr><tr><td>4'd6</td><td>1 : 4</td></tr><tr><td>4'd7</td><td>1 : 5</td></tr><tr><td>4'd8</td><td>1 : 10</td></tr><tr><td>Others</td><td>Reserved</td></tr></tbody></table> NOTE: If the chip runs in USB OHCI mode, the OCP frequency cannot be lower than 30 MHz. It means that $PLL_FREQ*(CPU_FFRAC/CPU_FDIV)/(CPU_OCP_RATIO+1) \geq 30 \text{ MHz}.$	Value	Ratio (SYS : CPU)	4'd0	1 : 1 (Reserved)	4'd1	1 : 1.5 (Reserved)	4'd2	1 : 2	4'd3	1 : 2.5 (Reserved)	4'd4	1 : 3	4'd5	1 : 3.5 (Reserved)	4'd6	1 : 4	4'd7	1 : 5	4'd8	1 : 10	Others	Reserved	0x4
Value	Ratio (SYS : CPU)																									
4'd0	1 : 1 (Reserved)																									
4'd1	1 : 1.5 (Reserved)																									
4'd2	1 : 2																									
4'd3	1 : 2.5 (Reserved)																									
4'd4	1 : 3																									
4'd5	1 : 3.5 (Reserved)																									
4'd6	1 : 4																									
4'd7	1 : 5																									
4'd8	1 : 10																									
Others	Reserved																									
15:13	-	-	Reserved	0x0																						

Bits	Type	Name	Description	Initial Value
12:8	RW	CPU_FDIV	CPU Frequency Divider The frequency divider is used to generate the CPU frequency. The value must be larger than or equal to CPU_FFRAC. Valid values range from 1 to 31.	0xA
7:5	-	-	Reserved	0x0
4:0	RW	CPU_FFRAC	CPU Frequency Fractional A parameter used in conjunction with the CPU frequency divider to determine the CPU frequency. Input a value in the following equation to determine the CPU frequency. Valid values range from 0 to 31. CPU frequency = $(\text{CPU_FFRAC}/\text{CPU_FDIV}) * \text{PLL_FREQ}$ NOTE: If the chip runs in USB OHCI mode, the OCP frequency cannot be lower than 30 MHz. It means that $\text{PLL_FREQ} * (\text{CPU_FFRAC}/\text{CPU_FDIV}) / (\text{CPU_OCP_RATIO} + 1) \geq 30 \text{ MHz}$.	0x1

NOTE:

- Equation used to derive system frequency after chip boot up:
 $\text{PLL_FREQ} = 600$
 $\text{CPU_FREQ} = \text{PLL_FREQ} * (\text{CPU_FFRAC} / \text{CPU_FDIV})$
 $\text{BUS_FREQ} = \text{CPU_FREQ} / 3$. (CPU_OCP_RATIO = 1:3)
 Limitations:
 $\text{CPU_FDIV} \geq \text{CPU_FFRAC}$.
- If the chip runs the USB function, the OCP frequency cannot be lower than 30 MHz. Then PLL_FREQ follows this limitation.
 $\text{BUS_FREQ} \geq 30 \text{ MHz}$.
- Example:
 $\text{PLL_FREQ} = 600 \text{ MHz}$.
 $\text{CPU_FREQ} = 600 * (1/5) = 300 \text{ MHz}$. (CPU_FFRAC=1; CPU_FDIV=5)
 $\text{BUS_FREQ} = 300/3 = 100 \text{ MHz}$. (CPU_OCP_RATIO=1:3)

16. CLK_LUT_CFG: CPU and SYS Clock Auto Control (offset: 0x0040)

Bits	Type	Name	Description	Initial Value																						
31	RW	SLP_EN	Sleep Mode Enable Enables sleep mode when MIPS SI_Sleep is asserted. 0: Disable 1: Enable Sleep Mode CPU Frequency = (1/CPU_FDIV)*PLL_FREQ	0x0																						
30	RW	STEP_EN	Step Jump Enable Enables step jump after MIPS exits sleep mode. The CPU will jump to the normal frequency in increments defined by STEP_FFRAC.bit[4:0] of this register. 0: Disable 1: Enable	0x0																						
29:28	-	-	Reserved	0x0																						
27:20	RW	STEP_CNT	Step Counter Sets the period of each step jump. When the counter counts down to zero, the CPU clock automatically changes to the next step frequency. The count period unit is 1 μs.	0x2																						
19:16	RW	SLP_OCP_RATIO	Sleep Mode CPU and System Bus Frequency Ratio Sets the ratio between the system bus frequency and the CPU frequency when entering sleep mode. (SYS:CPU) <table><tr><th>Value</th><th>Ratio (SYS : CPU)</th></tr><tr><td>4'd0</td><td>1 : 1</td></tr><tr><td>4'd1</td><td>1 : 1.5 (Reserved)</td></tr><tr><td>4'd2</td><td>1 : 2</td></tr><tr><td>4'd3</td><td>1 : 2.5 (Reserved)</td></tr><tr><td>4'd4</td><td>1 : 3</td></tr><tr><td>4'd5</td><td>1 : 3.5 (Reserved)</td></tr><tr><td>4'd6</td><td>1 : 4</td></tr><tr><td>4'd7</td><td>1 : 5</td></tr><tr><td>4'd8</td><td>1 : 10</td></tr><tr><td>Others</td><td>Reserved</td></tr></table>	Value	Ratio (SYS : CPU)	4'd0	1 : 1	4'd1	1 : 1.5 (Reserved)	4'd2	1 : 2	4'd3	1 : 2.5 (Reserved)	4'd4	1 : 3	4'd5	1 : 3.5 (Reserved)	4'd6	1 : 4	4'd7	1 : 5	4'd8	1 : 10	Others	Reserved	0x4
Value	Ratio (SYS : CPU)																									
4'd0	1 : 1																									
4'd1	1 : 1.5 (Reserved)																									
4'd2	1 : 2																									
4'd3	1 : 2.5 (Reserved)																									
4'd4	1 : 3																									
4'd5	1 : 3.5 (Reserved)																									
4'd6	1 : 4																									
4'd7	1 : 5																									
4'd8	1 : 10																									
Others	Reserved																									
15:5	-	-	Reserved	0x0																						

Bits	Type	Name	Description	Initial Value
4:0	RW	STEP_FFRAC	Step Frequency Fraction Sets the fractional size of the increment in CPU frequency after the CPU exits from sleep mode and returns to normal operation. This step is only valid when SLP_STEP_EN is enabled. FRAC_VALUE = PREVIOUS_FRAC_VALUE + STEP_FFRAC CPU Frequency = (FRAC_VALUE/CPU_FDIV)*PLL_FREQ	0x6

17. CUR_CLK_STS: Current Clock Status (offset: 0x0044)

Bits	Type	Name	Description	Initial Value																						
31:21	-	-	Reserved	0x0																						
20	RO	SAME_FREQ	Indicates that the SYS and DRAM clocks are on the same frequency. 0: False 1: True	-																						
19:16	RO	CUR_OCP_RATIO	Current CPU_OCP_Ratio (SYS : CPU) Shows the current ratio between the system bus and CPU frequencies. <table><tr><th>Value</th><th>Ratio (SYS : CPU)</th></tr><tr><td>4'd0</td><td>1 : 1</td></tr><tr><td>4'd1</td><td>1 : 1.5 (Reserved)</td></tr><tr><td>4'd2</td><td>1 : 2</td></tr><tr><td>4'd3</td><td>1 : 2.5 (Reserved)</td></tr><tr><td>4'd4</td><td>1 : 3</td></tr><tr><td>4'd5</td><td>1 : 3.5 (Reserved)</td></tr><tr><td>4'd6</td><td>1 : 4</td></tr><tr><td>4'd7</td><td>1 : 5</td></tr><tr><td>4'd8</td><td>1 : 10</td></tr><tr><td>Others</td><td>Reserved</td></tr></table>	Value	Ratio (SYS : CPU)	4'd0	1 : 1	4'd1	1 : 1.5 (Reserved)	4'd2	1 : 2	4'd3	1 : 2.5 (Reserved)	4'd4	1 : 3	4'd5	1 : 3.5 (Reserved)	4'd6	1 : 4	4'd7	1 : 5	4'd8	1 : 10	Others	Reserved	-
Value	Ratio (SYS : CPU)																									
4'd0	1 : 1																									
4'd1	1 : 1.5 (Reserved)																									
4'd2	1 : 2																									
4'd3	1 : 2.5 (Reserved)																									
4'd4	1 : 3																									
4'd5	1 : 3.5 (Reserved)																									
4'd6	1 : 4																									
4'd7	1 : 5																									
4'd8	1 : 10																									
Others	Reserved																									
15:13	-	-	Reserved	0x0																						
12:8	RO	CUR_CPU_FDIV	Current CPU Frequency Divider The frequency divider is used to generate the CPU frequency. For more information, see CPU_SYS_CLKCFG, offset 0x003C, bit[12:8].	0xA																						
7:5	-	-	Reserved	0x0																						
4:0	RO	CUR_CPU_FFRAC	Current CPU Frequency Fraction A parameter used in conjunction with the CPU frequency divider to determine the CPU frequency. For more information, see CPU_SYS_CLKCFG, offset 0x003C, bit[4:0].	0x1																						

18. BPLL_CFG0: BB PLL Configuration 0 (offset: 0x0048)

Bits	Type	Name	Description	Initial Value
31	RW	BPLL_SW_CFG	BB PLL Software Configuration Sets BB PLL parameters set by software. 0: Apply default parameters set by hardware. 1: Apply new parameters set by software in BPLL_CFG0 & BPLL_CFG1.	0x0
30:23	-	-	Reserved	0x0
22:20	RW	BBPL_OPTION	Reserved	0x0
19:17	-	-	Reserved	0x0
16	RW	BBPL_PD	BB PLL Power Down 0: Power On 1: Power Down	0x0
15:14	-	-	Reserved	0x0
13	RO	BBPL_FBDV2	BB PLL Feedback Divisor 2 This value depends on the bootstrap pin. <0x0>: 40 MHz <0x1>: 20 MHz	BS
12	RW	BBPL_FOUTDV2	BB PLL Frequency Output Divisor 2 0: Fixed at 960 MHz	0x0
11:8	RW	BBPL_RDV	BB PLL Reference Input Divisor divisor: $M=RDV[3:0]$	0x1
7:4	RW	BBPL_FDV	BB PLL Feedback Divisor Control Sets the real feedback divisor (N) based on the value of BBPL_FBDV2 (bit13). ▪ If FBDV2=0, $N=FDV[3:0]+16$ ▪ If FBDV2=1, $N=2*(FDV[3:0]+16)$	0x8
3:0	RW	BBPL_ODV	FOUT Frequency Control Sets the real output divisor (P) based on the value of BBPL_FOUTDIV2 (bit12). ▪ If FOUTDV2=0, $P=ODV[3:0]$ ▪ If FOUTDV2=1, $P=ODV[3:0]*2$ NOTE: In this chip $ODV[3:0]=0000$, so FOUT=0.	0x1

19. BPLL_CFG1: BB PLL Configuration 0 (offset: 0x004C)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30	RO	BBPL_OK	Lock-detector state 0: Not locked 1: Locked	-

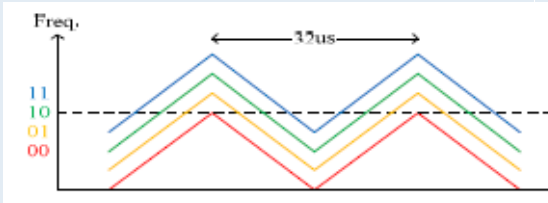
Bits	Type	Name	Description	Initial Value
29:28	RW	BBPL_ICPP	PLL CPP current control Sets the proportional charge pump current. (Default: 01) 00: 25 μ A 10: 75 μ A 01: 50 μ A 11: 100 μ A	0x1
27:26	RW	BBPL_ICPI	PLL CPI current control Sets the integral charge pump current. 00: 1.25 μ A 10: 3.75 μ A 01: 2.5 μ A 11: 5 μ A	0x1
25:24	RW	BBPL_VCS	PLL I-path initial voltage 00: Reserved 10: 600 mV 01: 500 mV 11: 700 mV	0x2
23	RW	BBPL_BP	PLL bypass mode for testing 0: Normal mode 1: Bypass mode	0x0
22:21	RW	BBPL_TESTSEL	Bandgap output test current selection 01: Pass bandgap PMOS current to output 10: Pass bandgap NMOS current to output 11: Reserved	0x0
20:17	RW	BBPL_OTDV	FTEST frequency control Sets the FTEST frequency based on the value of BBPL_FTESTDV2 (bit16). - If FTESTDV2=0, divisor=OTDV[3:0], OTDV[3:0]=0001, FTEST=0 - If FTESTDV2=1, divisor=OTDV[3:0]*2, OTDV[3:0]=0001, FTEST=0 NOTE: In this chip OTDV[3:0]=0000, so FTEST=0.	0x0
16	RW	BBPL_FTESTDV2	FTEST Divisor 2 Used in bit[20:17] to calculate FTEST frequency.	0x1
15	RW	BBPL_FOKTH	Lock Detection FOUT Threshold Selection 0: Freq. window < +/- 3.2% 1: Disable (BBPL_OK=1)	0x0
14:13	RW	BBPL_TSTT	The time AFC waits until BIAS is ready 00: 5 μ s 10: 20 μ s 01: 10 μ s 11: 40 μ s	0x0

Bits	Type	Name	Description	Initial Value
12:11	RW	BBPL_TLCK	BB PLL Time Lock The delay from when AFC is ready to when PLL starts locking. 00: 5 μ s 10: 20 μ s 01: 10 μ s 11: 40 μ s	0x0
10	RW	BBPL_FORCE	Force PLL open loop 0: Close loop 1: Open loop	0x0
9:0	RW	BBPL_AFC	BB PLL Automatic Frequency Calibration VCO band selection/output code[8:0] 0xxxxxxx: Normal 1xxxxxxx: Manual set When read, BBPL_AFC[8:0] is the output code from BBPL macro	0x0

20. CPLL_CFG0: CPU PLL Configuration 0 (offset: 0x0054)

Bits	Type	Name	Description	Initial Value
31	RW	CPLL_SW_CFG	CPU PLL Software Configuration Sets CPU PLL parameters set by software. 0: Apply default parameters set by hardware. 1: Apply new parameters set by software in CPLL_CFG0[25:0], CPLL_CFG1[9:0] and [26].	0x0
30:25	-	-	Reserved	0x0
24	RW	OPEN_LOOP	Force PLL Open Loop Forces PLL to operate in open loop mode. 0: Closed loop 1: Open loop	0x0
23:22	RW	AFC_WAIT_TIME	Automatic Frequency Calibration (AFC) Wait Time The time AFC waits until BIAS is ready. 00: 5 μ s 01: 10 μ s 10: 20 μ s 11: 40 μ s	0x0
21:20	RW	PLL_LOCK_TIME	PLL Lock Time The delay from when AFC is ready to when PLL starts locking. 00: 5 μ s 01: 10 μ s 10: 20 μ s 11: 40 μ s	0x0

Bits	Type	Name	Description	Initial Value
19	RW	EC_CUPLLOCK	CPU Lock OK 0: Check AFC. After AFC, if F_{VCO} is within $\pm 3.2\%$ of the target value, this bit is set to 1. 1: Set this bit to always indicate CPU Lock status is OK, and disable the AFC check.	0x0
18:16	RW	PLL_MULT_RATIO	PLL Multiplying Ratio Sets the ratio between the VCO and reference clock frequencies. - When LC_CURFCK = 0: Factor=1 PLL_MULT_RATIO = $F_{VCO} / F_{REF}(40 \text{ MHz}) / \text{Factor}$ - When LC_CURFCK = 1: Factor=2 PLL_MULT_RATIO = $F_{VCO} / F_{REF}(20 \text{ MHz}) / \text{Factor}$ where F_{VCO} = VCO frequency F_{REF} = Reference clock frequency 000: 24 001: 25 010: 26 011: 27 100: 28 101: 29 110: 30 (default) 111: 31 (test only)	0x6
15	RW	LC_CURFCK	PLL Input Frequency Source 0: 40 MHz 1: 20 MHz	BS
14	RW	BYPASS_REF_CLK	Bypass Reference Clock 0: Normal 1: Bypass	0x0
13:12	RW	IPATH_INI_VAL	I-path Initial Voltage 00: Reserved 01: 500 mV 10: 600 mV (default) 11: 700 mV	0x2

Bits	Type	Name	Description	Initial Value
11:10	RW	PLL_DIV_RATIO	PLL Dividing Ratio Sets the ratio between the VCO and PLL output frequency. $PLL_DIV_RATIO = F_{VCO}/F_{OUT}$. where F_{VCO} = VCO frequency F_{OUT} = PLL output frequency 00: 2 (default) 01: 3 10: 4 11: 8	0x0
9:8	RW	SSC_UP_BOUND	Spread Spectrum Clock (SSC) Frequency Upper Boundary 00: 0 (default) 01: 1/4 SSC swing 10: 2/4 SSC swing 11: 3/4 SSC swing	0x0
				
7	RW	SSC_EN	Spread Spectrum Clock (SSC) Enable Enables the spread spectrum clock (SSC) to reduce EMI and improve SNR. 0: Disable (default) 1: Enable	0x0
6:4	RW	SSC_SWING	SSC Swing 000: 1250 ppm 001: 2500 ppm 010: 3750 ppm 011: 5000 ppm 100: 6250 ppm 101: 7500 ppm 110: 8750 ppm 111: 10000 ppm (default)	0x7
3:2	RW	INT_PATH_OPT	Integration Path Option 00: 1.25 μ A (default) 01: 2.5 μ A 10: 3.75 μ A 11: 5 μ A	0x0
1:0	RW	PRO_PATH_OPT	Proportional Path Option 00: 25 μ A 01: 50 μ A (default) 10: 75 μ A 11: 100 μ A	0x1

21. CPLL_CFG1: CPU PLL Configuration 1 (offset: 0x0058)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	CPLL_PD	CPU PLL Power Down 0: Power on 1: Power down	0x0
25	RW	CPU_CLK_AUX1	CPU Clock Source Select Selects CPU source clock from aux0 or Xtal_IN pins. 0: From aux0 1: From Xtal_IN	0x0
24	RW	CPU_CLK_AUX0	CPU Clock Auxiliary 0 Enable Selects CPU source clock from temporary 480 Mhz clock. 0: Disable 1: Enable	0x0
23	RO	CPLL_LD	CPLL Lock 0: Unlock 1: Lock	-
22:14	RO	EC_CUAFCCOUT	CPU PLL AFC output code	0x0
13:10	RO	EC_CUPHDRFT	SSCG output code (two's complement)	0x0
9:0	RW	FR_CUAFCCSET	CPU PLL AFC Set 0xxxxxxx: Normal 1xxxxxxx: Manual set	0x0

22. USB_PHY_CFG: USB PHY Control (offset: 0x005C)

Bits	Type	Name	Description	Initial Value
31:2	-	-	Reserved	0x0
1	RW	UTMI_8B60M	USB UTMI 8-bit 60 Mhz Mode Select Sets the operation mode of the UTMI interface. 0: 16-bit 30 Mhz mode 1: 8-bit 60 Mhz mode	0x0
0	RW	UDEV_WAKEUP	USB Device Wakeup Enables remote wakeup of the USB device. 0: Disable 1: Enable	0x0

23. GPIOMODE: GPIO Purpose Select (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:30	RW	SUTIF_SHARE_MODE	Serial UTIF Pin Share Mode Sets the serial UTIF pin to operate in UARTL or I ² C mode. 0: Not shared 1: Shared with UARTL -overwrites the UARTLITE_GPIO_MODE setting. 2: Shared with I ² C - overwrites the I2C_GPIO_MODE setting. 3: Reserved	0x0
29:23	-	-	Reserved	0x0
22:21	RW	WDT_RST_MODE	Watchdog Timer GPIO Share Mode Sets the watchdog timer reset pin to operate in REFCLK_OUT or GPIO mode. 0: WDT_RST_N (normal mode) 1: REFCLK0_OUT 2: GPIO mode 3: Reserved	0x0
20	RW	PA_G_GPIO_MODE	Power Amplifier GPIO Share Mode Sets the power amplifier pin to operate in GPIO mode. 0: PA_PE_G0/PA_PE_G1/ANT_TRN/ANT_TRNB (normal mode) 1: GPIO Mode	0x1
19:18	RW	ND_SD_GPIO_MODE	NAND/SD GPIO Share Mode Sets the ND pins to operate in SD, BT or GPIO mode. 0: ND Mode 1: SD Mode (BT Coexist) 2: GPIO Mode 3: Reserved	0x2
17:16	RW	PERST_GPIO_MODE	PCIe Reset GPIO Share Mode Sets the PERST_N pin to operate in REFCLK0 or GPIO mode. 2'b00: PERST_N (normal mode) 2'b01: REFCLK0_OUT 2'b10: GPIO mode 2'b11: Reserved	0x2
15	RW	EPHY_LED_GPIO_MODE	LED JTAG GPIO Share Mode Sets an LED pin to operate in JTAG or GPIO mode. 0: Normal Mode (JTAG/EPHY_LED depending on bootstrapping settings) 1: GPIO Mode	0x0
14	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
13	RW	WLED_GPIO_MODE	WLAN LED GPIO Share Mode Sets the WLAN LED pin to operate in GPIO mode. 0: Normal mode 1: GPIO Mode	0x1
12	RW	SPI_REFCLK0_MODE	SPI Reference Clock GPO Share Mode Sets SPI pins to operate in reference clock and GPO mode. 0: Normal SPI mode 1: SPI_CS1 pins are shared with the reference clock and GPO mode.	0x1
11	RW	SPI_GPIO_MODE	SPI GPIO Share Mode Sets the SPI pins to operate in GPIO mode. 0: Normal Mode 1: GPIO Mode	0x0
10	RW	RGMII2_GPIO_MODE	RGMII2 GPIO Share Mode Sets the RGMII2 pins to operate in GPIO mode. 0: Normal Mode 1: GPIO Mode	0x1
9	RW	RGMII1_GPIO_MODE	RGMII1 GPIO Share Mode Sets the RGMII1 pins to operate in GPIO mode. 0: Normal Mode 1: GPIO Mode	0x1
8:7	RW	MDIO_GPIO_MODE	MDIO GPIO Share Mode Sets the MDIO pin to operate in GPIO mode. 2'b00: Normal Mode 2'b01: REF_CLK Mode 2'b10: GPIO Mode 2'b11: Reserved	0x2
6	-	-	Reserved	0x0
5	RW	UARTL_GPIO_MODE	UART Lite GPIO Share Mode Sets the UART Lite pins to operate in GPIO mode. 0: Normal Mode 1: GPIO Mode	0x1
4:2	RW	UARTF_SHARE_MODE	UART Full Interface Share Mode Sets the UART Full interface to operate in PCM, I2S, and GPIO mode. A detailed description of the UARTF Mode Pin Sharing scheme is shown in the datasheet for this chip.	0x7
1	-	-	Reserved	0x0
0	RW	I2C_GPIO_MODE	I2C GPIO Share Mode Sets the I2C pins to operate in GPIO mode. 0: Normal Mode 1: GPIO Mode	0x1

NOTE: For more information on pin sharing schemes, see the datasheet for this chip.

24. PCIPDMA_STAT: Control and Status of PDMA in PCIe Device (offset: 0x0064)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	0x0
3	RW	PCIPDMA_RX_EN	PDMA Rx DMA Enable In iNIC applications, the external Host can enable the PDMA of a PCIe Device to start Rx PDMA (from the point of view of the external host). However, the actual PDMA Rx is enabled when both of following conditions are met. ▪ MIPS (internal CPU) writes 1 to PCIPDMA_RX_EN. ▪ External Host writes 1 to RX_DMA_EN via BAR1.	0x0
2	RW	PCIPDMA_TX_EN	PDMA Tx DMA Enable In iNIC applications, the external Host can enable the PDMA of a PCIe Device to start Tx PDMA (from the point of view of the external host). However, the actual PDMA Tx is enabled when both of following conditions are met. ▪ MIPS (internal CPU) writes 1 to PCIPDMA_TX_EN. ▪ External Host writes 1 to TX_DMA_EN via BAR1.	0x0
1	RO	PCIPDMA_RX_BUSY	PCIe PDMA Rx Busy Indicates PDMA Rx in the PCIe device is busy. 0: PDMA Rx is idle 1: PDMA Rx is busy	0x0
0	RO	PCIPDMA_TX_BUSY	Indicates PDMA Tx in the PCIe device is busy. 0: PDMA Tx is idle 1: PDMA Tx is busy	0x0

25. PMU0_CFG: (offset: 0x0088)

Bits	Type	Name	Description	Initial Value
31:29	-	-	Reserved	0x0
28	RW	PMU_SW_SET	PMU Software Register Set 0: Set hardware to control the PMU software register. 1: Set software to control the software register field [24:16]	0x0
24	RW	A_DCDC_EN	SW Analog DC/DC Converter Enable 0: Disable 1: Enable	0x1

Bits	Type	Name	Description	Initial Value
23:20	-	-	Reserved	0x0
19	RW	A_SSCPERI	Analog Spread Spectrum Clock Generator (SSCG) Modulation Period Select 0: 16.5 kHz 1: 33 kHz	0x1
18	RW	A_SSCGEN	Analog Spread Spectrum Clock Generator Enable 0: Disable 1: Enable	0x1
17:16	RW	A_SSC	Analog Spread Spectrum Clock Control Increases the SSCG modulation frequency from a base level of 1 MHz. <0x0>: $\pm 5\%$ <0x1>: Reserved <0x2>: $\pm 10\%$ <0x3>: $\pm 20\%$	0x2
15:11	-	-	Reserved	0x0
10:8	RW	A_DLY	Analog Delay Controls the output power MOSFET dead zone. Sets the turn off/delay period between the external upper and lower MOSFET. The periods given below are approximate as the exact value depends on the production process for each chip, the input voltage, and the chip temperature. <0x1>: Approx. 40 nsec <0x2>: Approx. 30 nsec <0x3>: Approx. 20 nsec <0x4>: Approx. 10 nsec	0x2
7:0	RW	A_VTUNE	Analog Voltage Tune Sets the output voltage level. <0x51>: 0.76 V (min) ... <0xB9>: 1.75 V - 20 mv <0xBA>: 1.75 V - 10 mv <0xBB>: 1.75 V (default) <0xBC>: 1.75 V + 10 mv <0xBD>: 1.75 V + 20 mv ... <0xFF> : 2.4 V (max)	0xBB

26. PMU1_CFG: (offset: 0x008C)

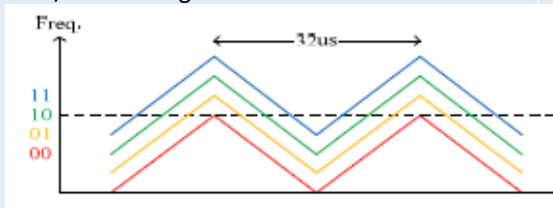
Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
29:28	RW	DIG_LDO_GAIN	DIG_LDO gain control 00: High DC gain 00: Reserved 10: Reserved 11: Low DC gain	0x0
27:26	-	-	Reserved	-
25	RW	DIG_SW_SEL	SW Configured Digital LDO output level 0: HW controlled DIG LDO 1: SW controlled DIG LDO field [24:16]	0x0
24	RW	DIG_LDO_EN	DIG LDO Enable 0: Disable 1: Enable	0x1
23:16	RW	DIG_LDO_VALUE	LDO Output Level Selection	0x69
15:14	-	-	Reserved	-
13:12	RW	DDR_LDO_Gain	DDR LDO gain control 00: High DC gain 00: Reserved 10: Reserved 11: Low DC gain	0x0
11:10	-	-	Reserved	-
9	RW	DDR_SW_SEL	SW Config DDR LDO Output Level 0: HW control DDR LDO (based on bootstrap value) 1: SW control DDR LDO field [8:0]	0x0
8	RW	DDR_LDO_EN	DDR LDO Enable 0: Disable 1: Enable	0x1
7:0	RW	DDR_LDO_VALUE	LDO Output Level Selection default: <10011011> for output=1.8 V (DDR2) <11010101> for output=2.5 V (DDR1)	BS

27. PPLL_CFG0: PCIe PLL Configuration 0 (offset: 0x0098)

Bits	Type	Name	Description	Initial Value
31	RW	PPLL_SW_SET	Programmable PLL Software Set 0: HW sets default PLL parameters 1: SW applies new parameters with PPLL_CFG0[23:0] & PPLL_CFG1[9:0] & PPLL_CFG1[26]	0x0
30:24	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
23:22	RW	AFC_WAIT_TIME	Automatic Frequency Control (AFC) Wait Time The time AFC waits until BIAS is ready. 00: 5 μ s 01: 10 μ s 10: 20 μ s 11: 40 μ s	0x0
21:20	RW	PLL_LOCK_TIME	PLL Lock Time The time PLL starts to lock after AFC is ready. 00: 5 μ s 01: 10 μ s 10: 20 μ s 11: 40 μ s	0x0
19	RW	EC_PEPLLOK	PCIe PLL Lock OK 0: Check AFC. After AFC, if F_{vco} is within $\pm 3.2\%$ of the target value, this bit is set to 1. 1: Set this bit to always indicate CPU Lock status is OK, and disable the AFC check.	0x0
18:17	-	-	Reserved	0x0
16	RW	OPEN_LOOP	PLL Open Loop Forces PLL to operate in open loop mode. 0: Close loop 1: Open loop	0x0
15	RW	LC_PERFCK	(Logic side Code) PCIe Reference Clock Frequency Source 0: 40 MHz 1: 20 MHz	BS
14	RW	BYPASS_REF_CLK	Bypass Reference Clock 0: Normal 1: Bypass	0x0
13:12	RW	IPATH_INI_VAL	I-path Initial Voltage 00: Reserved 01: 500 mV 10: 600 mV (default) 11: 700 mV	0x2
11:10	RW	PLL_OUT_FREQ	Output Clock Frequency 00: 50 MHz (test only) 01: 100 MHz (default) 10: 200 MHz (test only) 11: 600 MHz (test only)	0x1

Bits	Type	Name	Description	Initial Value
9:8	RW	SSC_UP_BOUND	Spread Spectrum Clock (SSC) Frequency Upper Boundary 00: 0 (default) 01: 1/4 SSC swing 10: 2/4 SSC swing 11: 3/4 SSC swing	0x0
				
7	RW	SSC_EN	SSC Enable Enables the spread spectrum clock (SSC) to reduce EMI and improve SNR. 0: Disable (default) 1: Enable	0x0
6:4	RW	SSC_SWING	SSC Swing 000: 1250 ppm 001: 2500 ppm 010: 3750 ppm 011: 5000 ppm 100: 6250 ppm 101: 7500 ppm 110: 8750 ppm 111: 10000 ppm (default)	0x3
3:2	RW	INT_PATH_OPT	Integration Path Option 00: 1.25 μ A (default) 01: 2.5 μ A 10: 3.75 μ A 11: 5 μ A	0x0
1:0	RW	PRO_PATH_OPT	Proportional Path Option 00: 25 μ A 01: 50 μ A (default) 10: 75 μ A 11: 100 μ A	0x1

28. PPLL_CFG1: PCIe PLL Configuration 1 (offset: 0x009C)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	PPLL_PD	PPLL Power Down 0: Power On 1: Power down	0x0
25:24	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
23	RO	PPLL_LD	PPLL Lock 0: Unlock 1: Lock	-
22:14	RO	EC_PEAFCOUT	PCIe PLL AFC output	0x0
13:10	RO	EC_PEPHDRFT	PCIe PLL Phase Drift SSCG output code (two's complement)	0x0
9:0	RW	FR_PEAFCSET	PCIe PLL AFC Set 0xxxxxxx: Normal 1xxxxxxx: Manual set	0x0

29. PPLL_DRV: PCIe Driver Configuration (offset: 0x00A0)

Bits	Type	Name	Description	Initial Value
31	RW	PDRV_SW_SET	PCIe Driver Software Set 0: HW sets default parameters 1: SW configures values for [19:0] in this register.	0x0
30:20	-	-	Reserved	0x0
19	RW	LC_CKDRVPD	(Logic side Code) PCIe Clock Driver Power Down (Low Active) 0: Power Down 1: Power On	0x0
18	RW	LC_CKDRVOHZ	(Logic side Code) Reference PCIe Output Clock Mode Enable 0: Enable output clock (Host mode only) 1: High Impedance (Device mode)	0x1
17	RW	LC_CKDRVHZ	(Logic side Code) PCIe PHY Clock Enable 0: Enable clock (Host mode only) 1: High Impedance (Device mode)	0x1
16	RW	LC_CKTEST	(Logic side Code) Single-ended clock for output testing 0: Normal operation 1: Testing only	0x0
15:0	RW	FR_CKDRVHZ	PCIe Clock Driver Set (default 0000-0101-0000-0100) See NOTE below.	0x0504

NOTE: [15:0] bit values are as follows.

Bits	Description						
15:13	Reserved						
12	Input clock selection						
	<table border="1"> <tr> <th>Value</th><th>Description</th></tr> <tr> <td>0</td><td>From PEPLL</td></tr> <tr> <td>1</td><td>From LC_CKTEST</td></tr> </table>	Value	Description	0	From PEPLL	1	From LC_CKTEST
Value	Description						
0	From PEPLL						
1	From LC_CKTEST						

Bits	Description					
11:10	Output voltage level					
	Value	Description				
	00	0.7 V				
	10	0.8 V				
	01	0.75 V				
	11	0.85 V				
9	Reserved					
8:4	Output termination adjustment					
	Value	Description	Value	Description	Value	Description
	00000	70	01010	52	10101	41
	00001	66	01011	51	10110	40
	00010	64	01100	50	10111	39
	00011	62	01101	49	11000	38.5
	00100	61	01110	48	11001	38
	00101	59	01111	47	11010	37.5
	00110	58	10000	46	11011	37
	00111	56	10001	45	11100	36.5
	01000	55	10010	44	11101	36
	01001	54	10011	43	11110	35.5
			10100	42	11111	35
3:2	Output slew-rate control					
	Value	Description				
	00	1.71 V/ns				
	01	1.12 V/ns				
	10	0.78 V/ns				
	11	0.6 V/ns				
1:0	Reserved					

2.3 Timer

2.3.1 Features

- Independent clock pre-scale for each timer.
- Independent interrupts for each timer.
- Two general-purpose timers which run at a 40 MHz clock rate. The other two run at a 32 kHz clock rate.
 - Periodic mode
 - Free-running mode
 - Time-out mode
 - Second timer may be used as a watchdog timer. Watchdog timer resets system on time-out.
- Timer Modes
 - *Periodic*

In periodic mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. After reaching zero, the load value is reloaded into the timer and the timer counts down again. A load value of zero disables the timer.
 - *Timeout*

In timeout mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. In this mode, the ENABLE bit is reset when the timer reaches zero, stopping the counter. After reaching zero, the load value is reloaded into the timer. A load value of zero disables the timer.
 - *Free-running*

In free-running mode, the timer counts down to zero from FFFFh. An interrupt is generated when the count is zero. After reaching zero, FFFFh is reloaded into the timer. This mode is identical to the periodic mode with a load value of 65535. It is worth noting that if firmware writes to the load value register in this mode, the timer will still load that value even though that value will be ignored thereafter. Also note that when the timer is first enabled, it will begin counting down from its current value, not necessarily FFFFh.
 - *Watchdog*

In watchdog mode, the timer counts down to zero from the load value. If the load value is not reloaded or the timer is not disabled before the count is zero, the chip will be reset. When this occurs, every register in the chip is reset except the watchdog reset status bit WDRST in the RSTSTAT register in the system control block; it remains set to alert firmware of the timeout event when it re-executes its bootstrap.

2.3.2 Block Diagram

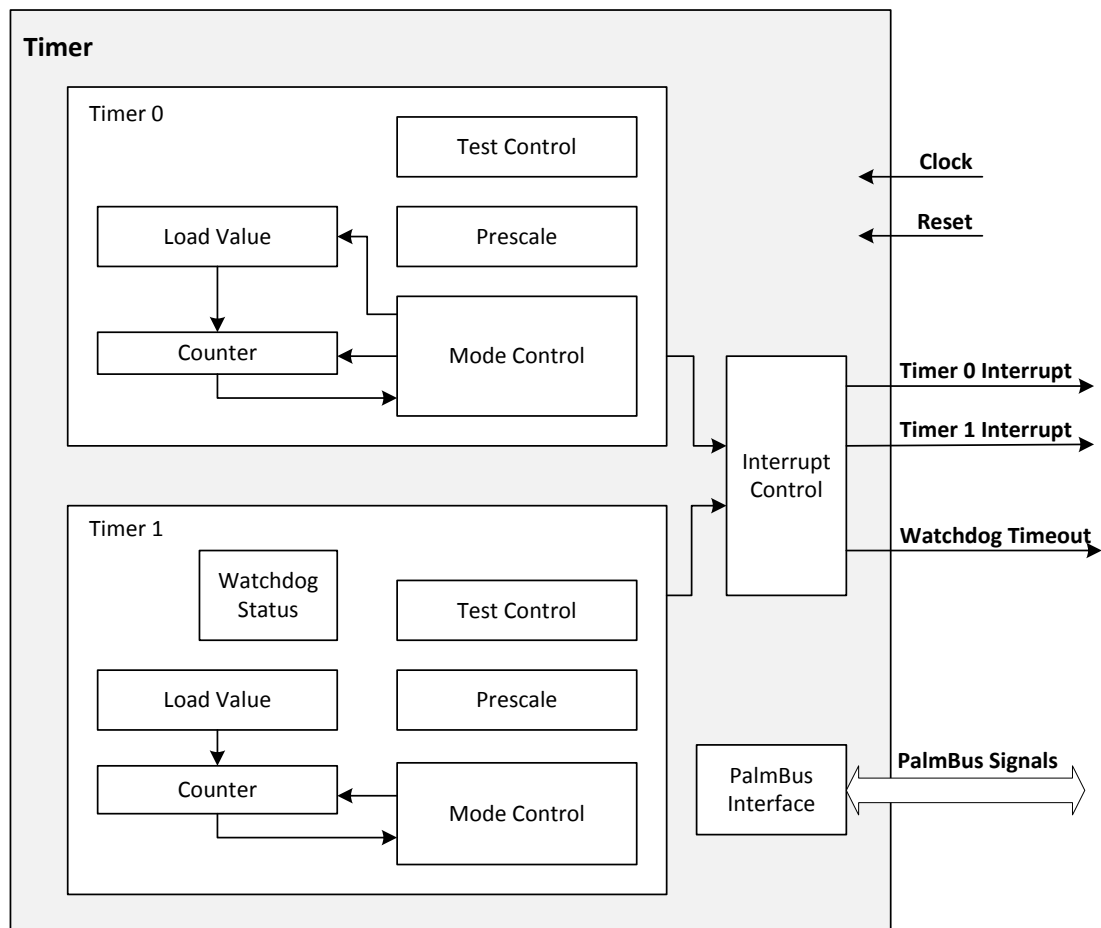


Figure 2-2 Timer Block Diagram

2.3.3 List of Registers

No.	Offset	Register Name	Description	Page
30	0x0000	TMRSTAT	Timer Status	49
31	0x0010	TMR0LOAD	Timer 0 Load Value	50
32	0x0014	TMR0VAL	Timer 0 Counter Value	50
33	0x0018	TMR0CTL	Timer 0 Control	50
34	0x0020	TMR1LOAD	Timer 1 Load Value	51
35	0x0024	TMR1VAL	Timer 1 Counter Value	51
36	0x0028	TMR1CTL	Timer 1 Control	51

2.3.4 Register Descriptions (base: 0x1000_0100)

30. TMRSTAT: Timer Status Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:6	-	-	Reserved	0x0
5	WO	TMR1RST	Timer 1 Reset <i>Read</i> Reading this bit returns a 0. <i>Write</i> 0: No effect. 1: Reset Timer 1 to 0xFFFF if in free-running mode, or to the value specified in the TMR1LOAD register in all other modes.	0x0
4	WO	TMR0RST	Timer 0 Reset <i>Read</i> Reading this bit returns a 0. <i>Write</i> 0: No effect. 1: Reset Timer 0 to 0xFFFF if in free-running mode, or to the value specified in the TMR0LOAD register in all other modes.	0x0
3:2	-	-	Reserved	0x0
1	R/W1C	TMR1INT	Timer 1 Interrupt Status Indicates that timer 1 has expired and timer 1 interrupt to the processor has asserted. After the interrupt is sent, the bit is written to 1 and cleared. <i>Read</i> 0: Not asserted. 1: Asserted. <i>Write</i> 0: No effect 1: Clears the interrupt.	0x0
0	R/W1C	TMR0INT	Timer 0 Interrupt Status Indicates that timer 0 has expired and timer 0 interrupt to the processor has asserted. After the interrupt is sent, the bit is written to 1 and cleared. <i>Read</i> 0: Not asserted. 1: Asserted. <i>Write</i> 0: No effect 1: Clears the interrupt.	0x0

31. TMR0LOAD: Timer 0 Load Value (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:16	RO	-	Reserved	0x0
15:0	RW	TMRLOAD	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. 0: Disables the timer, except in free-running mode.	0x0

32. TMR0VAL: Timer 0 Counter Value (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RO	TMRVAL	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	0xffff

33. TMR0CTL: Timer 0 Control (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15	RW	TESTEN	Test Enable Reserved for testing. This bit should be set to 0.	0x0
14:8	-	-	Reserved	0x0
7	RW	ENABLE	Timer Enable Enables the 40 MHz timer0. 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	0x0
6	-	-	Reserved	0x0
5:4	RW	MODE	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Time-out	0x0

Bits	Type	Name	Description	Initial Value																
3:0	RW	PRESCALE	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. <table><tr><th>Value</th><th>Timer Clock Frequency</th></tr><tr><td>0</td><td>System clock</td></tr><tr><td>1</td><td>System clock / 4</td></tr><tr><td>2</td><td>System clock / 8</td></tr><tr><td>3</td><td>System clock / 16</td></tr><tr><td>...</td><td>...</td></tr><tr><td>14</td><td>System clock / 32768</td></tr><tr><td>15</td><td>System clock / 65536</td></tr></table> NOTE: The pre-scale value should not be changed unless the timer is disabled.	Value	Timer Clock Frequency	0	System clock	1	System clock / 4	2	System clock / 8	3	System clock / 16	...	...	14	System clock / 32768	15	System clock / 65536	0x0
Value	Timer Clock Frequency																			
0	System clock																			
1	System clock / 4																			
2	System clock / 8																			
3	System clock / 16																			
...	...																			
14	System clock / 32768																			
15	System clock / 65536																			

34. TMR1LOAD: Timer 1 Load Value (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	TMRLOAD	Timer Load Value This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. 0: Disable the timer, except in free-running mode.	0x0

35. TMR1VAL: Timer 1 Counter Value (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RO	TMRVAL	Timer Counter Value This register contains the current value of the timer. During functional operation, writes have no effect.	0xffff

36. TMR1CTL: Timer 1 Control (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15	RW	TESTEN	Test Enable Reserved for testing. This bit should be set to 0.	0x0

Bits	Type	Name	Description	Initial Value																
14:8	-	-	Reserved	0x0																
7	RW	ENABLE	Timer Enable Enables the 40 MHz timer1. 0: Disable the timer. The timer will stop counting and will retain its current value. 1: Enable the timer. The timer will begin counting from its current value.	0x0																
6	RW	WD_TIMEOUT_SRC	Watchdog Timeout Alarm Source 0: From Timer 1 1: From PMU watch dog timer	0x0																
5:4	RW	MODE	Timer Mode 0: Free-running 1: Periodic 2: Time-out 3: Watchdog	0x0																
2:0	RW	PRESCALE	Timer Clock Pre-scale These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. <table><tr><th>Value</th><th>Timer Clock Frequency</th></tr><tr><td>0</td><td>System clock</td></tr><tr><td>1</td><td>System clock / 4</td></tr><tr><td>2</td><td>System clock / 8</td></tr><tr><td>3</td><td>System clock / 16</td></tr><tr><td>...</td><td>...</td></tr><tr><td>14</td><td>System clock / 32768</td></tr><tr><td>15</td><td>System clock / 65536</td></tr></table> NOTE: The pre-scale value should not be changed unless the timer is disabled.	Value	Timer Clock Frequency	0	System clock	1	System clock / 4	2	System clock / 8	3	System clock / 16	...	...	14	System clock / 32768	15	System clock / 65536	0x0
Value	Timer Clock Frequency																			
0	System clock																			
1	System clock / 4																			
2	System clock / 8																			
3	System clock / 16																			
...	...																			
14	System clock / 32768																			
15	System clock / 65536																			

2.4 Interrupt Controller

2.4.1 Features

- Supports a central point for interrupt aggregation for platform related blocks
- Separated interrupt enable and disable registers
- Supports global disable function
- 2-level Interrupt priority selection
- Each interrupt source can be directed to IRQ#0 or IRQ#1

NOTE: MT7620 supports MIPS 24K's vector interrupt mechanism.

There are 6 hardware interrupts supported by MIPS 24K. The interrupt allocation is shown below:

MIPS H/W interrupt pins	Connect to	Remark
HW_INT#5	Timer interrupt	Highest priority
HW_INT#4	Reserved	
HW_INT#3	FE	
HW_INT#2	PCIe	
HW_INT#1	Other high priority interrupts (IRQ#1)	
HW_INT#0	Other low priority interrupts (IRQ#0)	Lowest priority

2.4.2 Block Diagram

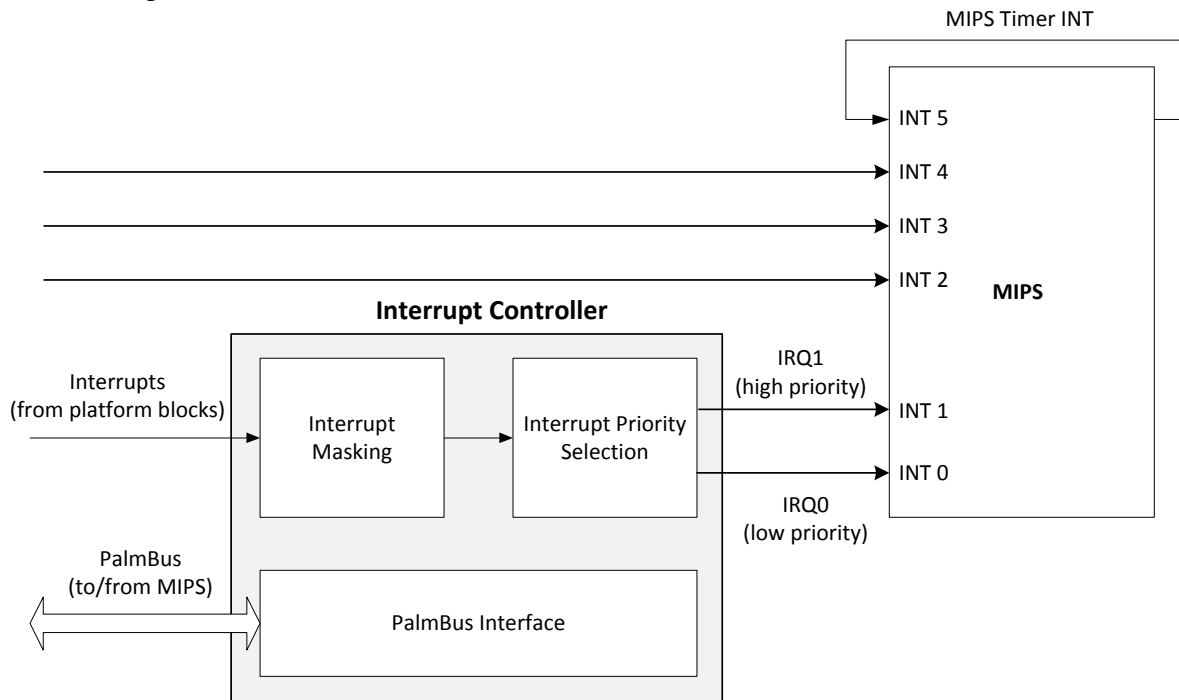


Figure 2-3 Interrupt Controller Block Diagram

2.4.3 List of Registers

No.	Offset	Register Name	Description	Page
37	0x0000	IRQ0STAT	Interrupt Type 0 Status after Enable Mask	55
38	0x0004	IRQ1STAT	Interrupt Type 1 Status after Enable Mask	55
39	0x0020	INTTYPE	Interrupt Type	56
40	0x0030	INTRAW	Raw Interrupt Status before Enable Mask	57
41	0x0034	INTENA	Interrupt Enable	58
42	0x0038	INTDIS	Interrupt Disable	58

2.4.4 Register Descriptions (base: 0x1000_0200)

37. IRQ0STAT: Interrupt Type 0 Status after Enable Mask (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	-
19	RO	UDEV	USB device interrupt status after mask	0x0
18	RO	UHST	USB host interrupt status after mask	0x0
17	RO	ESW	Ethernet Switch interrupt status after mask	0x0
16	-	-	Reserved	0x0
15	RO	R2P	R2P interrupt after mask	0x0
14	RO	SDHC	SDHC interrupt after mask	0x0
13	-	-	Reserved	0x0
12	RO	UARTLITE	UARTLITE interrupt status after mask	0x0
11	RO	SPI	SPI interrupt status after mask	0x0
10	RO	I2S	I2S interrupt status after mask	0x0
9	RO	PC	MIPS performance counter interrupt status after mask	0x0
8	-	-	Reserved	0x0
7	RO	DMA	DMA interrupt status after mask	0x0
6	RO	PIO	PIO interrupt status after mask	0x0
5	RO	UART	UART interrupt status after mask	0x0
4	RO	PCM	PCM interrupt status after mask	0x0
3	RO	ILL_ACC	Illegal access interrupt status after mask	0x0
2	RO	WDTIMER	Watchdog timer interrupt status after mask	0x0
1	RO	TIMER0	Timer 0 interrupt status after mask	0x0
0	RO	SYSCTL	System control interrupt status after mask	0x0

NOTE: These bits are set if the corresponding interrupt is asserted from the source and with the following two conditions.

1. The interrupt is not masked (the bit is not set in the INTDIS register)
2. The interrupt type is set to INTO (in the INTTYPE register).

NOTE: Writing to these bits is ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

38. IRQ1STAT: Interrupt Type 1 Status after Enable Mask (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	-
19	RO	UDEV	USB device interrupt status after mask	0x0
18	RO	UHST	USB host interrupt status after mask	0x0
17	RO	ESW	Ethernet Switch interrupt status after mask	0x0
16	-	-	Reserved	0x0
15	RO	R2P	R2P interrupt after mask	0x0

Bits	Type	Name	Description	Initial Value
14	RO	SDHC	SDHC interrupt after mask	0x0
13	-	-	Reserved	0x0
12	RO	UARTLITE	UARTLITE interrupt status after mask	0x0
11	RO	SPI	SPI interrupt status after mask	0x0
10	RO	I2S	I2S interrupt status after mask	0x0
9	RO	PC	MIPS performance counter interrupt status after mask	0x0
8	-	-	Reserved	0x0
7	RO	DMA	DMA interrupt status after mask	0x0
6	RO	PIO	PIO interrupt status after mask	0x0
5	RO	UART	UART interrupt status after mask	0x0
4	RO	PCM	PCM interrupt status after mask	0x0
3	RO	ILL_ACC	Illegal access interrupt status after mask	0x0
2	RO	WDTIMER	Watchdog timer interrupt status after mask	0x0
1	RO	TIMER0	Timer 0 interrupt status after mask	0x0
0	RO	SYSCTL	System control interrupt status after mask	0x0

NOTE: These bits are set if the corresponding interrupt is asserted from the source and with the following two conditions:

1. The interrupt is not masked (the bit is not set in the INTDIS register)
2. The interrupt type is set to INT1 (in the INTTYPE register).

NOTE: Writing to these bits is ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

39. INTTYPE: Interrupt Type (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	-
19	RW	UDEV	USB device interrupt status type	0x0
18	RW	UHST	USB host interrupt status type	0x0
17	RW	ESW	Ethernet Switch interrupt status type	0x0
16	-	-	Reserved	0x0
15	RW	R2P	R2P Interrupt status type	0x0
14	RW	SDHC	SDHC Engine interrupt status type	0x0
13	-	-	Reserved	0x0
12	RW	UARTLITE	UARTLITE interrupt status type	0x0
11	RW	SPI	SPI interrupt status type	0x0
10	RW	I2S	I2S interrupt status type	0x0
9	RW	PC	MIPS performance counter interrupt status type	0x0
8	-	-	Reserved	0x0
7	RW	DMA	DMA interrupt status type	0x0

Bits	Type	Name	Description	Initial Value
6	RW	PIO	PIO interrupt status type	0x0
5	RW	UART	UART interrupt status type	0x0
4	RW	PCM	PCM interrupt status type	0x0
3	RW	ILL_ACC	Illegal access interrupt status type	0x0
2	RW	WDTIMER	Watchdog timer interrupt status type	0x0
1	RW	TIMER0	Timer 0 interrupt status type	0x0
0	RW	SYSCTL	System control interrupt status type	0x0

NOTE:

0: IRQ type 0

1: IRQ type 1

The interrupt type may be changed at any time; if the interrupt type is changed while the interrupt is active, the interrupt is immediately redirected.

40. INTRAW: Raw Interrupt Status before Enable Mask (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RO	UDEV	USB device interrupt status before mask	0x0
18	RO	UHST	USB host interrupt status before mask	0x0
17	RO	ESW	Ethernet Switch interrupt status before mask	0x0
16	-	-	Reserved	0x0
15	RO	R2P	R2P interrupt status before mask	0x0
14	RO	SDHC	SDHC interrupt status before mask	0x0
13	-	-	Reserved	0x0
12	RO	UARTLITE	UARTLITE interrupt status before mask	0x0
11	RO	SPI	SPI interrupt status before mask	0x0
10	RO	I2S	I2S interrupt status before mask	0x0
9	RO	PC	MIPS performance counter interrupt status before mask	0x0
8	-	-	Reserved	0x0
7	RO	DMA	DMA interrupt status before mask	0x0
6	RO	PIO	PIO interrupt status before mask	0x0
5	RO	UART	UART interrupt status before mask	0x0
4	RO	PCM	PCM interrupt status before mask	0x0
3	RO	ILL_ACC	Illegal access interrupt status before mask	0x0
2	RO	WDTIMER	Watchdog timer interrupt status before mask	0x0
1	RO	TIMER0	Timer 0 interrupt status before mask	0x0
0	RO	SYSCTL	System control interrupt status before mask	0x0

NOTE: These bits are set if the corresponding interrupt is asserted from the source. The status bit is set if the interrupt is active, even if it is masked, and regardless of the interrupt type. This provides a single-access snapshot of all active interrupts for implementation of a polling system.

41. INTENA: Interrupt Enable (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31	RW	GLOBAL	Global Interrupt Enable Allows local interrupts in this register to be individually enabled. Set this bit before enabling interrupts in this register.	0x0
30:20	-	-	Reserved	0x0
19	-	-	Reserved	0x0
18	RW	UHST	USB host interrupt enable	0x0
17	RW	ESW	Ethernet Switch interrupt enable	0x0
16	-	-	Reserved	0x0
15	RW	R2P	R2P interrupt enable	0x0
14	RW	SDHC	SDHC interrupt enable	-
13	-	-	Reserved	-
12	RW	UARTLITE	UARTLITE interrupt enable	0x0
11	RW	SPI	SPI interrupt enable	0x0
10	RW	I2S	I2S interrupt enable	0x0
9	RW	PC	MIPS performance counter interrupt enable	0x0
8	-	-	Reserved	0x0
7	RW	DMA	DMA interrupt enable	0x0
6	RW	PIO	PIO interrupt enable	0x0
5	RW	UART	UART interrupt enable	0x0
4	RW	PCM	PCM interrupt enable	0x0
3	RW	ILL_ACC	Illegal access interrupt enable	0x0
2	RW	WDTIMER	Watchdog timer interrupt enable	0x0
1	RW	TIMER0	Timer 0 interrupt enable	0x0
0	RW	SYSCTL	System control interrupt enable	0x0

NOTE: Where applicable,
1: Enable

42. INTDIS: Interrupt Disable (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31	RW	GLOBAL	Global Interrupt Disable Allows local interrupts in this register to be individually disabled. Set this bit before disabling interrupts in this register.	0x0
30:20	-	-	Reserved	0x0
19	-	-	Reserved	0x0
18	RW	UHST	USB host interrupt status disable	0x0
17	RW	ESW	Ethernet Switch interrupt disable	0x0
16	-	-	Reserved	0x0
15	RW	R2P	R2P interrupt disable	0x0

Bits	Type	Name	Description	Initial Value
14	RW	SDHC	SDHC interrupt disable	0x0
13	-	-	Reserved	0x0
12	RW	UARTLITE	UARTLITE interrupt disable	0x0
11	RW	SPI	SPI interrupt disable	0x0
10	RW	I2S	I2S interrupt disable	0x0
9	RW	PC	MIPS performance counter interrupt disable	0x0
8	RW	NAND	NAND flash controller interrupt disable	0x0
7	RW	DMA	DMA interrupt disable	0x0
6	RW	PIO	PIO interrupt disable	0x0
5	RW	UART	UART interrupt disable	0x0
4	RW	PCM	PCM interrupt disable	0x0
3	RW	ILL_ACC	Illegal access interrupt disable	0x0
2	RW	WDTIMER	Watchdog timer interrupt disable	0x0
1	RW	TIMER0	Timer 0 interrupt disable	0x0
0	RW	SYSCTL	System control interrupt disable	0x0

NOTE: Where applicable,
1: Disable

2.5 System Tick Counter

2.5.1 List of Registers

No.	Offset	Register Name	Description	Page
43	0x0000	STCK_CNT_CFG	MIPS Configuration	61
44	0x0004	CMP_CNT	MIPS Compare	61
45	0x0008	CNT	MIPS Counter	61

2.5.2 Register Descriptions (base: 0x1000_0d00)

43. STCK_CNT_CFG: MIPS Configuration Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:2	-	-	Reserved	-
1	RW	EXT_STK_EN	External System Tick Enable Selects the system tick source 0: Use the MIPS internal timer interrupt. 1: Use the external timer interrupt from an external MIPS counter.	0x0
0	RW	CNT_EN	Count Enable Enables the free run counter (MIPS counter). This counter increments every 20 μ s. 0: Disable 1: Enable	0x0

44. CMP_CNT: MIPS Compare Register (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RW	CMP_CNT	Compare Count Sets the cutoff point for the free run counter (MIPS counter). If the free run counter equals the compare counter, then the timer circuit generates an interrupt. The interrupt remains active until the compare counter is written again.	0x0

45. CNT: MIPS Counter Register (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RW	CNT	MIPS Counter The MIPS counter (free run counter) increases by 1 every 20 μ s (50 KHz). The counter continues to count until it reaches the value loaded into CMP_CNT.	0x0

2.6 UART

2.6.1 Features

- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345 600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

2.6.2 Block Diagram

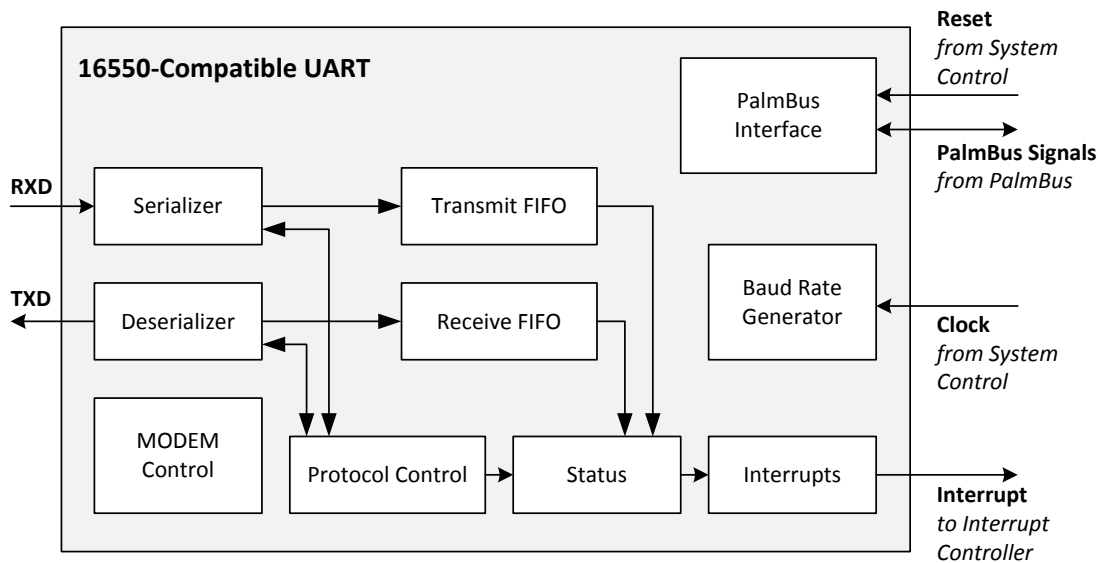


Figure 2-4 UART Block Diagram

2.6.3 List of Registers

No.	Offset	Register Name	Description	Page
46	0x0000	RBR	Receive Buffer Register	64
47	0x0004	TBR	Transmit Buffer Register	64
48	0x0008	IER	Interrupt Enable Register	64
49	0x000C	IIR	Interrupt Identification Register	65
50	0x0010	FCR	FIFO Control Register	66
51	0x0014	LCRLCR	Line Control Register	66
52	0x0018	MCR	Modem Control Register	67
53	0x001C	LSR	Line Status Register	68
54	0x0020	MSR	Modem Status Register	69
55	0x0024	SCRATCH	Scratch	70
56	0x0028	DL	Clock Divider Divisor Latch	70
57	0x002C	DLLO	Clock Divider Divisor Latch Low	71
58	0x0030	DLHI	Clock Divider Divisor Latch High	71

2.6.4 Register Descriptions (base: 0x1000_0500)

46. RBR: Receive Buffer Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	-
7:0	RO	RXD	Receive Buffer Data Data is transferred to this register from the receive shift register after a full character is received. If the contents of this register have not been read before another character is received, the OE bit in the LSR register is set, indicating a received data buffer overrun.	0x0

47. TBR: Transmit Buffer Register (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	-
7:0	RO	TXD	Transmit Buffer Data When a character is written to this register, it is stored in the transmitter holding register. If the transmitter register is empty, the character is moved to the transmitter register, starting transmission.	0x0

48. IER: Interrupt Enable Register (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	-
3	RW	EDSSI	Enable Modem Interrupt Enables the following modem status interrupts. ▪ Data Carrier Detect (DCD) ▪ Ring Indicator (RI) ▪ Data Set Ready (DSR) ▪ Clear to Send (CTS) ▪ Delta Data Carrier Detect (DDCD) ▪ Trailing Edge Ring Indicator (TERI) ▪ Delta Data Set Ready (DDSR) to Send (DCTS)	0x0
2	RW	ELSI	Enable Receiver Line Status Interrupt Enables the following receive line status interrupts. ▪ Overrun Error (OE) ▪ Parity Error (PE) ▪ Framing Error (FE) ▪ Break Interrupt (BI)	0x0
1	RW	ETBEI	Enable Transmit Buffer Empty Interrupt Enables the transmit buffer empty (THRE) interrupt.	0x0

Bits	Type	Name	Description	Initial Value
0	RW	ERBFI	Enable Rx Buffer Full Interrupt Enables the receive buffer full interrupt, as well as the data ready (DR) and character time-out interrupts.	0x0

NOTE:

0: Disable

1: Enable

49. IIR: Interrupt Identification Register (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	-
7:6	RO	FIFOEN	FIFOs Enabled These bits reflect the FIFO enable bit setting in the FIFO Control Register. 00: FIFO enable bit is cleared. 11: FIFO enable bit is set.	0x0
5:4	-	-	Reserved	0x0
3:1	RO	INTID	Interrupt Identifier These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. See NOTE below.	0x0
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	0x1

NOTE:

The interrupt encoding is given below.

ID	Priority	Type	Source
7		Undefined	
6		Undefined	
5		Undefined	
4		Undefined	
3	1 (highest)	Receiver Line Status	OE, PE, FE, BI
2	2	Receiver Buffer Full	DR
1	3	Transmitter Buffer Empty	THRE
0	4 (lowest)	Modem Status	DCTS, DDSR, RI, DCD

If more than one category of interrupt is asserted, only the highest priority ID is given.

The line and modem status interrupts are cleared by reading the corresponding status register in the UART block (LSR (0x001C), MSR (0x0020)). The receive buffer full interrupt is cleared when all of the data is read from the receive buffer. The transmit buffer empty interrupt is cleared when data is written to the TBR register (0x0004) in the UART block.

50. FCR: FIFO Control Register (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	-
7:6	RW	RXTRIG	Rx Trigger Level Sets the number of characters contained by the receive buffer which triggers assertion of the data ready (DR) interrupt. 0: 1 1: 4 2: 8 3: 14 NOTE: This register is not used if the receive FIFO is disabled.	0x0
5:4	RW	TXTRIG	Tx Trigger Level Sets the number of characters contained by the transmit buffer which triggers the threshold empty (THRE) interrupt. 0: 1 1: 4 2: 8 3: 12	0x0
3	RW	DMAMODE	Enable DMA transfers This bit is writeable and readable, but has no other hardware function.	0x0
2	WO	TXRST	Tx Reset 1: Clears the transmit FIFO and resets the transmit status. The shift register is not cleared.	0x0
1	WO	RXRST	Rx Reset 1: Clears the receive FIFO and resets the receive status. The shift register is not cleared.	0x0
0	RW	FIFOENA	FIFO Enable Enables Tx and Rx FIFOs. When disabled, the FIFOs have an effective depth of one character. 0: Disable 1: Enable NOTE: The FIFO status and data are automatically cleared when this bit is changed.	0x0

51. LCR: Line Control Register (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RW	DLAB	Divisor Latch Access Bit This bit has no functionality, and is retained for compatibility only	0x0

Bits	Type	Name	Description	Initial Value
6	RW	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to 0. Tx otherwise operates normally.	0x0
5	RW	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to 0. If odd parity is selected, the (transmitted and checked) parity if forced to 1.	0x0
4	RW	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is 1). 1: Even parity selected (checksum, including parity is 0). NOTE: This bit is ignored if the PEN bit is 0.	0x0
3	RW	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	0x0
2	RW	STB	Stop Bit Select 0: 1 Stop Bit is transmitted and received. 1: 1.5 Stop Bits are transmitted and received if WLS is 0; 2 Stop Bits are transmitted and received if WLS is 1, 2, or 3.	0x0
1:0	RW	WLS	Word Length Select Selects the character length. 0: Each character is 5 bits in length 1: Each character is 6 bits in length 2: Each character is 7 bits in length 3: Each character is 8 bits in length	0x0

52. MCR: Modem Control Register (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:5	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value												
4	RW	LOOP	Loopback Mode Enable 0: Normal Operation. 1: The UART is put into loopback mode, and used for self-testing. The TXD pin is driven high; the TXD signal connections are made internally. <table><tr><td>Signal</td><td>Wrapped Back Through:</td></tr><tr><td>TXD</td><td>RXD</td></tr><tr><td>DTRN</td><td>DSRN</td></tr><tr><td>RTSN</td><td>CTSN</td></tr><tr><td>OUT1N</td><td>RIN</td></tr><tr><td>OUT2N</td><td>DCDN</td></tr></table>	Signal	Wrapped Back Through:	TXD	RXD	DTRN	DSRN	RTSN	CTSN	OUT1N	RIN	OUT2N	DCDN	0x0
Signal	Wrapped Back Through:															
TXD	RXD															
DTRN	DSRN															
RTSN	CTSN															
OUT1N	RIN															
OUT2N	DCDN															
3	RW	OUT2	OUT2 Pin Value 0: OUT2N pin is driven to a high level. 1: OUT2N pin is driven to a low level. NOTE: This bit is only functional in loopback mode.	0x0												
2	RW	OUT1	OUT1 Pin Value 0: OUT1N pin is driven to a high level. 1: OUT1N pin is driven to a low level. NOTE: This bit is only functional in loopback mode.	0x0												
1	RW	RTS	RTSN1 Pin Value 0: RTSN pin is driven to a high level. 1: RTSN pin is driven to a low level.	0x0												
0	RW	DTR	DTRN 1 Pin Value 0: DTRN pin is driven to a high level. 1: DTRN pin is driven to a low level.	0x0												

53. LSR: Line Status Register (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RC	ERINFIFO	Error in FIFO Indicates that a FIFO contains data which was received with a parity error, framing error, or break condition.	0x0
6	RC	TEMT	Transmit Shift Register Empty Indicates that the transmit shift register is empty. This bit is reset when data is written to the transmit buffer register (TBR).	0x1
5	RC	THRE	Transmit Holding Register Empty Indicates that the transmitter holding register is empty. This bit is reset when data is written to the transmit buffer register (TBR).	0x1

Bits	Type	Name	Description	Initial Value
4	RC	BI	Break Interrupt Indicates that a break is received, that is, when the RXD signal is at a low state for more than one character transmission time (from Start Bit to Stop Bit). Under this condition, a single 0 is received.	0x0
3	RC	FE	Framing Error Indicates that a valid Stop Bit is not detected. If a framing error occurs, the receive buffer will attempt to re-synchronize by sampling the Start Bit twice and then receiving the data.	0x0
2	RC	PE	Parity Error Indicates that the received parity is different from the expected value.	0x0
1	RC	OE	Overrun Error Indicates that when a receive overrun occurs. This happens if a character is received before the previous character has been read by firmware.	0x0
0	RC	DR	Data Ready Indicates that character is received, and has been transferred to the receive buffer register. This bit is reset when all the characters are read from the receive buffer register.	0x0

NOTE:

0: False

1: True

54. MSR: Modem Status Register (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RC	DCD	Data Carrier Detect Indicates the DCDN (Data Carrier Detect) pin is at a low value.	0x0
6	RC	RI	Ring Indicator Indicates the RIN (Ring Indicator) pin is at a low value.	0x0
5	RC	DSR	Data Set Ready Indicates the DSRN (Data Set Ready) pin is at a low value.	0x0
4	RC	CTS	Clear to Send Indicates the CTSN (Clear to Send) pin is at a low value.	0x0
3	RC	DDCD	Delta Data Carrier Detect Indicates when the DCDN (Data Carrier Detect) pin changes.	0x0

Bits	Type	Name	Description	Initial Value
2	RC	TERI	Trailing Edge Ring Indicator Indicates when the RIN (Ring Indicator) pin changes from a low to a high value.	0x0
1	RC	DDSR	Delta Data Set Ready Indicates when the DSRN (Data Set Ready) pin changes.	0x0
0	RC	DCTS	Delta Clear to Send Indicates when the CTSN (Clear to Send) pin changes.	0x0

NOTE:

0: False

1: True

55. SCRATCH: Scratch Register (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	SCRATCH	Scratch This register is defined as a scratch register in 16550 application. It has no hardware function, and is retained for compatibility only.	0x0

56. DL: Clock Divider Divisor Latch (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	DL	Divisor Latch This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as: baud rate = 40 MHz / (CLKDIV * 16).	0x1

NOTE:

1. In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.

2. DL[15:0] should be >= 4.

SRC Clock Freq.	Req. Baud Rate (Bd)	DL [15:0]	Err Rate (%)
40 MHz	57000	44	-0.32%
	115200	22	-1.36%
	230400	11	-1.36%
	345600	7	3.34%
	460800	5	8.51%

57. DLLO: Clock Divider Divisor Latch Low (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	DLLO	This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	0x1

58. DLHI: Clock Divider Divisor Latch High (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	DLHI	This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	0x0

2.7 UART Lite

2.7.1 Features

- 2-pin UART
- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

2.7.2 Block Diagram

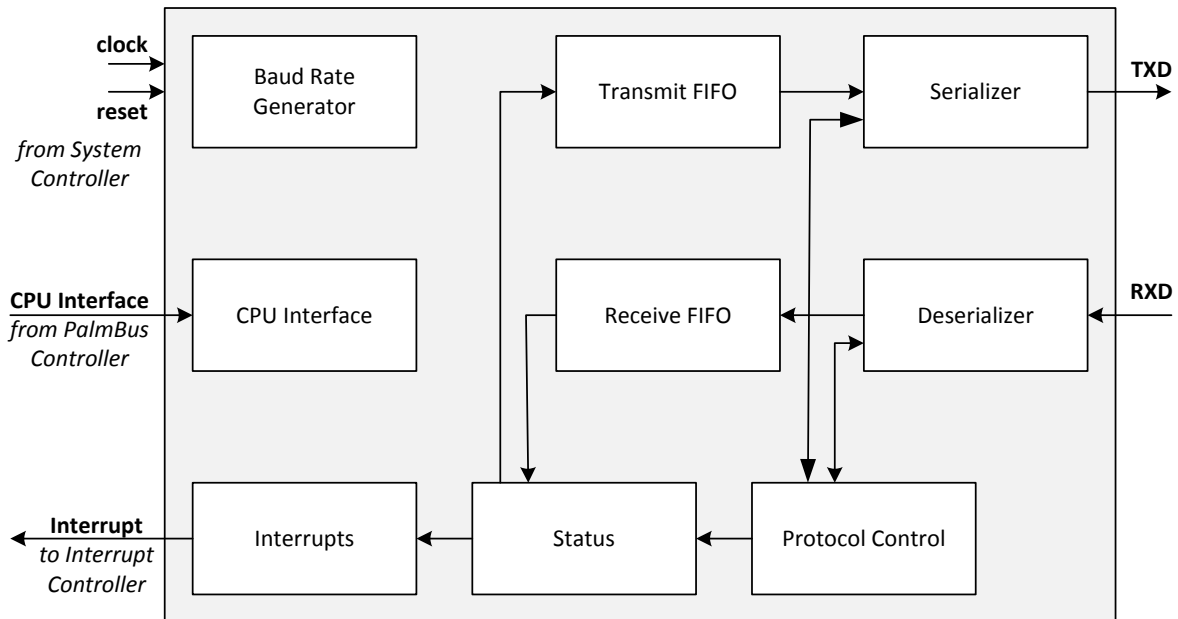


Figure 2-5 UART Lite Block Diagram

2.7.3 List of Registers

No.	Offset	Register Name	Description	Page
59	0x0000	RBR	Receive Buffer Register	74
60	0x0004	TBR	Transmit Buffer Register	74
61	0x0008	IER	Interrupt Enable Register	74
62	0x000C	IIR	Interrupt Identification Register	75
63	0x0010	FCR	FIFO Control Register	76
64	0x0014	LCR	Line Control Register	76
65	0x0018	MCR	Modem Control Register	77
66	0x001C	LSR	Line Status Register	78
67	0x0028	DL	Clock Divider Divisor Latch	79
68	0x002C	DLLO	Clock Divider Divisor Latch Low	79
69	0x0030	DLHI	Clock Divider Divisor Latch High	80
70	0x0034	IFCTL	Interface Control	80

2.7.4 Register Descriptions (base: 0x1000_0C00)

59. RBR: Receive Buffer Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RO	RXD	Receive Buffer Data Data is transferred to this register from the Rx shift register after a full character is received. The OE bit in the LSR register is set if the contents of this register have not been read before another character is received, indicating an Rx buffer overrun.	0x0

60. TBR: Transmit Buffer Register (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RO	TXD	Transmit Buffer Data When a character is written to this register, it is stored in the Tx holding register; if the Tx register is empty, the character is moved to the Tx register, starting transmission.	0x0

61. IER: Interrupt Enable Register (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:3	-	-	Reserved	0x0
2	RW	ELSI	Enable Line Status Interrupts Enables the following Rx line status interrupts. ▪ Overrun Error (OE) ▪ Parity Error (PE) ▪ Framing Error (FE) ▪ Break Interrupt (BI)	0x0
1	RW	ETBEI	Enable Tx Buffer Empty Interrupt Enables the Tx buffer empty interrupt (THRE), which indicates the Tx buffer is empty.	0x0
0	RW	ERBFI	Enable Rx Buffer Full Interrupt Enables the Rx buffer full interrupt, as well as the Data Ready (DR) and Character Time-Out interrupts.	0x0

NOTE:

0: Disable

1: Enable

62. IIR: Interrupt Identification Register (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:6	RO	FIFOENA	FIFOs Enabled These bits reflect the FIFO enable bit setting in the FIFO Control Register. 00: FIFO enable bit is cleared. 11: FIFO enable bit is set.	0x0
5:4	-	-	Reserved	0x0
3:1	RO	INTID	Interrupt Identifier These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. See NOTE below.	0x0
0	RO	INTPEND	Interrupt Pending 0: An interrupt bit is set and is not masked. 1: No interrupts are pending.	0x1

NOTE:

The interrupt encoding is given below.

Table 2-1 UART Lite Interrupt Priorities

ID	Priority	Type	Source
7		Undefined	
6		Undefined	
5		Undefined	
4		Undefined	
3	1 (highest)	Receiver Line Status	OE, PE, FE, BI
2	2	Receiver Buffer Full	DR
1	3	Transmit Buffer Empty	THRE
0		Undefined	

If more than one category of interrupt is asserted, only the highest priority ID is given.

The line and modem status interrupts are cleared by reading the corresponding status register (LSR (0x001C)).

The receiver buffer full interrupt is cleared when all of the data is read from the receive buffer. The transmitter buffer empty is cleared when data is written to the TBR register (0x0004).

63. FCR: FIFO Control Register (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:6	RW	RXTRIG	Rx Trigger Level Sets the number of characters contained by the receive buffer which triggers the data ready (DR) interrupt. 0: 1 character 1: 4 characters 2: 8 characters 3: 14 characters NOTE: This register is not used if the Rx FIFO is disabled.	0x0
5:4	RW	TXTRIG	Tx Trigger Level Sets the number of characters contained by the transmit buffer which will trigger the threshold empty (THRE) interrupt. 0: 1 character 1: 4 characters 2: 8 characters 3: 12 characters	0x0
3	RW	DMAMODE	DMA Mode Enables DMA transfers This bit is writeable and readable, but has no other hardware function.	0x0
2	WO	TXRST	Tx Reset 1: Clears the transmit FIFO and resets its status. The shift register is not cleared.	0x0
1	WO	RXRST	Rx Reset 1: Clears the receive FIFO and resets its status. The shift register is not cleared.	0x0
0	RW	FIFOENA	FIFO Enable Enables Tx and Rx FIFOs. When disabled, the FIFOs have an effective depth of one character. 0: Disable 1: Enable NOTE: The FIFO status and data are automatically cleared when this bit is changed.	0x0

64. LCR: Line Control Register (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RW	DLAB	Divisor Latch Access Bit This bit has no functionality, and is retained for compatibility only.	0x0

Bits	Type	Name	Description	Initial Value
6	RW	SETBRK	Set Break Condition 0: Normal functionality. 1: Force TXD pin to 0. Tx otherwise operates normally.	0x0
5	RW	FORCEPAR	Force Parity Bit 0: Normal functionality. 1: If even parity is selected, the (transmitted and checked) parity is forced to 0. If odd parity is selected, the (transmitted and checked) parity if forced to 1.	0x0
4	RW	EPS	Even Parity Select 0: Odd parity selected (checksum, including parity is 1). 1: Even parity selected (checksum, including parity is 0). NOTE: This bit is ignored if the PEN bit is 0.	0x0
3	RW	PEN	Parity Enable 0: Parity is not transmitted or checked. 1: Parity is generated (transmit), and checked (receive).	0x0
2	RW	STB	Stop Bit Select 0: 1 Stop Bit is transmitted and received. 1: 1.5 Stop Bits are transmitted and received if WLS is 0; 2 Stop Bits are transmitted and received if WLS is 1, 2, or 3.	0x0
1:0	RW	WLS	Word Length Select Selects the character length. 0: Each character is 5 bits in length 1: Each character is 6 bits in length 2: Each character is 7 bits in length 3: Each character is 8 bits in length	0x0

65. MCR: Modem Control Register (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:5	-	-	Reserved	0x0
4	RW	LOOP	Loopback Mode Enable 0: Normal Operation. 1: The UART is put into loop-back mode, used for self-testing: The TXD pin is driven high; the TXD signal are connected to RXD internally.	0x0
3:0	RO	-	Reserved	0x0

66. LSR: Line Status Register (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RC	ERINFIFO	Error in FIFO Indicates that a FIFO contains data which was received with a parity error, framing error, or break condition.	0x0
6	RC	TEMT	Transmit Shift Register Empty Indicates that the transmit shift register is empty. This bit is reset when data is written to the transmit buffer register (TBR).	0x1
5	RC	THRE	Transmit Holding Register Empty Indicates that the transmitter holding register is empty. This bit resets when data is written to the Tx buffer register (TBR).	0x1
4	RC	BI	Break Interrupt Indicates that a break is received, that is, when the RXD signal is at a low state for more than one character transmission time (from Start Bit to Stop Bit). Under this condition, a single 0 is received.	0x1
3	RC	FE	Framing Error Indicates that a valid Stop Bit is not detected. If a framing error occurs, the receive buffer will attempt to re-synchronize by sampling the Start Bit twice and then receiving the data.	0x0
2	RC	PE	Parity Error Indicates that the received parity is different from the expected value.	0x0
1	RC	OE	Overrun Error Indicates that when a receive overrun occurs. This happens if a character is received before the previous character has been read by firmware.	0x0
0	RC	DR	Data Ready Indicates that a character is received, and has been transferred to the receive buffer register. The bit is reset when all the characters are read from the receive buffer register.	0x0

NOTE:

0: False

1: True

67. DL: Clock Divider Divisor Latch (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	DL	Divisor Latch This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as: Baud rate = system clock frequency / (CLKDIV * 16). See NOTE below.	0x1

NOTE:

1. In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.
2. DL[15:0] should be ≥ 4 .

SRC Clock Freq.	Req. Baud Rate (Bd)	DL [15:0]	Error Rate (%)
40 MHz	57 000	44	-0.32%
	115 200	22	-1.36%
	230 400	11	-1.36%
	345 600	7	3.34%
	460 800	5	8.51%

68. DLLO: Clock Divider Divisor Latch Low (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	DLLO	Divisor Latch Low This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	0x1

69. DLHI: Clock Divider Divisor Latch High (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	DLHI	Divisor Latch High This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility. NOTE: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.	0x0

70. IFCTL: Interface Control (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	0x0
0	RW	IFCTL	Open Collector Mode Control This register controls if the UART Lite TXD output functions in open collector mode or is always driven. 0: The output is always driven with the value of the transmit data signal. 1: The TXD output functions in open collector mode, where the TXD output is either driven low (when the transmit data output is active low) or tri-stated (when the transmit data output is active high).	0x0

2.8 Programmable I/O

2.8.1 Features

- Supports 73 programmable I/Os
- Parameterized numbers of independent inputs, outputs, and inputs
- Independent polarity controls for each pin
- Independently masked edge detect interrupt on any input transition
- Programmable I/O pins are shared with MDIO, JTAG, UART-Lite, UART, SPI, PCM, I2C, GE1, and EPHY_LED.

2.8.2 Block Diagram

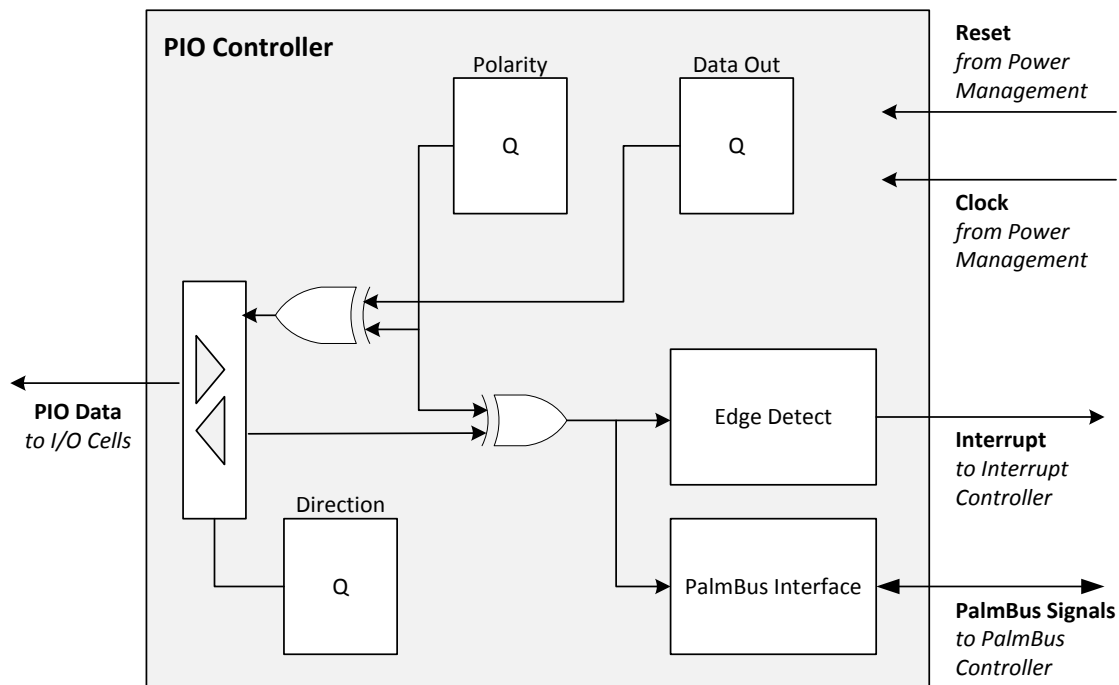


Figure 2-6 Programmable I/O Block Diagram

2.8.3 List of Registers

No.	Offset	Register Name	Description	Page
71	0x0000	GPIO23_00_INT	PIO Pin Ports 23 to 00 Interrupt Status	84
72	0x0004	GPIO23_00_EDGE	PIO Pin Ports 23 to 00 Edge Status	84
73	0x0008	GPIO23_00_RMASK	PIO Pin Ports 23 to 00 Rising Edge Interrupt Mask	85
74	0x000C	GPIO23_00_MASK	PIO Pin Ports 23 to 00 Falling Edge Interrupt Mask	85
75	0x0020	GPIO23_00_DATA	PIO Pin Ports 23 to 00 Data	85
76	0x0024	GPIO23_00_DIR	PIO Pin Ports 23 to 00 Data Direction	86
77	0x0028	GPIO23_00_POL	PIO Pin Ports 23 to 00 Data Polarity	86
78	0x002C	GPIO23_00_SET	PIO Pin Ports 23 to 00 Set Data Bit	86
79	0x0030	GPIO23_00_RESET	PIO Pin Ports 23 to 00 Clear Data Bit	86
80	0x0034	GPIO23_00_TOG	PIO Pin Ports 23 to 00 Toggle PIO Data Bit	86
81	0x0038	GPIO39_24_INT	PIO Pin Ports 39 to 24 Pin Interrupt Status	87
82	0x003C	GPIO39_24_EDGE	PIO Pin Ports 39 to 24 Pin Edge Status	87
83	0x0040	GPIO39_24_RMASK	PIO Pin Ports 39 to 24 Rising Edge Interrupt Mask	88
84	0x0044	GPIO39_24_FMASK	PIO Pin Ports 39 to 24 Falling Edge Interrupt Mask	88
85	0x0048	GPIO39_24_DATA	PIO Pin Ports 39 to 24 Data	89
86	0x004C	GPIO39_24_DIR	PIO Pin Ports 39 to 24 Data Direction	89
87	0x0050	GPIO39_24_POL	PIO Pin Ports 39 to 24 Data Polarity	89
88	0x0054	GPIO39_24_SET	PIO Pin Ports 39 to 24 Set Data Bit	90
89	0x0058	GPIO39_24_RESET	PIO Pin Ports 39 to 24 Clear Data Bit	90
90	0x005C	GPIO39_24_TOG	PIO Pin Ports 39 to 24 Toggle Data Bit	90
91	0x0060	GPIO71_40_INT	PIO Pin Ports 71 to 40 Interrupt Status	90
92	0x0064	GPIO71_40_EDGE	PIO Pin Ports 71 to 40 Edge Status	91
93	0x0068	GPIO71_40_RMASK	PIO Pin Ports 71 to 40 Rising Edge Interrupt Mask	91
94	0x006C	GPIO71_40_FMASK	PIO Pin Ports 71 to 40 Falling Edge Interrupt Mask	91
95	0x0070	GPIO71_40_DATA	PIO Pin Ports 71 to 40 Data	92
96	0x0074	GPIO71_40_DIR	PIO Pin Ports 71 to 40 Data Direction	92
97	0x0078	GPIO71_40_POL	PIO Pin Ports 71 to 40 Data Polarity	92
98	0x007C	GPIO71_40_SET	PIO Pin Ports 71 to 40 Set Data Bit	93
99	0x0080	GPIO71_40_RESET	PIO Pin Ports 71 to 40 Clear Data Bit	93
100	0x0084	GPIO71_40_TOG	PIO Ports 71 to 40 Toggle Data Bit	93
101	0x0088	GPIO72_INT	PIO Pin Port 72 Interrupt Status	93
102	0x008C	GPIO72_EDGE	PIO Pin Port 72 Edge Status	93
103	0x0090	GPIO72_RMASK	PIO Pin Port 72 Rising Edge Interrupt Mask	94
104	0x0094	GPIO72_FMASK	PIO Pin Port 72 Falling Edge Interrupt Mask	94
105	0x0098	GPIO72_DATA	PIO Pin Port 72 Data	95
106	0x009C	GPIO72_DIR	PIO Pin Port 72 Data Direction	95
107	0x00A0	GPIO72_POL	PIO Pin Port 72 Data Polarity	95
108	0x00A4	GPIO72_SET	PIO Pin Port 72 Set Data Bit	96

109	0x00A8	GPIO72_RESET	PIO Pin Port 72 Clear Data Bit	96
110	0x00AC	GPIO72_TOG	PIO Pin Port 72 Toggle Data Bit	96

2.8.4 Register Descriptions (base: 0x1000_0600)

71. GPIO23_00_INT: PIO Pin Interrupt Status (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	RC	PIOINT	PIO Pin Interrupt A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMASK or PIOFMASK register. The pin must be set as an input in the PIODIR register to generate an interrupt. <i>Read</i> 0: No change detected. 1: Change detected. <i>Write</i> All bits are cleared by writing 1 to either this register or the PIOEDGE register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

72. GPIO23_00_EDGE: PIO Pin Edge Status (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	RC	PIOEDGE	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMASK or PIOFMASK register. <i>Read</i> If the PIO PIN Interrupt for this PIO pin is asserted, the corresponding PIOEDGE bit indicates whether a falling or rising edge triggered the interrupt. 0: Interrupt triggered by falling edge. 1: Interrupt triggered by rising edge. If the interrupt is masked (disabled), the PIOEDGE bit is set on either a rising or falling edge and remains set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. <i>Write</i> All bits are cleared by writing 1 to either this register or the PIOINT register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

73. GPIO23_00_RMASK: PIO Pin Rising Edge Interrupt Mask (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	RW	PIORMASK	PIO Pin Rising Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 0 to a 1, i.e. a rising edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

74. GPIO23_00_MASK: PIO Pin Falling Edge Interrupt Mask (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	RW	PIOFMASK	PIO Pin Falling Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 1 to a 0, i.e. a falling edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

75. GPIO23_00_DATA: PIO Pin Data (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	RW	PIODATA	PIO Pin Data These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. NOTE: - The value of any bit in this register is inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. - The values read from the PIO pins are not synchronized; the user should be sure that the data will not change when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	PC

76. GPIO23_00_DIR: PIO Pin Direction (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	RW	PIODIR	PIO Pin Direction Sets the data direction on PIO pins corresponding to bits in this register. 0: Set data direction to input. 1: Set data direction to output. The values driven onto the PIO pins are controlled by the PIOPOL and PIODATA registers.	0x0

77. GPIO23_00_POL: PIO Pin Polarity (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	RW	PIOPOL	PIO Pin Polarity Sets the polarity of data on PIO pins corresponding to bits in this register. 0: Maintain original polarity 1: Invert existing polarity NOTE: The polarity controls affect both input and output modes.	0x0

78. GPIO23_00_SET: Set PIO Pin Data Bit (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	W	PIOSET	PIO Pin Set Sets the corresponding bit in the PIODATA output register. 0: No effect. 1: Set the selected PIODATA bit.	0x0

79. GPIO23_00_RESET: Clear PIO Pin Data Bit (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23:0	W	PIORESET	PIO Pin Reset Clears the corresponding bit in the PIODATA output register. 0: No effect. 1: Clear the selected PIODATA bit.	0x0

80. GPIO23_00_TOG: Toggle PIO Pin Data Bit (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
23:0	W	PIOTOG	PIO Pin Toggle Toggles the corresponding bit in the PIODATA output register. 0: No effect. 1: Invert the selected PIODATA bit.	0x0

81. GPIO39_24_INT: PIO Pin Interrupt (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RC	PIOINT	PIO Interrupt A PIOINT bit is set when its corresponding PIO pin changes Value and the edge for that pin is enabled via the PIORMASK or PIOFMASK register. The pin must be set as an input in the PIODIR register to generate an interrupt. <i>Read</i> 0: No change detected. 1: Change detected. <i>Write</i> All bits are cleared by writing 1 to either this register or the PIOEDGE register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

82. GPIO39_24_EDGE: PIO Pin Edge Status (offset: 0x003C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
15:0	RC	PIOEDGE	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMASK or PIOFMASK register. <i>Read</i> If the PIO Pin Interrupt for this PIO pin is asserted, the corresponding PIOEDGE bit indicates whether a falling or rising edge triggered the interrupt. 0: Interrupt triggered by falling edge. 1: Interrupt triggered by rising edge. If the interrupt is masked (disabled), the PIOEDGE bit is set on either a rising or falling edge and remains set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. <i>Write</i> All bits are cleared by writing 1 to either this register or the PPOINT register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

83. GPIO39_24_RMASK: PIO Pin Rising Edge Interrupt Mask (offset: 0x0040)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RW	PIORMASK	PIO Pin Rising Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 0 to a 1, i.e. a rising edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

84. GPIO39_24_FMASK: PIO Pin Falling Edge Interrupt Mask (offset: 0x0044)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RW	PIOFMASK	PIO Pin Falling Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 1 to a 0, i.e. a falling edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

85. GPIO39_24_DATA: PIO Pin Data (offset: 0x0048)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RW	PIODATA	PIO Pin Data These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. NOTE: 1. The value of any bit in this register is inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. 2. The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	PC

86. GPIO39_24_DIR: Program I/O Direction (offset: 0x004C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RW	PIODIR	PIO Pin Direction Sets the data direction on PIO pins corresponding to bits in this register. 0: Set data direction to input. 1: Set data direction to output. The values driven onto the PIO pins are controlled by the PIOPOL and PIODATA registers.	0x0

87. GPIO39_24_POL: PIO Pin Polarity (offset: 0x0050)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RW	PIOPOL	PIO Pin Polarity Sets the polarity of data on PIO pins corresponding to bits in this register. 0: Maintain original polarity 1: Invert existing polarity NOTE: The polarity controls affect both input and output modes.	0x0

88. GPIO39_24_SET: Set PIO Pin Data Bit (offset: 0x0054)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RC	PIOSET	PIO Pin Set Sets the corresponding bit in the PIODATA output register. 0: No effect. 1: Set the selected PIODATA bit.	0x0

89. GPIO39_24_RESET: Clear PIO Pin Data Bit (offset: 0x0058)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RC	PIORESET	PIO Pin Reset Clears the corresponding bit in the PIODATA output register. 0: No effect. 1: Clear the selected PIODATA bit.	0x0

90. GPIO39_24_TOG: Toggle PIO Pin Data Bit (offset: 0x005C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15:0	RC	PIOTOG	PIO Pin Toggle Toggles the corresponding bit in the PIODATA output register. 0: No effect. 1: Invert the selected PIODATA bit.	0x0

91. GPIO71_40_INT: PIO Pin Interrupt Status (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
31:0	RC	PIOINT	PIO Pin Interrupt A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMASK or PIOFMASK register. The pin must be set as an input in the PIODIR register to generate an interrupt. <i>Read</i> 0: No change detected. 1: Change detected. <i>Write</i> All bits are cleared by writing 1 to either this register or the PIOEDGE register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

92. GPIO71_40_EDGE: PIO Pin Edge Status (offset: 0x0064)

Bits	Type	Name	Description	Initial Value
31:0	RC	PIOEDGE	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMASK or PIOFMASK register. <i>Read</i> If the PIO PIN Interrupt for this PIO pin is asserted, the corresponding PIOEDGE bit indicates whether a falling or rising edge triggered the interrupt. 0: Interrupt triggered by falling edge. 1: Interrupt triggered by rising edge. If the interrupt is masked (disabled), the PIOEDGE bit is set on either a rising or falling edge and remains set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. <i>Write</i> All bits are cleared by writing 1 to either this register or the PIOINT register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

93. GPIO71_40_RMASK: PIO Pin Rising Edge Interrupt Mask (offset: 0x0068)

Bits	Type	Name	Description	Initial Value
31:0	RW	PIORMASK	PIO Pin Rising Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 0 to a 1, i.e. a rising edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

94. GPIO71_40_FMASK: PIO Pin Falling Edge Interrupt Mask (offset: 0x006C)

Bits	Type	Name	Description	Initial Value
31:0	RW	PIOFMASK	PIO Pin Falling Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 1 to a 0, i.e. a falling edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

95. GPIO71_40_DATA: PIO Pin Data (offset: 0x0070)

Bits	Type	Name	Description	Initial Value
31:0	RW	PIODATA	PIO Pin Data These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. NOTE: 1. The value of any bit in this register is inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. 2. The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	PC

96. GPIO71_40_DIR: PIO Pin Direction (offset: 0x0074)

Bits	Type	Name	Description	Initial Value
31:0	RW	PIODIR	PIO Pin Direction Sets the data direction on PIO pins corresponding to bits in this register. 0: Set the data direction on this pin to input. 1: Set the data direction on this pin to output. The values driven onto the PIO pins are controlled by the PIOPOL and PIODATA registers.	0x0

97. GPIO71_40_POL: PIO Pin Polarity (offset: 0x0078)

Bits	Type	Name	Description	Initial Value
31:0	RW	PIOPOL	PIO Pin Polarity Sets the polarity of data on PIO pins corresponding to bits in this register. 0: Maintain original polarity 1: Invert existing polarity NOTE: The polarity controls affect both input and output modes.	0x0

98. GPIO71_40_SET: Set PIO Pin Data Bit (offset: 0x007C)

Bits	Type	Name	Description	Initial Value
31:0	RC	PIOSET	PIO Pin Set Sets the corresponding bit in the PIODATA output register. 0: No effect. 1: Set the selected PIODATA bit.	0x0

99. GPIO71_40_RESET: Clear PIO Pin Data bit (offset: 0x0080)

Bits	Type	Name	Description	Initial Value
31:0	RC	PIORESET	PIO Pin Reset Clears the corresponding bit in the PIODATA output register. 0: No effect. 1: Clear the selected PIODATA bit.	0x0

100. GPIO71_40_TOG: Toggle PIO Pin Data bit (offset: 0x0084)

Bits	Type	Name	Description	Initial Value
31:0	RC	PIOTOG	PIO Pin Toggle Toggles the corresponding bit in the PIODATA output register. 0: No effect. 1: Invert the selected PIODATA bit.	0x0

101. GPIO72_INT: PIO Pin Interrupt Status (offset: 0x0088)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	RC	PIOINT	PIO Pin Interrupt A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMASK or PIOFMASK register. The pin must be set as an input in the PIODIR register to generate an interrupt. <i>Read</i> 0: No change detected. 1: Change detected. <i>Write</i> All bits are cleared by writing 1 to either this register or the PIOEDGE register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

102. GPIO72_EDGE: PIO Pin Edge Status (offset: 0x008C)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
0	RC	PIOEDGE	The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMASK or PIOFMASK register. <i>Read</i> If the PIO PIN Interrupt for this PIO pin is asserted, the corresponding PIOEDGE bit indicates whether a falling or rising edge triggered the interrupt. 0: Interrupt triggered by falling edge. 1: Interrupt triggered by rising edge. If the interrupt is masked (disabled), the PIOEDGE bit is set on either a rising or falling edge and remains set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. <i>Write</i> All bits are cleared by writing 1 to either this register or the PPOINT register. NOTE: Changes to the PIO pins can only be detected when the clock is running.	0x0

103. GPIO72_RMASK: PIO Pin Rising Edge Interrupt Mask (offset: 0x0090)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	RW	PIORMASK	PIO Pin Rising Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 0 to a 1, i.e. a rising edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

104. GPIO72_FMASK: PIO Pin Falling Edge Interrupt Mask (offset: 0x0094)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	RW	PIOFMASK	PIO Pin Falling Edge Interrupt Mask Masks the PIO interrupt indicating when data on the corresponding PIO pin transitions from a 1 to a 0, i.e. a falling edge. 0: No mask 1: Mask NOTE: Edge detection is done after the polarity is adjusted according to the PIOPOL register.	0x0

105. GPIO72_DATA: PIO Pin Data (offset: 0x0098)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	RW	PIODATA	PIO Pin Data These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins. NOTE: 1. The value of any bit in this register is inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes. 2. The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.	PC

106. GPIO72_DIR: PIO Pin Direction (offset: 0x009C)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	RW	PIODIR	PIO Pin Direction Sets the data direction on PIO pins corresponding to bits in this register. 0: Set the data direction on this pin to input. 1: Set the data direction on this pin to output. The values driven onto the PIO pins are controlled by the PIOPOL and PIODATA registers.	0x0

107. GPIO72_POL: PIO Pin Polarity (offset: 0x00A0)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	RW	PIOPOL	PIO Pin Polarity Sets the polarity of data on PIO pins corresponding to bits in this register. 0: Maintain original polarity 1: Invert existing polarity NOTE: The polarity controls affect both input and output modes.	0x0

108. GPIO72_SET: Set PIO Pin Data Bit (offset: 0x00A4)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	W	PIOSET	PIO Pin Set Sets the corresponding bit in the PIODATA output register. 0: No effect. 1: Set the selected PIODATA bit.	0x0

109. GPIO72_RESET: Clear PIO Pin Data Bit (offset: 0x00A8)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	W	PIORESET	PIO Pin Reset Clears the corresponding bit in the PIODATA output register. 0: No effect. 1: Clear the selected PIODATA bit.	0x0

110. GPIO72_TOG: Toggle PIO Pin Data Bit (offset: 0x00AC)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	W	PIOTOG	PIO Pin Toggle Toggles the corresponding bit in the PIODATA output register. 0: No effect. 1: Invert the selected PIODATA bit.	0x0

2.9 I²C Controller

2.9.1 Features

- Programmable I²C bus clock rate
- Supports the Synchronous Inter-Integrated Circuits (I²C) serial protocol
- Bi-directional data transfer
- Programmable address width up to 8 bits
- Sequential byte read or write capability
- Device address and data address can be transmitted for device, page and address selection
- Supports Standard mode and Fast mode

2.9.2 Block Diagram

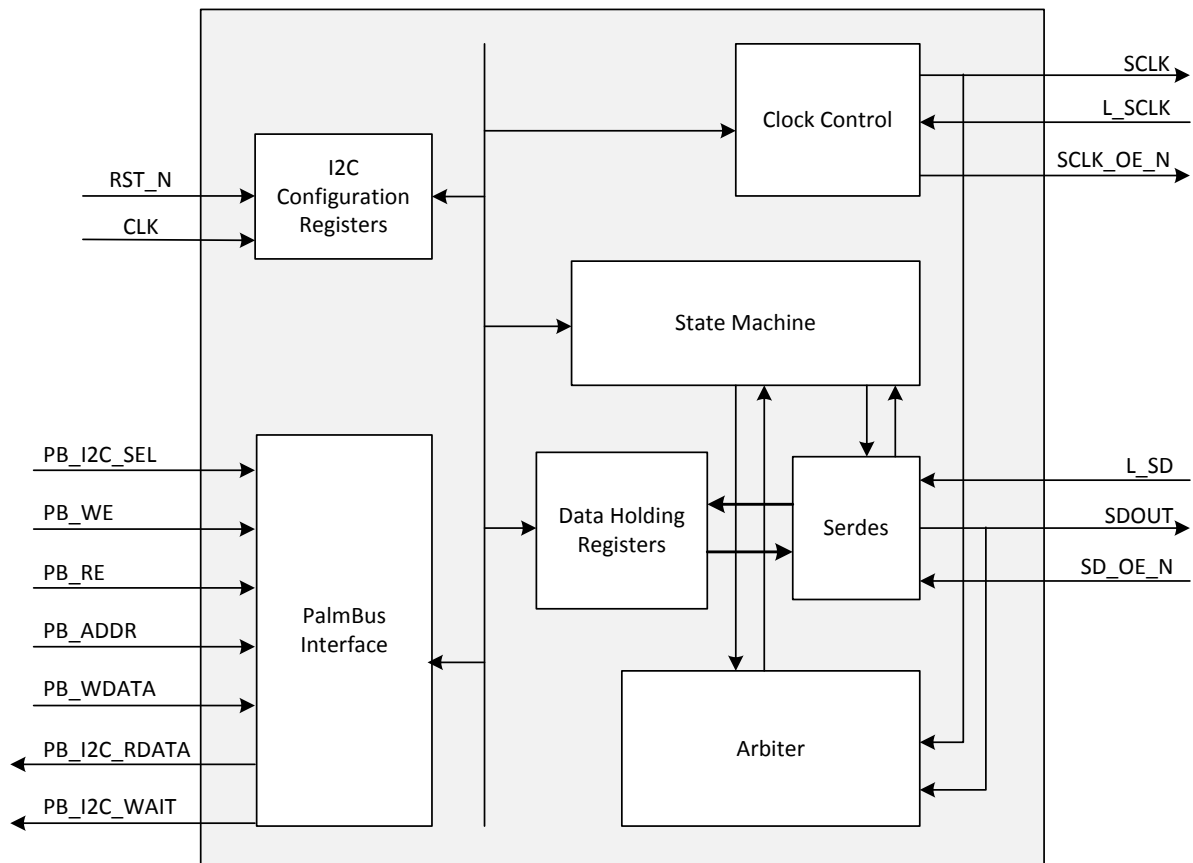


Figure 2-7 I2C Controller Block Diagram

2.9.3 List of Registers

No.	Offset	Register Name	Description	Page
111	0x0000	CONFIG	I ² C Configuration	99
112	0x0004	CLKDIV	I ² C Clock Divisor	99
113	0x0008	DEVADDR	I ² C Device Address	100
114	0x000C	ADDR	I ² C Address	100
115	0x0010	DATAOUT	I ² C Data Out	100
116	0x0014	DATAIN	I ² C Data In	101
117	0x0018	STATUS	I ² C Status	101
118	0x001C	STARTXFR	I ² C Transfer Start	102
119	0x0020	BYTECNT	I ² C Byte Counter	102

2.9.4 Register Descriptions (base: 0x1000_0900)

111. CONFIG: I²C Configuration Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	-
7:5	RW	ADDRLEN	Address Length The value written to this register plus one indicates the number of address bits to be transferred from the I2C ADDR register. 0: Transfers a 1-bit address 1: Transfers a 2-bit address, etc.	0x0
4:2	RW	DEVADLEN	Device Address Length The value written to this register plus one indicates the number of device address bits to be transferred from the DEVADDR register. This field should be programmed to 6 for compliance with I2C bus protocol.	0x0
1	RW	ADDRDIS	Address Disable Selects whether the address is included in transmission. 0: Normal transfers occur with the address included in the transfer, followed by read or write data. 1: The controller reads or writes serial data without transferring the address.	0x0
0	RW	DEVADDIS	Device Address Disable 0: The device address is transmitted before the data address. 1: The controller does not transfer the device address. NOTE: 1. If this bit is set, the ADDRDIS bit is ignored, and an address is always transmitted. 2. Most I ² C slave devices require a device address to be transmitted; this bit should typically be set to 0.	0x0

112. CLKDIV: I²C Clock Divisor Register (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
15:0	RW	CLKDIV	Clock Divisor The value written to this register is used to generate the I2C bus SCLK signal by applying the following equation: $\text{SCLK frequency} = 40 \text{ MHz} / (2 \times \text{CLKDIV})$ NOTE: 1. Only values of 8 and above are valid. 2. Due to synchronization between the I²C internal clock and the system clock, the exact equation is actually $\text{SCLK frequency} = \text{PB_CLK frequency} / ((2 \times \text{CLKDIV}) + 5).$ For most systems, CLKDIV is usually programmed to very larger numbers since the system clock frequency should be orders of magnitude faster than the I2C bus clock. These results in the synchronization errors being insignificant and the exact equation approximating the simpler one given above.	0x0

113. DEVADDR: I²C Device Address Register (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:7	-	-	Reserved	0x0
6:0	RW	DEVADDR	I²C Device Address This value is transmitted as the device address, if DEVADDIS bit in the CONFIG register is not set to 1.	0x0

114. ADDR: I²C Address Register (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	ADDR	I²C Address These bits store the 8-bits of address to be sent to the external I2C slave devices when the ADDRDIS bit is 0.	0x0

115. DATAOUT: I²C Data Out Register (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	DATAOU	I²C Data Out These bits store the 8-bits of data to be written to the external I2C slave devices during a write transfer.	0x0

116. DATAIN: I²C Data In Register (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RO	DATAIN	I ² C Data In These bits store the 8-bits of data received from the external I2C slave devices during a read transaction. The DATARDY bit in the STATUS register is set to 1 when data is valid in this register.	0x0

117. STATUS: I²C Status Register (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:5	-	-	Reserved	0x0
4	RO	STARTERR	Start Overflow Error 0: Indicates firmware is writing to the STARTXFR register when the BUSY bit is cleared. 1: Indicates an overflow error occurred. The STARTXFR register is written and a transfer is in progress. When this occurs, the write to the STARTXFR register is ignored.	0x0
3	RO	ACKERR	I ² C Acknowledge Error Detect 0: Indicates firmware is writing to the STARTXFR register. 1: Indicates the Host controller did not receive a proper acknowledge from the I2C slave device after the transmission of a device address, address, or data out.	0x0
2	RO	DATARDY	I ² C Data Ready for Read This bit indicates that the receive buffer contains valid data. 0: Indicates firmware is reading the DATAIN register. 1: Indicates data is received from an I2C slave device and is transferred from the interface shift register to the DATAIN register.	0x0
1	RO	SDOEMPTY	I ² C Serial Data Out Register Empty This bit indicates that the transmit data buffer is empty. 0: Indicates the DATAOUT register is being written to by software. 1: Indicates when transmit data is transferred from the DATAOUT register to the interface shift register. Firmware may write to the DATAOUT register when this bit is 1.	0x1

Bits	Type	Name	Description	Initial Value
0	RO	BUSY	I ² C State Machine Busy 0: The I2C interface is idle. Firmware may initiate an I2C transfer. 1: Indicates the I2C interface is active, and firmware should not modify any I2C host controller.	0x0

118. STARTXFR: I²C Transfer Start Register (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:2	-	-	Reserved	0x0
1	RW	NODATA	No Data Transfer Initiate transfers without transferring data. When this register is written with this bit set, an address-only transaction is initiated. If DEVADDIS is 0, the device address, direction, address and stop condition are transmitted to the I2C slave device. If DEVADDIS is 1, the address and stop condition are transmitted to the I2C slave device. This bit should be written with a 0 for normal I2C bus accesses. NOTE: ADDRDIS is ignored if this bit is set for a transaction.	0x0
0	RW	RWDIR	Read/Write Direction When this register is written with this bit set, a read transaction is initiated; when written with this bit reset, a write transaction is initiated. NOTE: This bit is shifted out to the I2C slave device after the device address; if DEVADDIS is 1, this bit is not shifted out to the device.	0x0

119. BYTECNT: I²C Byte Counter Register (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:6	-	-	Reserved	0x0
5:0	RW	BYTCNT	Byte Count Used for sequential reads/writes. The value written to this register plus one indicates the number of data bytes to be written to or read from the external I2C slave device. If its value is non-zero, multiple sequential read or write cycles will be issued with a single address (and/or device address).	0x0

2.9.4.1 I²C Programming Description

Write Operation: (Single)

S	DEV_ADR	A(S)	SUB_ADR	A(S)	DATA	A(S)	P
---	---------	------	---------	------	------	------	---

S	DEV_ADR	A(S)	SUB_ADR	A(S)	DATA	A(M)	P
---	---------	------	---------	------	------	------	---

NOTE:

The bit-width of DEV_ADR is defined in REG(CONFIG) bit[7:5]

The bit-width of SUB_ADR is defined in REG(CONFIG) bit[4:2]

NOTE: As REG(CONFIG) bit[1]=1'b1, the SUB_ADR field will be absent.
(the waveform will be shown as below.)

S	DEV_ADR	A(S)	DATA	A(S)	P
---	---------	------	------	------	---

NOTE: As REG(CONFIG) bit[0]=1'b1, the DEV_ADR field will be absent.
(the waveform will be shown as below.)

S	SUB_ADR	A(S)	DATA	A(S)	P
---	---------	------	------	------	---

Sequence Write Operation:

Action-1	S	DEV_ADR	A(S)	SUB_ADR	A(S)	DATA	A(S)
----------	---	---------	------	---------	------	------	------

Action-2	RS	DEV_ADR	A(S)	DATA	A(S)	P
----------	----	---------	------	------	------	---

Action-1: SET REG(STARTXFR) bit[2]=1'b1, the "STOP" <P> field disappears.

Action-2: SET REG(STARTXFR) bit[2]=1'b0, the "STOP" <P> field appears.

S	START bit	A(S)	ACKNOWLEDGE BY DEVICE
P	STOP bit	A(M)	ACKNOWLEDGE BY HOST

Initialization:

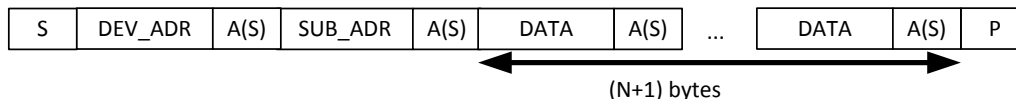
1. Configure the REG(CLKDIV) to decide the clock frequency of I2C.
2. Configure the bit width of DEV_ADDR and SUB_ADDR by configure REG(CONFIG).

Read/Write Operation:

1. Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR).
2. Write the DATAout (REG(DATAOUT)) for write operation.
3. Write the operation cfg by REG(STARTXFR) to kick off the command.
4. Read the BUSY status by REG(STATUS) to monitor if the operation is done.
5. Read back the REG(DATAIN) for read operation.

Multiple Data Transfer: (write operation.)

E.g. we want to write (n+1) beats data by I2C

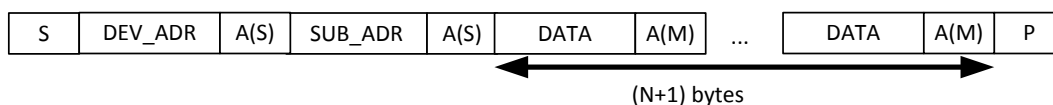


Burst Write Operation:

- 1) Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write (N) to REG(BYTECNT).
- 3) Write the REG(DATAOUT) for write operation.
- 4) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 5) Read the SDOEMPTY bit by REG(STATUS) to monitor if the data is sent.
- 6) Quit when all data is written, otherwise put the new data to the REG(DATAOUT) for write operation.
- 7) Return to step 4.

Multiple Data Transfer: (read operation.)

E.g. we want to read (n+1) beats data by I2C



Burst Read Operation:

- 1) Write the DEV_ADDR and SUB_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write (N) to REG(BYTECNT).
- 3) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 4) Read the DATARDY bit by REG(STATUS) to monitor if the data is obtained.
- 5) Read REG(DATAIN) and return to step-4 until all bytes are read.

2.10 NAND Flash Controller

2.10.1 Features

- Supports read/erase/page program NAND flash memory.
- Hardware ECC engine. (Hardware generating and software correcting)
- Supports NAND flash memory with 512-byte and 2048-byte page size.
- Indirect access for special commands.
- Configurable write protect register.
- Little / bit ending operation.

2.10.2 Normal Mode Flow

Under this mode, CPU must first configure the command register of the controller register. After configuration of the command register, the controller sends serial commands and addresses to NAND flash memory. Then a byte data is read (write) from the data buffer (NAND flash) to NAND flash (data buffer). At the same time, the CPU or GDMA is responsible for writing (reading) data into (from) the data buffer.

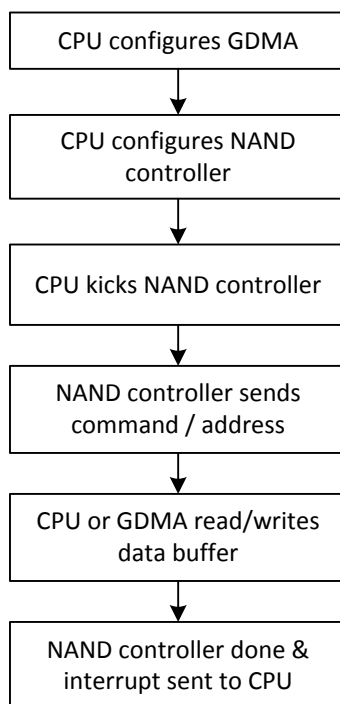


Figure 2-8 Normal Mode Flow

2.10.3 ECC

The ECC engine uses Hamming code. The Hamming code generates a 24-bit ECC per 512 bytes in order to perform a 2-bit detection and a 1-bit correction. In our application, hardware performs ECC error detection, and software performs 1-bit ECC error correction.

The following table shows how the 24-bit ECC was generated from 512-byte data.

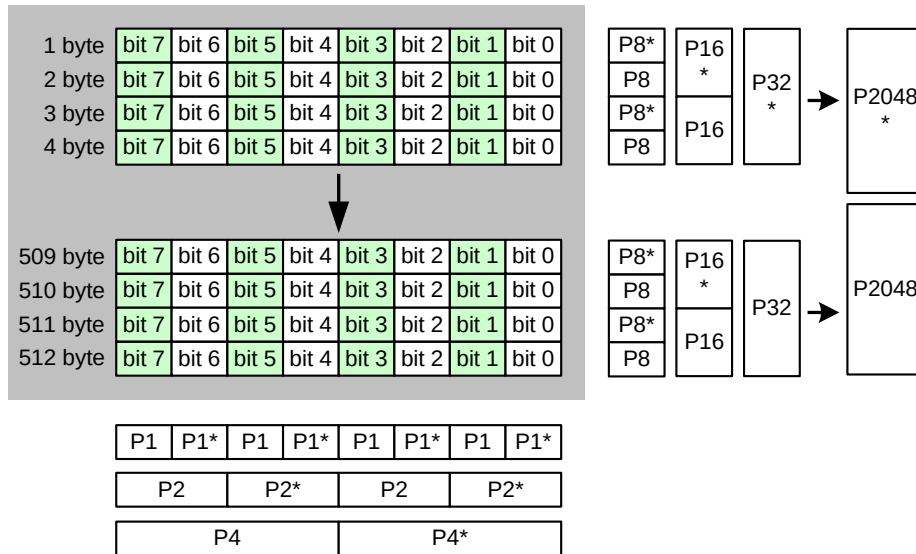


Figure 2-9 24-bit ECC Generated from 512-Byte Data

$$\begin{aligned}
 P1 &= \text{bit7} \wedge \text{bit5} \wedge \text{bit3} \wedge \text{bit1} \wedge P1 \\
 P2 &= \text{bit7} \wedge \text{bit6} \wedge \text{bit3} \wedge \text{bit2} \wedge P2 \\
 P4 &= \text{bit7} \wedge \text{bit6} \wedge \text{bit5} \wedge \text{bit4} \wedge P4 \\
 P8 &= \text{bit7} \wedge \text{bit6} \wedge \text{bit5} \wedge \text{bit4} \wedge P4 \wedge \text{bit3} \wedge \text{bit2} \wedge \text{bit1} \wedge \text{bit0} \wedge P8
 \end{aligned}$$

$$\begin{aligned}
 P1^* &= \text{bit8} \wedge \text{bit6} \wedge \text{bit4} \wedge \text{bit2} \wedge P1^* \\
 P2^* &= \text{bit5} \wedge \text{bit4} \wedge \text{bit1} \wedge \text{bit0} \wedge P2^* \\
 P4^* &= \text{bit3} \wedge \text{bit2} \wedge \text{bit1} \wedge \text{bit0} \wedge P4^* \\
 P8^* &= \text{bit7} \wedge \text{bit6} \wedge \text{bit5} \wedge \text{bit4} \wedge P4 \wedge \text{bit3} \wedge \text{bit2} \wedge \text{bit1} \wedge \text{bit0} \wedge P8^*
 \end{aligned}$$

The following table shows how the 24-bit ECC bits are arranged in three bytes. The first and second ECC bytes contains row parity bits. The third ECC byte contains six column parity bits, plus two row parity bits.

ECC	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECC 0	P64	P64*	P32	P32*	P16	P16*	P8	P8*
ECC 1	P1024	P1024*	P512	P512*	P256	P256*	P128	P128*
ECC 2	P4	P4*	P2	P2*	P1	P1*	P2048	P2048*

The figure below shows the hardware ECC detection flow chart.

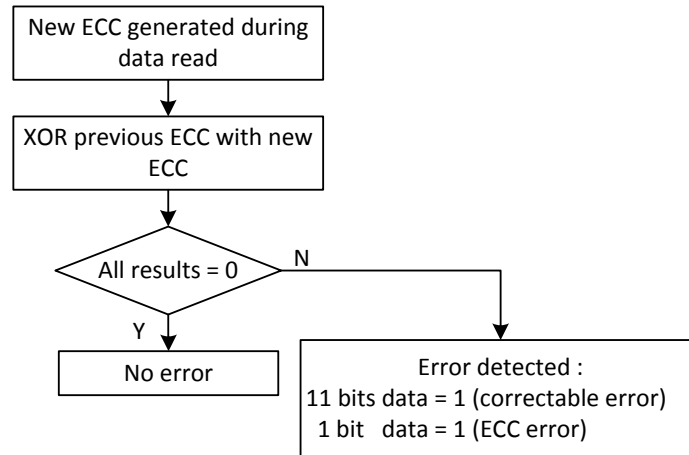


Figure 2-10 Hardware ECC Detection Flowchart

2.10.4 List of Registers

No.	Offset	Register Name	Description	Page
120	0x0010	CTRL0	Control 0	109
121	0x0014	TRANS_CFG	Transfer Configuration	109
122	0x0018	CMD1	Command 1	110
123	0x001C	CMD2	Command 2	110
124	0x0020	CMD3	Command 3	111
125	0x0024	ADDR	Address	111
126	0x0028	DATA	Data	111
127	0x0030	STATUS	ECC Status	111
128	0x0034	INT_ENA	Interrupt Enable	112
129	0x0038	INT_STA	Interrupt Status	112
130	0x003C	CTRL1	Control 1	112
131	0x0040	ECC_PAGE1	Error Correction Code Page 1	113
132	0x0044	ECC_PAGE2	Error Correction Code Page 2	113
133	0x0048	ECC_PAGE3	Error Correction Code Page 3	113
134	0x004C	ECC_PAGE4	Error Correction Code Page 4	113
135	0x0050	ECC_ERR_PAGE1	ECC Error Information Page 1	113
136	0x0054	ECC_ERR_PAGE2	ECC Error Information Page 2	114
137	0x0058	ECC_ERR_PAGE2	ECC Error Information Page 3	114
138	0x005C	ECC_ERR_PAGE3	ECC Error Information Page 4	114
139	0x0060	ADDR2	Address 2	115

2.10.5 Register Descriptions (base: 0x1000_0800)

120. CTRL0: Control 0 (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	TWAITB	Time Wait Busy Signal Dummy time period to wait for a busy signal = clock * (TWAITB + 1)	0x0
15:12	RW	THOLD	Time Hold Hold time duration = clock * (THOLD+1)	0x0
11:8	RW	TPERIOD	Time Period Period time duration = clock * (TPERIOD+1)	0x0
7:4	RW	TSETUP	Time Setup Setup time duration = clock * (TSETUP+1)	0x0
3:2	RW	BURST_SIZE	Burst Size 0: 1 DW 1: 2 DW 2: 4 DW 3: 8 DW	0x0
1	RW	DBUF_CLR	Clear Data Buffer 0: No effect 1: Clear	0x0
0	RW	WP	Write Protect Enable 0: Disable 1: Enable	0x0

121. TRANS_CFG: Transfer Configuration (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:20	RW	BNUM_DATA	Byte Number Of Data Sets the number of bytes to be transferred. (unit: bytes)	0x528
19	-	-	Reserved	0x0
18:16	RW	BNUM_ADDR	Byte Number Of Addresses Sets the number of bytes in an address. (unit: bytes) NOTE: Maximum number is 4	0x3
15:14	-	-	Reserved	0x0
13:12	RW	BNUM_CMD3	Byte Number Of Commands 3 Sets the number of bytes in a command. (unit: bytes)	0x0
11:10	RW	BNUM_CMD2	Byte Number Of Commands 2 Sets the number of bytes in a command. (unit: bytes)	0x0

Bits	Type	Name	Description	Initial Value
9:8	RW	BNUM_CMD1	Byte Number Of Commands 1 Sets the number of bytes in a command. (unit: bytes)	0x1
7	RW	RESPB_DATA	Respect busy signal after data phase. 0: Disable 1: Enable	0x0
6	RW	RESPB_ADDR	Respect busy signal after address phase. 0: Disable 1: Enable	0x0
5	RW	RESPB_CMD3	Respect busy signal after command 3 phase. 0: Disable 1: Enable	0x0
4	RW	RESPB_CMD2	Respect busy signal after command 2 phase. 0: Disable 1: Enable	0x0
3	RW	ECC_ENA	Error Correction Code (ECC) Enable 0: Disable 1: Enable NOTE: In read transfers, HW ECC check function is active. In write transfers, HW ECC generate function will be active.	0x0
2	RW	DMA_ENA	DMA Enable Sets the GDMA to read or write data to the data buffer. 0: CPU (default) 1: GDMA	0x0
1	RW	WR_TRANS	Sets a transfer to read or write. 0: Read 1: Write	0x0
0	W1C	KICK_TRANS	Kicks a NAND flash transfer. 0: No transfer 1: Kick a transfer NOTE: This bit will auto-clear	0x0

122. CMD1: Command 1 (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	CMD1_BYTE3	3rd byte of command 1	0x0
15:8	RW	CMD1_BYTE2	2nd byte of command 1	0x0
7:0	RW	CMD1_BYTE1	1st byte of command 1	0x0

123. CMD2: Command 2 (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	CMD2_BYTE3	3rd byte of command 2	0x0
15:8	RW	CMD2_BYTE2	2nd byte of command 2	0x0
7:0	RW	CMD2_BYTE1	1st byte of command 2	0x0

124. CMD3: Command 3 (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	CMD3_BYTE3	3rd byte of command 3	0x0
15:8	RW	CMD3_BYTE2	2nd byte of command 3	0x0
7:0	RW	CMD3_BYTE1	1st byte of command 3	0x0

125. ADDR: Address (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:24	RW	ADD_BYTE4	4th byte of NAND memory address	0x0
23:16	RW	ADD_BYTE3	3rd byte of NAND memory address	0x0
15:8	RW	ADD_BYTE2	2nd byte of NAND memory address	0x0
7:0	RW	ADD_BYTE1	1st byte of NAND memory address	0x0

126. DATA: Data (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:0	RW	DATA	Data for read / write	0x0

127. STATUS: ECC Status (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
16:8	RO	DEC_BYTE	ECC Decode Failed Byte Address Shows the address of a byte that failed ECC decoding.	0x0
7	-	-	Reserved	0x0
6:4	RO	DEC_BIT	ECC Decode Failed Byte Address Shows the address of a bit that failed ECC decoding.	0x0
3	-	-	Reserved	0x0
2	RO	ND_RB_N	NAND Flash Ready 0: Busy 1: Ready	0x1

Bits	Type	Name	Description	Initial Value
1	RO	DEC_ERR	Decode Error Shows the ECC decode check status. 0: No error 1: Correctable error or ECC error	0x0
0	RO	BUSY	NAND flash controller is busy. 0: Idle 1: Busy	0x0

128. INT_ENA: Interrupt Enable (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
7:0	RW	INT_ENA	Interrupt Enable Control 0: Disable 1: Enable	0x0

129. INT_STA: Interrupt Status (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
7	W1C	RX_BUF_ERR1	Rx Buffer Error 1 Interrupt Asserts when kicking a new transfer but the Rx buffer is not empty.	0x0
6	W1C	TX_BUF_ERR1	Tx Buffer Error 1 Interrupt Asserts when kicking a new transfer but the Tx buffer is not empty.	0x0
5	W1C	RX_BUF_ERR0	Rx Buffer Error 0 Interrupt Asserts when transfer is complete but the Rx buffer is not empty.	0x0
4	W1C	TX_BUF_ERR0	Tx Buffer Error 0 Interrupt Asserts when transfer is complete but the Tx buffer is not empty.	0x0
3	W1C	ECC_ERR	ECC Check Error Interrupt Asserts when an ECC error is detected.	0x0
2	W1C	RX_BUF_RRDY	Rx Buffer Read Ready Interrupt Asserts when the Rx buffer is ready for reads.	0x0
1	W1C	TX_BUF_WRDY	Tx Buffer Write Ready Interrupt Asserts when the Tx buffer is ready for writes.	0x0
0	W1C	XFER_DONE	Transfer Done Interrupt Asserts when transfer is complete.	0x0

130. CTRL1: Control 1 (offset: 0x003C)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19:16	RW	ECC_BYTE3_LOC	The location of 3 rd ECC byte in spare 16-byte	0x8

Bits	Type	Name	Description	Initial Value
15:12	RW	ECC_BYTE2_LOC	The location of 2 nd ECC byte in spare 16-byte	0x7
11:8	RW	ECC_BYTE1_LOCT	The location of 1 st ECC byte in spare 16-byte	0x6
7:2	-	-	Reserved	0x0
1	RW	DATA_BYTE_SWAP	Data Byte Swap Enable 0: Disable 1: Enable	0x0
0	RW	PAGE_SIZE	Page Size 0: 512 bytes per page 1: 2048 bytes per page	0x0

131. ECC_PAGE1: Error Correction Code Page 1 (offset: 0x0040)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:0	RO	ECC_PAGE1	HW ECC computing result for page1	0x0

132. ECC_PAGE2: Error Correction Code Page 2 (offset: 0x0044)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:0	RO	ECC_PAGE2	HW ECC computing result for page 2	0x0

133. ECC_PAGE3: Error Correction Code Page 3 (offset: 0x0048)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:0	RO	ECC_PAGE3	HW ECC computing result for page 3	0x0

134. ECC_PAGE4: Error Correction Code Page 4 (offset: 0x004C)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:0	RO	ECC_PAGE4	HW ECC computing result for page 4	0x0

135. ECC_ERR_PAGE1: ECC Error Information Page 1 (offset: 0x0050)

Bits	Type	Name	Description	Initial Value
31:15	-	-	Reserved	0x0
14:6	RO	ECC_ERR_BYTE	HW ECC Failed Byte Address Shows the address of a byte that failed ECC.	0x0
5	-	-	Reserved	0x0
4:2	RO	ECC_ERR_BIT	HW ECC Failed Bit Address Shows the address of a bit that failed ECC.	0x0
1	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
0	RO	ECC_ERR	HW ECC Failed 0: Pass 1: Fail	0x0

136. ECC_ERR_PAGE2: ECC Error Information Page 2 (offset: 0x0054)

Bits	Type	Name	Description	Initial Value
31:15	-	-	Reserved	0x0
14:6	RO	ECC_ERR_BYTE	HW ECC Failed Byte Address Shows the address of a byte that failed ECC.	0x0
5	-	-	Reserved	0x0
4:2	RO	ECC_ERR_BIT	HW ECC Failed Bit Address Shows the address of a bit that failed ECC.	0x0
1	-	-	Reserved	0x0
0	RO	ECC_ERR	HW ECC Failed 0: Pass 1: Fail	0x0

137. ECC_ERR_PAGE2: ECC Error Information Page 3 (offset: 0x0058)

Bits	Type	Name	Description	Initial Value
31:15	-	-	Reserved	0x0
14:6	RO	ECC_ERR_BYTE	HW ECC Failed Byte Address Shows the address of a byte that failed ECC.	0x0
5	-	-	Reserved	0x0
4:2	RO	ECC_ERR_BIT	HW ECC Failed Bit Address Shows the address of a bit that failed ECC.	0x0
1	-	-	Reserved	0x0
0	RO	ECC_ERR	HW ECC Failed 0: Pass 1: Fail	0x0

138. ECC_ERR_PAGE3: ECC Error Information Page 3 (offset: 0x005C)

Bits	Type	Name	Description	Initial Value
31:15	-	-	Reserved	0x0
14:6	RO	ECC_ERR_BYTE	HW ECC Failed Byte Address Shows the address of a byte that failed ECC.	0x0
5	-	-	Reserved	0x0
4:2	RO	ECC_ERR_BIT	HW ECC Failed Bit Address Shows the address of a bit that failed ECC.	0x0
1	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
0	RO	ECC_ERR	HW ECC Failed 0: Pass 1: Fail	0x0

139. ADDR2: Address 2 (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	ADD_BYTE7	7th byte of NAND memory address	0x0
15:8	RW	ADD_BYTE6	6th byte of NAND memory address	0x0
7:0	RW	ADD_BYTE5	5th byte of NAND memory address	0x0

2.11 PCM Controller

2.11.1 Features

- PCM module provides PBUS interface for register configuration and data transfer
- Two clock sources are reserved for PCM circuit. (From internal clock generator, INT_PCM_CLK and EXT_PCM_CLK)
- PCM module can drive a clock out (with fraction-N divisor) to an external codec.
- Up to 4 channels PCM are available. 4 to 128 slots are configurable.
- Each channel supports a-law (8-bit)/u-law (8-bit)/raw-PCM (8-bit and 16-bit) transfer.
- Hardware converter of a-law <-> raw-16 and u-law <-> raw-16 are implemented in design.
- Support long (8 cycle)/short (1 cycle)/configurable (intervals are configurable, use to emulate I²S interface) FSYNC.
- DATA & FSYNC can be driven and sampled by either rising/falling of clock.
- Last bit of DTX can be configured as tri-stated on falling edge.
- Beginning of each slot is configurable by 10-bit registers on each channel.
- 32-byte FIFO are available for each channel
- PCM interface can emulate I2S interface (only 16-bit data-width supported).
- MSB/LSB order is configurable.
- Supports both a-law/u-law (8-bits) → linear PCM(16-bit) and linear PCM(16-bit) → a-law/u-law (8-bit)

2.11.2 Block Diagram

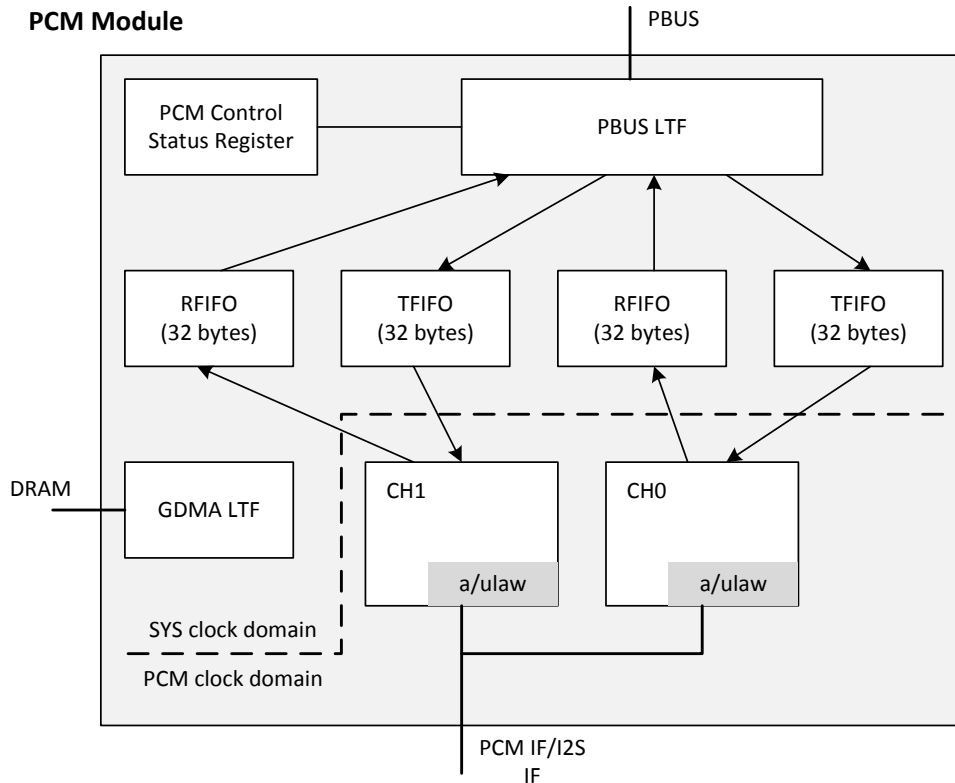


Figure 2-11 PCM Controller Block Diagram

Two clock domains are partitioned in this design. PCM converter (u-law $\leftrightarrow$ raw-16-bit and A-law $\leftrightarrow$ raw 16-bit) are implemented in PCM. The threshold of FIFO is configurable. When the threshold is reached, PCM (a) triggers the DMA interface to notify external DMA engine to transfer data, and (b) triggers an interrupt to the host.

The interrupt sources include:

- The threshold is reached.
- FIFO is under-run or over-run.
- A fault is detected at the DMA interface.

The A-law and u-law converter is implemented based on the ITU-G.711 A-law and u-law table. In this design, both A-law/u-law(8-bit) $\rightarrow$ linear PCM (16-bit) and linear PCM (16-bit) $\rightarrow$ A-law/u-law (8-bit) are supported.

The data-flow from codec to PCM-controller (Rx-flow) is shown as below:

- The PCM controller latches the data from DRX at the indicated time slot and then writes it to FIFO. If FIFO is full, the data is lost.
- When the Rx-FIFO reaches the threshold, two actions may be taken:
 - When DMA_ENA=1, DMA_REQ is asserted to request a burst transfer. It rechecks the FIFO threshold after DMA_END is asserted by GDMA. (GDMA should be configured before channel is enabled.)
 - Assert the interrupt source to notify the host. The host can check RFIFO_AVAIL information then get back the data from FIFO.

The data flow from the PCM controller to codec (Tx-flow) is shown below. After GDMA is configured, software should configure and enable the PCM channel. The empty FIFO should behave as follows.

- When DMA_ENA=1, DMA_REQ is triggered to request a burst transfer. It then re-checks the FIFO threshold after DMA_END is asserted by GDMA (a burst is completed).
- The Interrupt source is asserted to notify HOST. HOST writes the data to Tx-FIFO. After that, HOST rechecks TFIFO_EMPTY information, and then writes more data if available.

NOTE: When DMA_ENA=1, the burst size of GDMA should be less than the threshold value.

2.11.3 List of Registers

No.	Offset	Register Name	Description	Page
140	0x0000	GLB_CFG	Global Configuration	119
141	0x0004	PCM_CFG	PCM Configuration	120
142	0x0008	INT_STATUS	Interrupt Status	121
143	0x000C	INT_EN	Interrupt Enable	121
144	0x0010, 0x0110	CHA_FF_STATUSn	Channel A FIFO Status n	122
145	0x0014, 0x0114	CHB_FF_STATUSn	Channel B FIFO Status n	123
146	0x0020, 0x0120	CHA_CFGn	Channel A Configuration n	124
147	0x0024, 0x0124	CHnB_CFG	Channel B Configuration n	125
148	0x0030	FSYNC_CFG	PCM FSYNC Configuration	125
149	0x0034, 0x0134	CHA_CFG2	Channel A Configuration	126
150	0x0034, 0x0138	CHB_CFG2	Channel B Configuration	126
151	0x0040	IP_INFO	IP Address Information	127
152	0x0038	RSV_REG16	Reserved	127
153	0x0050	DIVCOMP_CFG	Integer Part of the Divisor	127
154	0x0054	DIVINT_CFG	Integer Part of the Divisor	127
155	0x0060	DIGDELAY_CFG	Digital Delay Configuration	127
156	0x0080	CH0_FIFO	Channel 0 FIFO	129
157	0x0084	CH1_FIFO	Channel 1 FIFO	129
158	0x0088	CH2_FIFO	Channel 2 FIFO	129
159	0x008C	CH3_FIFO	Channel 3 FIFO	129

2.11.4 Register Descriptions (base: 0x1000_2000)

140. GLB_CFG: (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31	RW	PCM_EN	PCM Enable When disabled, all FSM of PCM are cleared to their default value. 0: Disable 1: Enable	0x0
30	RW	DMA_EN	DMA Enable 0: Disable the DMA interface, transfer data using software. 1: Enable the DMA interface, transfer data using DMA.	0x0
29	RW	LBK_EN	Loopback Enable 0: Normal mode 1: Loopback (Asyn-TXFIFO → DTX → DRX → Asyn-RXFIFO)	0x0
28	RW	EXT_LBK_EN	External Loopback Enable 0: Normal mode 1: External loopback enable (Ext-Codec → DRX → DTX → Ext-Codec)	0x0
27:23	-	-	Reserved	0x0
22:20	RW	RFF_THRES	RXFIFO Threshold When the threshold is reached, the host/DMA is notified to fill FIFO. The threshold should be >2 and <6. When data in FIFO is under the threshold, the following interrupts and GDMA are triggered. ▪ CHOT_THRES ▪ CHOR_THRES ▪ CH1T_THRES ▪ CH1R_THRES (unit: word)	0x4
19	-	-	Reserved	0x0
18:16	RW	TFF_THRES	TXFIFO Threshold When the threshold is reached, the host/DMA is notified to fill FIFO. It should be >2 and <6. When data in FIFO is over the threshold, an interrupt and DMA are triggered. (unit: word)	0x4
15:4	-	-	Reserved	-
3:0	RW	CH_EN	Channels 3 to 0 Tx and Rx Enable 0: Disable 1: Enable	0x0

141. PCM_CFG: (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved for future.	0x0
30	RW	CLKOUT_EN	PCM Clock Out Enable 0: A PCM clock is provided from the external Codec/OSC. 1: A PCM clock is provided from the internal divisor. NOTE: Normally, the register should be asserted to 1. Also, it should be asserted after configuring the divider and enabling the divider clock.	0x0
29:28	-	-	Reserved	0x0
27	RW	EXT_FSYNC	FSYNC is provided externally 0: FSYNC is generated by internal circuit. 1: FSYNC is provided externally	0x0
26	RW	LONG_FSYNC	FSYNC Mode 0: Short FSYNC 1: Long FSYNC	0x0
25	RW	FSYNC_POL	FSYNC Polarity 0: FSYNC is low active 1: FSYNC is high active	0x1
24	RW	DTX_TRI	DTX Tri-State Tristates DTX when the clock signal on the last bit is has a falling edge. 0: Non- tristate DTX 1: Tristate DTX	0x1
23:3	-	-	Reserved	0x0
2:0	RW	SLOT_MODE	Sets the number of slots in each PCM frame. 0: 4 slots, PCM clock out/in should be 256 KHz. 1: 8 slots, PCM clock out/in should be 512 KHz. 2: 16 slots, PCM clock out/in should be 1.024 MHz. 3: 32 slots, PCM clock out/in should be 2.048 MHz. 4: 64 slots, PCM clock out/in should be 4.096 MHz. 5: 128 slots, PCM clock out/in should be 8.192 MHz. Other: Reserved. NOTE: When using the external clock, the frequency clock should be equal to PCM_clock out. Otherwise, the PCM_CLKin should be 8.192 MHz.	0x0

142. INT_STATUS: (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	R/W1C	CHT_DMA_FAULT	Channel Tx DMA Fault Interrupt Asserts when a fault has been detected in a CH-Tx DMA signal.	0x0
6	R/W1C	CHT_OVRUN	Channel Tx FIFO Overrun Interrupt Asserts when the CH-Tx FIFO is overrun.	0x0
5	R/W1C	CHT_UNRUN	Channel Tx FIFO Underrun Interrupt Asserts when the CH-Tx FIFO is underrun.	0x0
4	R/W1C	CHT_THRES	Channel Tx Threshold Interrupt Asserts when the CH-Tx FIFO is lower than the defined threshold.	0x0
3	R/W1C	CHR_DMA_FAULT	Channel Rx DMA Fault Interrupt Asserts when a fault is detected in a CH-Rx DMA signal.	0x0
2	R/W1C	CHR_OVRUN	Channel Rx Overrun Interrupt Asserts when the CH-Rx FIFO is overrun.	0x0
1	R/W1C	CHR_UNRUN	Channel Rx Underrun Interrupt Asserts when the CH-Rx FIFO is underrun.	0x0
0	R/W1C	CHR_THRES	Channel Rx Threshold Interrupt Asserts when the CH-Rx FIFO is lower than the defined threshold.	0x0

NOTE:

Read

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

143. INT_EN: (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:8	RO	-	Reserved	0x0
7	RW	INT7_EN	INT_STATUS[7] Enable Enables the Channel Tx DMA Fault Interrupt. This interrupt asserts when a fault has been detected in a CH-Tx DMA signal.	0x0
6	RW	INT6_EN	INT_STATUS[6] Enable Enables the Channel Tx FIFO Overrun Interrupt. This interrupt asserts when the CH-Tx FIFO is overrun.	0x0
5	RW	INT5_EN	INT_STATUS[5] Enable Enables the Channel Tx FIFO Underrun Interrupt. This interrupt asserts when the CH-Tx FIFO is underrun.	0x0

Bits	Type	Name	Description	Initial Value
4	RW	INT4_EN	INT_STATUS[4] Enable Enables the Channel Tx Threshold Interrupt. This interrupt when the CH-Tx FIFO is lower than the defined threshold.	0x0
3	RW	INT3_EN	INT_STATUS[3] Enable Enables the Channel Rx DMA Fault Interrupt. This interrupt when a fault is detected in a CH-Rx DMA signal.	0x0
2	RW	INT2_EN	INT_STATUS[2] Enable Enables the Channel Rx Overrun Interrupt. This interrupt when the CH-Rx FIFO is overrun.	0x0
1	RW	INT1_EN	INT_STATUS[1] Enable Enables the Channel Rx Underrun Interrupt. This interrupt when the CH-Rx FIFO is under-run.	0x0
0	RW	INT0_EN	INT_STATUS[0] Enable Enables the Channel Rx Threshold Interrupt. This interrupt asserts when the CH-Rx FIFO is lower than the defined threshold.	0x0

NOTE:

0: Disable

1: Enable

144. CHA_FF_STATUSn: (offset: 0x0010, 0x0110) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23	R/ W1C	CHTX_DMA_FAULT	Tx DMA Fault Detected Interrupt Asserts when a fault is detected in a Channel A Tx DMA signal.	0x0
22	R/ W1C	CHTX_OVRUN	Tx Overrun Interrupt Asserts when the Channel A Tx FIFO is overrun.	0x0
21	R/ W1C	CHTX_UNRUN	Tx FIFO Underrun Interrupt Asserts when the Channel A Tx FIFO is underrun.	0x0
20	R/ W1C	CHTX_THRES	Tx FIFO Below Threshold Interrupt Asserts when the Channel A FIFO is lower than the defined threshold.	0x1
19	R/ W1C	CHRX_DMA_FAULT	Rx DMA Fault Detected Interrupt Asserts when a fault is detected in a Channel A Rx DMA signal.	0x0
18	R/ W1C	CHRX_OVRUN	Rx FIFO Overrun Interrupt Asserts when the Channel A Rx FIFO is overrun.	0x0
17	R/ W1C	CHRX_UNRUN	Rx FIFO Underrun Interrupt Asserts when the Channel A Rx FIFO is underrun.	0x0

Bits	Type	Name	Description	Initial Value
16	R/ W1C	CHRX_THRES	Rx FIFO Below Threshold Interrupt Asserts when the Channel A FIFO is lower than the defined threshold.	0x0
15:8	-	-	Reserved	0x0
7:4	RO	CHRFF_AVCNT	Channel A RXFIFO Available Space Count Counts the available space for reads in channel A RXFIFO. (unit: word)	0x0
3:0	RO	CHTFF_EPCNT	Channel A TXFIFO Available Space Count Counts the available space for writes in channel A TXFIFO. (unit: word)	0x8

NOTE:

1. CHA_FF_STATUSn and CHB_FF_STATUSn registers have n=2 channels each, which together make up CHA0, CHB0, CHA1, and CHB1. To configure a specific channel, select an offset in CHA_FF_STATUSn or CHB_FF_STATUSn registers, where the first or second offset is indicated by n=0 or 1, respectively.

2. Where applicable,

Read

0: Not asserted

1: Asserted

Write

1: Clear this bit.

145. CHB_FF_STATUSn: (offset: 0x0014, 0x0114) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23	R/ W1C	CHTX_DMA_FAULT	Tx DMA Fault Detected Interrupt Asserts when a fault is detected in Channel B Tx DMA signal	0x0
22	W1C	CHTX_OVRUN	Tx Overrun Interrupt Asserts when the Channel B Tx FIFO is overrun.	0x0
21	W1C	CHTX_UNRUN	Tx FIFO Underrun Interrupt Asserts when the Channel B Tx FIFO is underrun.	0x0
20	W1C	CHTX_THRES	Tx FIFO Below Threshold Interrupt Asserts when the Channel B FIFO is lower than the defined threshold.	0x1
19	W1C	CHRX_DMA_FAULT	Rx DMA Fault Detected Interrupt Asserts when a fault is detected in a Channel B Rx DMA signal.	0x0
18	W1C	CHRX_OVRUN	Rx FIFO Overrun Interrupt Asserts when the Channel B Rx FIFO is overrun.	0x0
17	W1C	CHRX_UNRUN	Rx FIFO Underrun Interrupt Asserts when the Channel B Rx FIFO is underrun.	0x0

Bits	Type	Name	Description	Initial Value
16	W1C	CHRX_THRES	Rx FIFO Below Threshold Interrupt Asserts when the Channel B FIFO is lower than the defined threshold.	0x0
15:8	-	-	Reserved	0x0
7:4	RO	CHRFF_AVCNT	Channel B Rx FIFO Available Space Count Counts the available space for reads in channel A Rx FIFO. (unit: word)	0x0
3:0	RO	CHTFF_EPCNT	Channel B Tx FIFO Available Space Count Counts the available space for writes in channel A Tx FIFO. (unit: word)	0x8

NOTE:

1. CHA_FF_STATUSn and CHB_FF_STATUSn registers have n=2 channels each, which together make up CHA0, CHB0, CHA1, and CHB1. To configure a specific channel, select an offset in CHA_FF_STATUSn or CHB_FF_STATUSn registers, where the first or second offset is indicated by n=0 or 1, respectively.

2. Where applicable,

Read

0: Not asserted

1: Asserted

Write

1: Clear this bit.

146. CHA_CFGn: (offset: 0x0020, 0x0120) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	CMP_MODE	Compression Mode Sets the conversion method for the hardware converter to compress raw data. 000: Disable HW converter, linear raw data (16-bit) 010: Disable HW converter, linear raw data (8-bit), A-law or u-law (8-bit) 011: Reserved 100: Enable HW converter, raw data(16-bit) → U-law mode (8-bit) (PCM bus in compressed format) 101: Enable HW converter, u-law mode (8-bit) → raw data (16-bit) (PCM bus in raw, 16-bit format) 110: Enable HW converter, raw data (16-bit) → A-law mode (8-bit) (PCM bus in compressed format) 111: Enable HW converter, A-law mode (8-bit) → raw data (16-bit) (PCM bus in raw, 16-bit format)	0x0
26:10	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
9:0	RW	TS_START	Timeslot starting location (unit: clock cycles)	0x1

147. CHnB_CFG: (offset: 0x0024, 0x0124) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	CMP_MODE	Compression Mode Sets the conversion method for the hardware converter to compress raw data. 000: Disable HW converter, linear raw-data (16-bit) 010: Disable HW converter, linear raw-data (8-bit), A-law or u-law (8-bit) 011: Reserved 100: Enable HW converter, raw data (16-bit) → u-law mode (8-bit) (PCM bus in compressed format) 101: Enable HW converter, u-law mode (8-bit) → raw-data(16-bit) (PCM bus in raw, 16-bit format) 110: Enable HW converter, raw-data (16-bit) → A-law mode (8-bit) (PCM bus in compressed format) 111: Enable HW converter, A-law mode (8-bit) → raw-data (16-bit) (PCM bus in raw, 16-bit format)	0x0
26:10	-	-	Reserved	0x0
9:0	RW	TS_START	Timeslot starting location (unit: clock cycles)	0x1

148. FSYNC_CFG: (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31	RW	CFG_FSYNC_EN	Enables configurable FSYNC. 0: Disable 1: Enable	0x0
30	RW	POS_CAP_DT	Positive Edge Capture Data Sets the PCM controller to capture data on the negative or positive edge of the PCM clock. 0: Negative edge 1: Positive edge NOTE: This configuration should be 0 if DTX_TRI=1.	0x0

Bits	Type	Name	Description	Initial Value
29	RW	POS_DRV_DT	Positive Edge Drive Data Sets the PCM controller to drive data on the negative or positive edge of the PCM clock. 0: Negative edge 1: Positive edge	0x1
28	RW	POS_CAP_FSYNC	Positive Edge Capture FSYNC Sets the PCM controller to capture FSYNC on the positive or negative edge of the PCM clock. 0: Negative edge 1: Positive edge	0x0
27	RW	POS_DRV_FSYNC	Positive Edge Driver FSYNC Sets the PCM controller to drive FSYNC on the negative or positive edge of the PCM clock. 0: Negative edge of PCM clock 1: Positive edge of PCM clock	0x1
26:22	-	-	Reserved	0x0
21:10	-	-	Reserved	0x0
9:0	RW	FSYNC_INTV	Interval when FSYNC may be configured. (unit: clock cycles)	0x0

149. CHA_CFG2: (offset: 0x0034, 0x0134) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	0x0
3	RW	CH_RXFF_CLR	Channel A Rx FIFO Clear 0: Normal operation 1: Clear this bit	0x0
2	RW	CH_TXFF_CLR	Channel Tx FIFO Clear 0: Normal operation 1: Clear this bit	0x0
1	-	-	Reserved	0x0
0	RW	CH_LSB	Enable CH Tx in LSB order.	0x0

150. CHB_CFG2: (offset: 0x0034, 0x0138) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	0x0
3	RW	CH_RXFF_CLR	Channel B Rx FIFO Clear 0: Normal operation 1: Clear this bit	0x0
2	RW	CH_TXFF_CLR	Channel B Tx FIFO Clear 0: Normal operation 1: Clear this bit	0x0
1	-	-	Reserved	0x0
0	RW	CH_LSB	Enables CH transmit in LSB order	0x0

151. IP_INFO: (offset: 0x0040)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RO	MAX_CH	Maximum channel number.	0x4
7:0	RO	VER	Version of this PCM Controller	0x1

152. RSV_REG16: (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	SPARE_REG	Spare register for future use.	0x0

153. DIVCOMP_CFG: (offset: 0x0050)

Bits	Type	Name	Description	Initial Value
31	RW	CLK_EN	Clock Enable Enables setting of the PCM interface clock based on DIVCOMP and DIVINT parameters.	0x0
30:8	-	-	Reserved	0x0
7:0	RW	DIVCOMP	A parameter in an equation which determines FREQOUT. See DIVINT.	0x0

154. DIVINT_CFG: (offset: 0x0054)

Bits	Type	Name	Description	Initial Value
31:10	-	-	Reserved	0x0
9:0	RW	DIVINT	A parameter in an equation which determines FREQOUT. Formula: $\text{FREQOUT} = 1 / (\text{FREQIN} * 2 * (\text{DIVINT} + \text{DIVCOMP} / (2^8)))$ FREQIN is always fixed to 40 MHz.	0x0

155. DIGDELAY_CFG: (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
31	RW	TXD_CLR_GLT	TXD Clear Glitch Flag Clears the glitch detected flag for TXD. 0: No effect. 1: Clear the flag.	0x0
30	RW	CHEN_CLR_GLT	Channel Enable (CHEN) Clear Glitch Flag Clears the glitch detected flag for CHEN. 0: No effect . 1: Clear the flag.	0x0
29:27	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
26	RO	TXD_GLT_ST	TXD Glitch Status Indicates if a glitch is detected in a TXD signal. It can be cleared by bit[31]. 0: Not detected. 1: Detected	0x0
25:23	-	-	Reserved	0x0
22	RO	CHENN_GLT_ST	CHEN Negative Glitch Status Indicates if a glitch is detected in a CHEN signal. It can be cleared by bit[30] (negedge sample). 0: Not detected. 1: Detected	0x0
21:19	-	-	Reserved	0x0
18	RO	CHENP_GLT_ST	CHEN Positive Glitch Status Indicates if a glitch is detected in a CHEN signal. It can be cleared by bit[30] (posedge sample). 0: Not detected. 1: Detected	0x0
17	-	-	Reserved	0x0
16	RO	CHENPD_GLT_ST	CHEN Positive Delay Glitch Status Indicates if a glitch is detected in a CHEN signal. It can be cleared by bit[30] (posedge sample, delay 1 cycle). 0: Not detected. 1: Detected	0x0
15	RW	TXD_DIGDLY_EN	TXD Digital Delay Enable Enables digital delay path. 0: Disable 1: Enable	0x0
14:13	-	-	Reserved	0x0
12:8	RW	TXD_DLYVAL	Delay Count Value The description is the same as the CHEN_DLYVAL field in this register.	0x2
7	RW	CHEN_DIGDLY_EN	CHEN Digital Delay Enable Enables the digital delay path. 0: Disable 1: Enable	0x0
6:5	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
4:0	RW	CHEN_DLYVAL	Delay Count Value The delay error = $\text{CLK_PERIOD} * (\text{SYNC_DELAY} + \text{SYNC_DELTA} + (\text{DLYCNT_CFG}) + 1)$ For example, $\text{DLYCNT_CFG} = 4,$ (SYNC_DELAY is always fixed to 4) Final Delay $= \text{CLK_PERIOD} * (2 + (-1/0/+1) + (4) + 1)$ $= \text{CLK_PERIOD} * (6/7/8) = \text{CLK_PERIOD} * (6 \text{ to } 8)$ $= 25 \text{ ns to } 33.3 \text{ ns}$ NOTE: Period is 1/240 MHz = 4.1667 ns in MT7620.	0x2

156. CH0_FIFO: (offset: 0x0080)

Bits	Type	Name	Description	Initial Value
31:0	RW	CH0_FIFO	Channel 0 FIFO access point	0x0

157. CH1_FIFO: (offset: 0x0084)

Bits	Type	Name	Description	Initial Value
31:0	RW	CH1_FIFO	Channel 1 FIFO access point	0x0

158. CH2_FIFO: (offset: 0x0088)

Bits	Type	Name	Description	Initial Value
31:0	RW	CH2_FIFO	Channel 2 FIFO access point	0x0

159. CH3_FIFO: (offset: 0x008C)

Bits	Type	Name	Description	Initial Value
31:0	RW	CH3_FIFO	Channel 3 FIFO access point	0x0

2.11.5 PCM Configuration

2.11.5.1 PCM Initialization Flow

1. Set PCM_CFG
2. Set CH0/1_CFG
3. Write PCM data to FIFO CH0/1_FIFO
4. Set GLB_CFG to enable the PCM and channel.
5. Set divisor clock
6. Enable clock
7. Monitor FF_STATUS to receive/transmit the other PCM data.

2.11.5.2 PCM Configuration Examples

Below are some examples of PCM configuration.

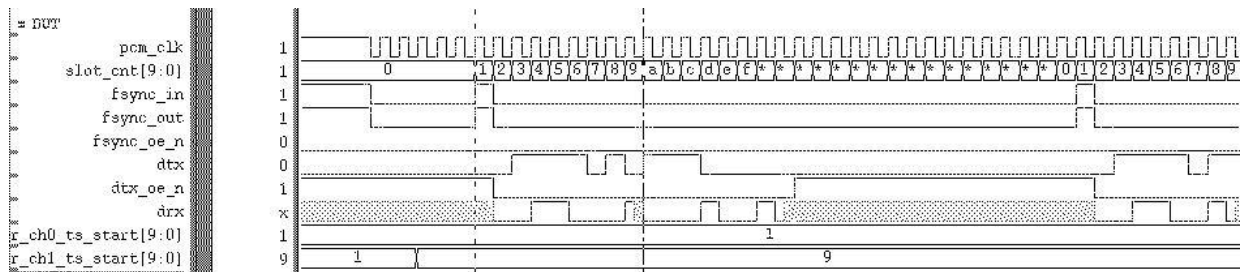
Case 1:

CFG_FSYNC Register: CFG_FSYNC_EN = 0 (PS: fsync is always driven at SLOT_CNT=1)

CH0_CFG Register: TS_START=1

CH1_CFG Register: TS_START=9

PCM_CFG Register: LONG_FSYNC=1'b0, FSYNC_POL=1'b1, DRX_TRI=1'b0, SLOT_MODE=3'b0



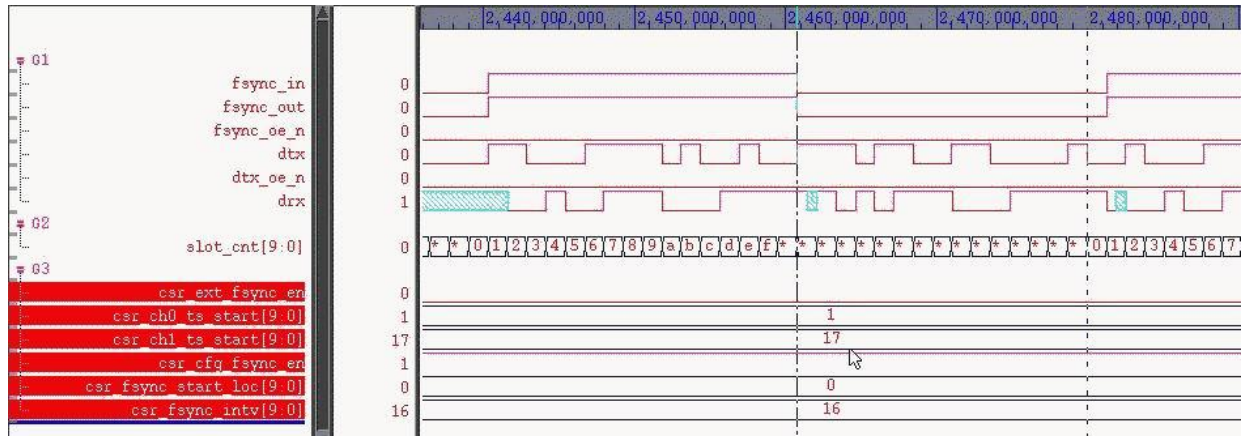
Case 2:

CFG_FSYNC Register: CFG_FSYNC_EN = 1, START_LOC=0, interval=16

CH0_CFG Register: TS_START=1

CH1_CFG Register: TS_START=17

PCM_CFG Register: LONG_FSYNC=1'b0, FSYNC_POL=1'b1, DRX_TRI=1'b0, SLOT_MODE=3'b0, RAW16-bits



Case 3:

CFG_FSYNC Register: CFG_FSYNC_EN = 1, START_LOC=0x1A, interval=2

CH0_CFG Register: TS_START=1 (disable)

CH1_CFG Register: TS_START=0x1A

PCM_CFG Register: LONG_FSYNC=1'b0, FSYNC_POL=1'b0 (LOW active), DRX_TRI=1'b0, SLOT_MODE=3'b0, RAW16-bits



2.12 Generic DMA Controller

2.12.1 Features

- Supports 16 DMA channels
- Supports 32 bit address.
- Maximum 65535 byte transfer
- Programmable DMA burst size (1, 2, 4, 8, 16 double word burst)
- Supports memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral transfers.
- Supports continuous mode.
- Supports division of target transfer count into 1 to 256 segments
- Support for combining different channels into a chain.
- Programmable hardware channel priority.
- Interrupts for each channel.

2.12.2 Block Diagram

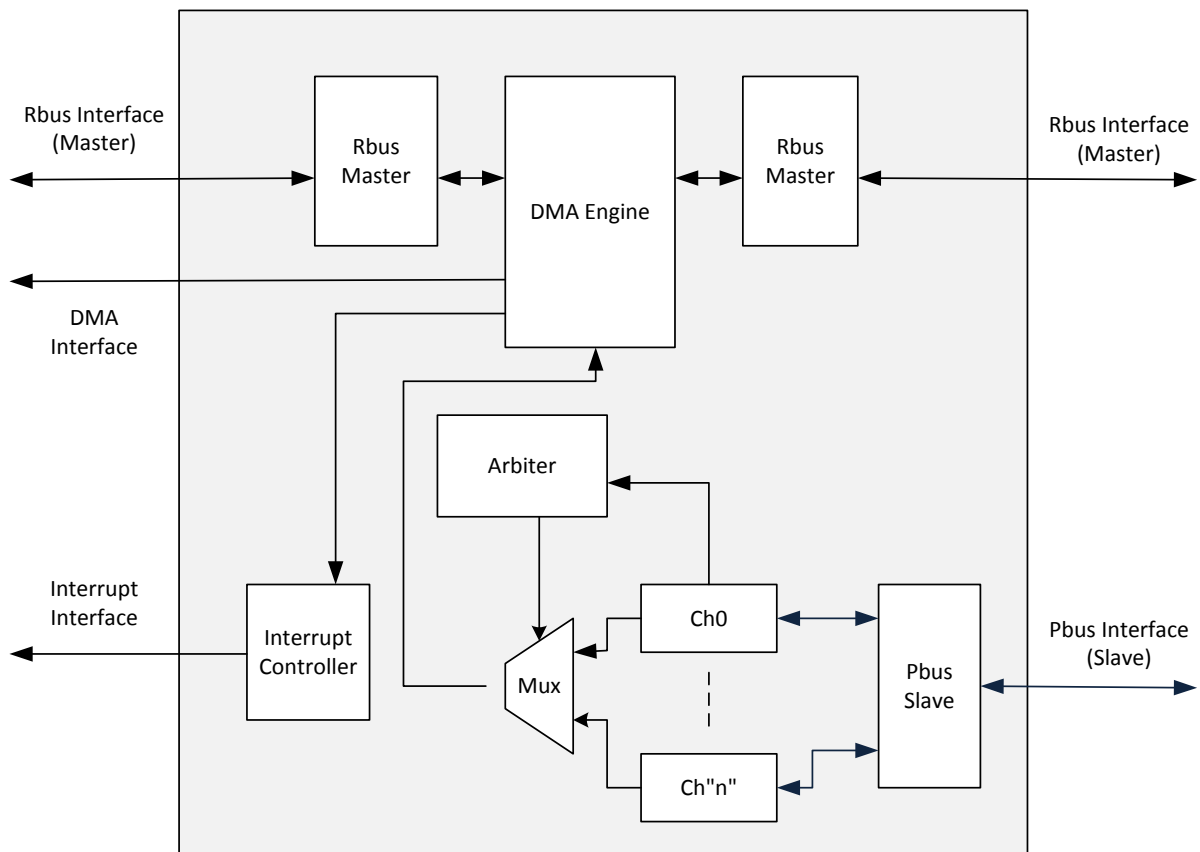


Figure 2-12 Generic DMA Controller Block Diagram

2.12.3 Peripheral Channel Connection

Channel number	Peripheral
0	Reserved
1	ND Controller
2	I2S Controller (TXDMA)
3	I2S Controller (RXDMA)
4	PCM Controller (RDMA, channel-0)
5	PCM Controller (RDMA, channel-1)
6	PCM Controller (TDMA, channel-0)
7	PCM Controller (TDMA, channel-1)
8	PCM Controller (RDMA, channel-2)
9	PCM Controller (RDMA, channel-3)
10	PCM Controller (TDMA, channel-2)
11	PCM Controller (TDMA, channel-3)
12	SPI Controller (RXDMA)
13	SPI Controller (TXDMA)
8 to 15	Reserved

2.12.4 List of Registers

No.	Offset	Register Name	Description	Page
160	0x0000, 0x0010, 0x0020, 0x0030, 0x0040, 0x0050, 0x0060, 0x0070, 0x0080, 0x0090, 0x00A0, 0x00B0, 0x00C0, 0x00D0, 0x00E0, 0x00F0	GDMA_SAn	GDMA Channel n Source Address	135
161	0x0004, 0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084, 0x0094, 0x00A4, 0x00B4, 0x00C4, 0x00D4, 0x00E4, 0x00F4	GDMA_DAn	GDMA Channel n Destination Address	135
162	0x0008, 0x0018, 0x0028, 0x0038, 0x0048, 0x0058, 0x0068, 0x0078, 0x0088, 0x0098, 0x00A8, 0x00B8, 0x00C8, 0x00D8, 0x00E8, 0x00F8	GDMA_CT0n	GDMA Channel n Control 0	135
163	0x000C, 0x001C, 0x002C, 0x003C, 0x004C, 0x005C, 0x006C, 0x007C, 0x008C, 0x009C, 0x00AC, 0x00BC, 0x00CC, 0x00DC, 0x00EC, 0x00FC	GDMA_CT1n	GDMA Channel n Control 1	136
164	0x0200	GDMA_UNMASKINT	GDMA Unmasked Interrupt Status	137
165	0x0204	GDMA_DONEINT	GDMA Interrupt Status	138
166	0x0220	GDMA_GCT	GDMA Global Control	138
167	0x02A0	GDMA_REQSTS	GDMA Request Status	138
168	0x02A4	GDMA_ACKSTS	GDMA Acknowledge Status	138
169	0x02A8	GDMA_FINSTS	GDMA Finish Status	138

2.12.5 Register Descriptions (base: 0x1000_2800)

160. GDMA_SAn: GDMA Channel n Source Address (offset: 0x0000, 0x0010, 0x0020, 0x0030, 0x0040, 0x0050, 0x0060, 0x0070, 0x0080, 0x0090, 0x00A0, 0x00B0, 0x00C0, 0x00D0, 0x00E0, 0x00F0) (n: 0 to 15)

Bits	Type	Name	Description	Initial Value
31:0	RW	CHANNEL SOURCE ADDRESS	Channel Source Address This register contains the source address information.	0x0

161. GDMA_DAn: GDMA Channel n Destination Address (offset: 0x0004, 0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084, 0x0094, 0x00A4, 0x00B4, 0x00C4, 0x00D4, 0x00E4, 0x00F4) (n: 0 to 15)

Bits	Type	Name	Description	Initial Value
31:0	RW	CHANNEL DESTINATION ADDRESS	Channel Destination Address This register contains the destination address information.	0x0

162. GDMA_CTOn: GDMA Channel n Control Register 0 (offset: 0x0008, 0x0018, 0x0028, 0x0038, 0x0048, 0x0058, 0x0068, 0x0078, 0x0088, 0x0098, 0x00A8, 0x00B8, 0x00C8, 0x00D8, 0x00E8, 0x00F8) (n: 0 to 15)

Bits	Type	Name	Description	Initial Value
31:16	RW	Target Transfer Count (Byte)	The number of bytes to be transferred.	0x0
15:8	RO	Current Segment	Indicates the current segment (0 to 255).	0x0
7	RW	Source Address Mode	Sets the source address mode 'b0: Incremental mode 'b1: Fix mode	0x0
6	RW	Destination Address Mode	Sets the destination address mode. 'b0: Incremental mode 'b1: Fix mode	0x0
5:3	RW	Burst Size	Sets the number of double words in each burst transaction. 'b000: 1 DW 'b001: 2 DWs 'b010: 4 DWs 'b011: 8 DWs 'b100: 16 DWs Others: Undefined	0x0
2	RW	Transmit Done Interrupt Enable	Enables the transmit done interrupt. This interrupt asserts after transfer of each segment is done. 'b1: Enable 'b0: Disable	0x0

Bits	Type	Name	Description	Initial Value
1	RW	Channel Enable	Channel Enable 'b0: Disable 'b1: Enable If CONTINUOUS MODE ENABLE=0, this bit is de-asserted by hardware after the number of bytes transferred reaches the Target Transfer Count.	0x0
0	RW	Hardware/Software Mode Select	Hardware/Software Mode Select 'b1: Software Mode 'b0: Hardware Mode - In software mode, the data transfer starts when the Channel Enable bit is set. - In hardware mode, the data transfer starts when DMA Request is asserted.	0x0

163. GDMA_CT1n: GDMA Channel n Control Register 1 (offset: 0x000C, 0x001C, 0x002C, 0x003C, 0x004C, 0x005C, 0x006C, 0x007C, 0x008C, 0x009C, 0x00AC, 0x00BC, 0x00CC, 0x00DC, 0x00EC, 0x00FC) (n: 0 to 15)

Bits	Type	Name	Description	Initial Value
31:26	-	-	Reserved	0x0
25:22	RW	Number of Segment (N)	The number of segments= 2^N , where N is the value of this bit. Valid values for this bit range from N=0 to 8. The segment size=(Target Transfer Count/ 2^N). If Target Transfer Count is not a multiple of 2^N , the segment size = (Target Transfer Count/ 2^N) + 1.	0x0
21:16	RW	Source DMA Request	Selects the source DMA request. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 ... n: DMA_REQn 32: The source of the transfer is memory Others: Undefined	0x0
15	-	-	Reserved	0x0
14	RW	Continuous Mode Enable	Sets HW to keep the data channel enabled when the number of bytes transferred reaches the Target Transfer Count defined in the GDMA_CT0n register. 0: HW will clear Channel Enable after the target transfer count is reached. 1: HW will NOT clear Channel Enable after the target transfer count is reached.	0x0

Bits	Type	Name	Description	Initial Value
13:8	RW	Destination DMA Request	Selects the destination DMA request. 0: DMA_REQ0 1: DMA_REQ1 2: DMA_REQ2 ... n: DMA_REQn 32: The destination of the transfer is memory. Others: Undefined	0x0
7:3	RW	Next Channel to Unmask	Selects the next unmasked channel. When the number of bytes transferred reaches the Target Transfer Count, the hardware clears the Channel Mask bit of the Next Channel to Unmask. 0: Channel 0 1: Channel 1 2: Channel 2 ... n: Channel n If the hardware does not need to clear any Channel Mask bit, these bits must be set to their own channel.	0x0
2	RW	Coherent Interrupt Enable	Enables the coherent interrupt. 1'b1: GDMA issues a dummy READ to Destination after the last WRITE to Destination. This can ensure the last WRITE arrived at the MEM and avoids a race problem between interrupt and data to the MEM. NOTE: Do not set this to 1'b1 if the destination is not MEM.	0x0
1	RW	Channel Unmask Failure Interrupt Enable	Enables the channel unmasked interrupt. 'b0: Disable 'b1: Enable When this bit is set, an interrupt is asserted when the hardware tries to clear the Channel Mask bit of Next Channel to Unmask but the Channel Mask bit is already set to 0.	0x0
0	RW	Channel Mask	Channel Mask 'b0: This channel is not masked 'b1: This channel is masked When this channel mask is set, the GDMA transaction does not start until this bit is clear.	0x0

164. GDMA_UNMASKINT: GDMA Unmasked Interrupt Status Register (offset: 0x0200)

Bits	Type	Name	Description	Initial Value
------	------	------	-------------	---------------

Bits	Type	Name	Description	Initial Value
31:0	W1C	Unmask Fail Interrupt	Indicates the status of unmasked fail interrupt. This bit is set when the hardware tries to clear the Channel Mask bit of Next Channel to Unmask but the Channel Mask bit is 0 already. Bit[n:0] is for channels n to 0 respectively.	0x0

165. GDMA_DONEINT: GDMA Interrupt Status Register (offset: 0x0204)

Bits	Type	Name	Description	Initial Value
31:0	W1C	Transmit Done Interrupt Status	Indicates the status of the transmit-done interrupt. The interrupt asserts after each segment size is transferred. Bit[n:0] is for channels n to 0 respectively.	0x0

166. GDMA_GCT: GDMA Global Control Register (offset: 0x0220)

Bits	Type	Name	Description	Initial Value
31:5	-	-	Reserved	-
4:3	RO	Total channel number	2'b0: 8 channels 2'b1: 16 channels 2'b2: 32 channels 2'b3: Reserved	0x1
2:1	RO	IP version	GDMA Core Version	0x3
0	RW	Arbitration Selection	Selects the channel arbitration method. 1'b0: Channel 0 has the highest priority. Channels 1 to n are round-robin. 1'b1: Channels 0 to n are round-robin.	0x0

167. GDMA_REQSTS: GDMA Request Status Register (offset: 0x02A0)

Bits	Type	Name	Description	Initial Value
31:0	RO	GDMA Request Signal Status	Indicates the status of the GDMA request signal. Bit[n:0] are for GDMA_REQ n to 0 respectively.	0x0

168. GDMA_ACKSTS: GDMA Acknowledge Status Register (offset: 0x02A4)

Bits	Type	Name	Description	Initial Value
31:0	RO	GDMA Acknowledge Signal Status	Indicates the status of the GDMA Acknowledge Signal. Bit[n:0] are for GDMA_ACK n to 0 respectively.	0x0

169. GDMA_FINSTS: GDMA Finish Status Register (offset: 0x02A8)

Bits	Type	Name	Description	Initial Value
31:0	RO	GDMA Finish Signal Status	Indicates the status of the GDMA Finish Signal. Bit[n:0] are for GDMA_FINISH n to 0 respectively.	0x0

2.13 SPI Controller

2.13.1 Features

- Supports up to 2 SPI master operations
- Programmable clock polarity
- Programmable interface clock rate
- Programmable bit ordering
- Firmware-controlled SPI enable
- Programmable payload (address + data) length
- Supports 1/2/4 multi-IO SPI flash memory
- Supports command/user mode operation
- Supports SPI direct access
- Extends the addressable range from 24 bits to 32 bits for memory size larger than 128 Mb.

2.13.2 Block Diagram

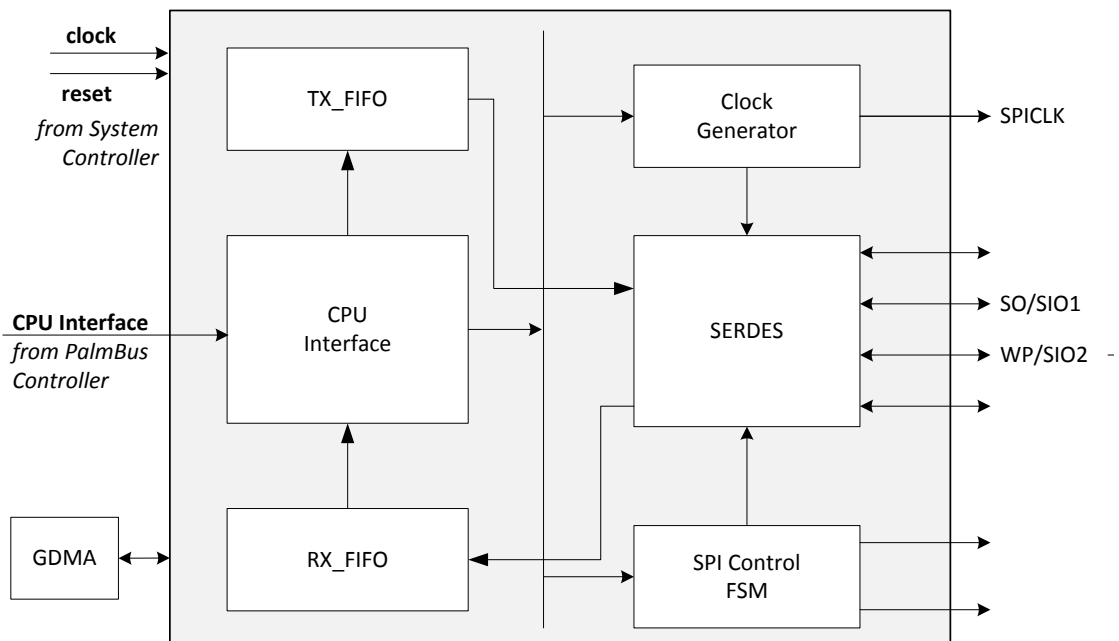


Figure 2-13 SPI Controller Block Diagram

2.13.3 List of Registers

No.	Offset	Register Name	Description	Page
170	0x0000	SPISTAT0171	SPI Interface 0 Status	141
171	0x0004	Reserved	-	141
172	0x0008	Reserved	-	141
173	0x000C	Reserved	-	141
174	0x0010	SPICFG0	SPI Interface 0 Configuration	141
175	0x0014	SPICTL0	SPI Interface 0 Control	142
176	0x0020	SPIDATA0	SPI Interface 0 Data	143
177	0x0024	SPIADDR0	SPI Interface 0 Address	144
178	0x0028	SPIBS0	SPI Interface 0 Block Size	144
179	0x002C	SPIUSER0	SPI Interface 0 User Mode	144
180	0x0030	SPITXFIFO0	SPI Interface 0 TX_FIFO	146
181	0x0034	SPIRXFIFO0	SPI Interface 0 RX_FIFO	146
182	0x0038	SPIFIFOSTAT0	SPI Interface 0 FIFO_STATUS	146
183	0x003C	SPIMD0	SPI Interface 0 Mode	147
184	0x0040	SPISTAT1	SPI Interface 1 Status	147
185	0x0050	SPICFG1	SPI Interface 1 Configuration	147
186	0x0054	SPICTL1	SPI Interface 1 Control	148
187	0x0060	SPIDATA1	SPI Interface 1 Data	149
188	0x0080	SPIDMA	SPI Interface DMA	150
189	0x0084	SPIDMASTAT	SPI Interface DMA_FIFO_STATUS	150
190	0x00F0	SPIARB	SPI Interface Arbiter	150

2.13.4 Register Descriptions (base: 0x1000_0B00)

170. SPISTAT0: SPI Interface 0 Status (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	-
0	RO	BUSY	Indicates SPI transfer in progress 0: The SPI interface is inactive. 1: An SPI transfer is in progress. NOTE: This bit must be set to 0 before initiating a transfer. Any attempt to start a data transfer is ignored if this bit is a 1.	0x0

171. Reserved (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:0	-	-	Reserved	0x0

172. Reserved: (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:0	-	-	Reserved	0x0

173. Reserved: (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:6	-	-	Reserved	0x0

174. SPICFG0: SPI Interface 0 Configuration (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:13	-	-	Reserved	-
12	RW	ADDRMODE	SPI Address Mode 0: 3-Byte address mode (for SPI flash <= 128 Mb) 1: 4-Byte address mode (for SPI flash >= 256 Mb)	0x0
11	RW	RXENVDIS	Rx Pre-Envelope Disable Disables setting a pre-data input before the first data is received. 0: Enable clock PRE_ENVELOP (slave mode) 1: Disable clock PRE_ENVELOP (SPI flash mode)	0x0
10	RW	RXCAP	Rx Capture Delay Mode 0: Rx data capture is not delayed. 1: Rx data capture is delayed for half an SPICLK cycle	0x0

Bits	Type	Name	Description	Initial Value
9	RW	SPIENMODE	SPI Enable Mode 0: SPI Enable is controlled by SW register settings (SPICTL0) 1: SPI Enable is controlled by HW (SPI Flash CMD)	0x0
8	RW	MSBFIRST	Bit Transfer Order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. NOTE: This bit applies to both the command and data.	0x1
7	-	-	Reserved	-
6	RW	SPICKPOL	SPI Clock Default Polarity Sets the default state of the SPICLK 0: Logic 0 1: Logic 1 NOTE: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	0x0
5	RW	RXCKEDGE	Rx Clock Capture Edge 0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	0x0
4	RW	TXCKEDGE	Tx Clock Transmit Edge 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	0x0
3	RW	HIZSPI	Tri-state all SPI pins 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. NOTE: This bit overrides all normal functionality.	0x0
2:0	RW	SPICLK	SPI Clock Divide Control 0: SPICLK rate is system clock rate / 2 1: SPICLK rate is system clock rate / 4 2: SPICLK rate is system clock rate / 8 3: SPICLK rate is system clock rate / 16 4: SPICLK rate is system clock rate / 32 5: SPICLK rate is system clock rate / 64 6: SPICLK rate is system clock rate / 128 7: SPICLK is disabled. NOTE: These rates may change in the future.	0x4

175. SPICTL0: SPI Interface 0 Control (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:5	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
4	RW	START	Start SPI Flash Transaction Mode 0: No effect 1: Starts SPI internal controller to start an SPI instruction transaction. NOTE: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
3	RW	HIZSDO	Tri-state Data Out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. NOTE: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	0x0
2	WO	STARTWR	Start SPI Write Transfer 0: No effect. 1: The contents of the SPIDATA register are transferred to the SPI slave device. NOTE: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
1	WO	STARTRD	Start SPI Read Transfer 0: No effect. 1: Start a read from the SPI slave. The read data is placed in the SPIDATA register. NOTE: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
0	RW	SPIENA	SPI Enable 0: The SPIENA pin is negated. 1: The SPIENA pin is asserted.	0x0

176. SPIDATA0: SPI Interface 0 Data (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
7:0	RW	SPIDATA	SPI Data Transfer This register is used for command/data transfers on the SPI interface. The use of this register is given below: <i>Write</i> The bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA [0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. <i>Read</i> The command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register. When using SPI Flash transaction, this SPIDATA[7:0] is used for SPI_INSTR[7:0].	0x0

177. SPIADDR0: SPI Interface 0 Address (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:0	RW	SPI_ADDR	SPI Flash Address When 3-Byte SPI address is configured, SPI_ADDR[31:8] is used. When 4-Byte SPI address is configured, SPI_ADDR[31:0] is used.	0x0

178. SPIBS0: SPI Interface 0 Block Size (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:0	RW	SPI_BLOCKSIZE	SPI Block Size Defines how many data bytes are transferred during an SPI instruction execution.	0x0

179. SPIUSER0: SPI Interface 0 User Mode (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:22	-	-	Reserved	0x0
21	RW	USERMODE	User Manual SPI Mode Enable 0: Disable user mode 1: Enable user mode. Allows SW to set the phase and type of SPI commands that are not pre-defined.	0x0

Bits	Type	Name	Description	Initial Value
20	RW	INSTR_PHASE	Instruction Phase 0: No instruction bytes 1: One byte instruction phase (SPIDATA0)	0x0
19:17	RW	ADDR_PHASE	Address Phase 000: No address byte 001: One byte address phase (SPIADDR0[31:24]) 010: Two byte address phase (SPIADDR0[31:16]) 011: Three byte address phase (SPIADDR0[31:8]) 100: Four byte address phase (SPIADDR0[31:0]) Others: Reserved	0x0
16	RW	MODE_PHASE	Mode Phase Byte Count 0: No mode bytes 1: One mode byte (SPIMD0[31:24])	0x0
15:14	RW	DUMMY_PHASE	Dummy Phase Byte Count 00: No dummy phase 01: One dummy byte 10: Two dummy bytes 11: Three dummy bytes	0x0
13:12	RW	DATA_PHASE	Data Phase Type 00: No data phase 01: Read data phase 10: Write data phase 11: Reserved Data writes to Tx/Rx FIFO when user mode is enabled.	0x0
11:9	RW	ADDR_TYPE	Address Transfer Type 001: Single Address Mode 010: Dual Address Mode 100: Quad Address Mode Others: Reserved	0x0
8:6	RW	MODE_TYPE	Mode Transfer Type 001: Single Address Mode 010: Dual Address Mode 100: Quad Address Mode Others: Reserved	0x0
5:3	RW	DUMMY_TYPE	Dummy Transfer Type 001: Single Address Mode 010: Dual Address Mode 100: Quad Address Mode Others: Reserved	0x0

Bits	Type	Name	Description	Initial Value
2:0	RW	DATA_TYPE	Data Transfer Type 001: Single Address Mode 010: Dual Address Mode 100: Quad Address Mode Others: Reserved	0x0

180. SPITXFIFO0: SPI Interface 0 TX_FIFO (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:8	RW	TX_FIFO	This register is used to write TX_DMA_FIFO[31:8].	0x0
7:0	RW	TX_FIFO	This register is used to write TX_FIFO[7:0]/TX_DMA_FIFO[7:0].	0x0

181. SPIRXFIFO0: SPI Interface 0 RX_FIFO (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31:8	RC	RX_FIFO	This register is used to read RX DMA FIFO[31:8].	0x0
7:0	RC	RX_FIFO	This register is used to read RX_FIFO[7:0]/RX_DMA_FIFO[7:0].	0x0

182. SPIFIFOSTAT0: SPI Interface 0 FIFO_STATUS (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RO	TX_EMPTY	Tx FIFO Empty	0x1
18	RO	RX_EMPTY	Rx FIFO Empty Should not read SPIRXFIFO0 data when this flag is true.	0x1
17	RO	TX_FULL	Tx FIFO Full Should not write SPITXFIFO0 data when this flag is true.	0x0
16	RO	RX_FULL	Rx FIFO Full	0x0
15:8	RO	TX_FIFO_CNT	Tx FIFO Count Transmit FIFO Depth = 16, When TX_FIFO_CNT=0, TX_EMPTY=1. When TX_FIFO_CNT=16, TX_FULL=1.	0x0
7:0	RO	RX_FIFO_CNT	Rx FIFO Count Receive FIFO Depth = 16, When RX_FIFO_CNT=0, RX_EMPTY=1. When RX_FIFO_CNT=16, RX_FULL=1.	0x0

NOTE: Where applicable,
0: False
1: True

183. SPIMD0: SPI Interface 0 Mode (offset: 0x003C)

Bits	Type	Name	Description	Initial Value
31:24	RW	SPI_MODE	SPI Flash Mode Selects the SPI flash mode. Available modes depend on the SPI flash vendor. For more information on available modes, please check the datasheet provided by the SPI vendor.	0x0
23:0	RW	SPI_DUMMY	SPI Dummy Contains data used for dummy writes to the SPI flash.	0x0

184. SPISTAT1: SPI Interface 1 Status (offset: 0x0040)

Bits	Type	Name	Description	Initial Value
31:2	-	-	Reserved	-
0	RO	BUSY	SPI Transfer In Progress 0: The SPI interface is inactive. 1: An SPI transfer is in progress. NOTE: This bit must be 0 before initiating a transfer. Any attempt to start a data transfer will be ignored if this bit is 1.	0x0

185. SPICFG1: SPI Interface 1 Configuration (offset: 0x0050)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11	RW	RXENVDIS	Rx Pre-Envelope Disable Disables setting a pre-data input before the first data is received. 0: Enable clock PRE_ENVELOP when (CLOCK_POL ^ RX_CLKEDGE = 0) 1: Disable clock PRE_ENVELOP (SPI flash mode)	0x0
10	RW	RXCAP	Rx Capture Delay Mode 0: Rx data captured is not delayed. 1: Rx data captured is delayed for half a SPICLK cycle.	0x0
9	-	-	Reserved	-
8	RW	MSBFIRST	Bit Transfer Order 0: LSB bits of data sent/received first. 1: MSB bits of data sent/received first. NOTE: This bit applies to both the command and data.	0x1
7	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
6	RW	SPICKPOL	SPI Clock Default Polarity Sets the default state of the SPICLK. 0: Logic 0 1: Logic 1 NOTE: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).	0x0
5	RW	RXCKEDGE	SPI Clock Default State 0: Data is captured on the rising edge of the SPICLK signal. 1: Data is captured on the falling edge of the SPICLK signal.	0x0
4	RW	TXCKEDGE	SPI Clock Default State 0: Data is transmitted on the rising edge of the SPICLK signal. 1: Data is transmitted on the falling edge of the SPICLK signal.	0x0
3	RW	HIZSPI	Tri-states all SPI pins 0: SPICLK and SPIENA pin are driven. 1: SPICLK and SPIENA pin are tri-stated. NOTE: This bit overrides all normal functionality.	0x0
2:0	RW	SPICLK	SPI Clock Divide Control Sets the SPI clock divisor. 0: SPICLK rate = system clock rate / 2 1: SPICLK rate = system clock rate / 4 2: SPICLK rate = system clock rate / 8 3: SPICLK rate = system clock rate / 16 4: SPICLK rate = system clock rate / 32 5: SPICLK rate = system clock rate / 64 6: SPICLK rate = system clock rate / 128 7: SPICLK is disabled NOTE: These rates may change in the future.	0x4

186. SPICTL1: SPI Interface 1 Control (offset: 0x0054)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	-
3	RW	HIZSDO	Tri-state Data Out 0: The SPIDO pin remains driven after the cycle is complete. 1: The SPIDO pin is tri-stated after the cycle is complete. NOTE: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.	0x0

Bits	Type	Name	Description	Initial Value
2	WO	STARTWR	Start SPI Write Transfer 0: No effect. 1: The contents of the SPIDATA register are transferred to the SPI slave device. NOTE: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
1	WO	STARTRD	Start Read 0: No effect. 1: Start a read from the SPI slave. The read data is placed in the SPIDATA register. NOTE: The BUSY bit in the SPISTAT register is set when a this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.	0x0
0	RW	SPIENA	SPI Enable 0: The SPIENA pin is set low. 1: The SPIENA pin is set high.	0x0

187. SPIDATA1: SPI Interface 1 Data (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	-
7:0	RW	SPIDATA	This register is used for command/data transfers on the SPI interface. The use of this register is given below: <i>Write</i> The bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA [0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits. <i>Read</i> The command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.	0x0

188. SPIDMA: SPI Interface DMA (offset: 0x0080)

Bits	Type	Name	Description	Initial Value
31:11	-	-	Reserved	0x0
10:9	RW	TxBurstSize	The number of transfers in a Tx burst transaction. 'b00: 1 transfer 'b01: 2 transfers 'b10: 4 transfers Others: Undefined	0x1
8	RW	TXDMA	Tx DMA Enable 0: Disable Tx GDMA 1: Write Tx FIFO from GDMA	0x0
7:3	-	-	Reserved	0x0
2:1	RW	RxBurstSize	The number of transfers in a Rx burst transaction. 'b00: 1 transfer 'b01: 2 transfers 'b10: 4 transfers Others: Undefined	0x1
0	RW	RXDMA	Rx DMA Enable 0: Disable Rx GDMA 1: Read Rx FIFO from GDMA	0x0

189. SPIDMASTAT: SPI Interface DMA FIFO Status (offset: 0x0084)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RO	TX_DMA_EMPTY	Indicates the Tx DMA FIFO is empty.	0x1
18	RO	RX_DMA_EMPTY	Indicates the Rx DMA FIFO is empty.	0x1
17	RO	TX_DMA_FULL	Indicates the Tx DMA FIFO is full.	0x0
16	RO	RX_DMA_FULL	Indicates the Rx DMA FIFO is full.	0x0
15:8	RO	TX_DMA_CNT	Shows the value of the Tx DMA FIFO counter.	0x0
7:0	RO	RX_DMA_CNT	Shows the value of the Rx DMA FIFO counter.	0x0

NOTE: Where applicable,
0: False
1: True

190. SPIARB: SPI Interface Arbiter (offset: 0x00F0)

Bits	Type	Name	Description	Initial Value
31	RW	ARB_EN	Arbiter Enable 0: Only one SPI interface will work depending on CSCTL settings. 1: SPI Interface 0 and 1 work concurrently.	0x0
30:19	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
18:16	RW	CSCTL	Chip Select Control 000: SPI control for chip select 0 001: SPI control for chip select 1 010-111: Reserved	0x0
15:2	-	-	Reserved	-
1	RW	SPI1_POR	SPI1 Pin Polarity Read Indicates that the SPI device on interface 1 is active depending on whether the chip enable pin is high or low. 0: Active when the chip enable pin is low. 1: Active when the chip enable pin is high.	0x0
0	RW	SPI0_POR	SPI0 Polarity Read Indicates that the SPI device on interface 0 is active depending on whether the chip enable pin is high or low. 0: Active when the chip enable pin is low. 1: Active when the chip enable pin is high	0x0

NOTE: This register must be configured when SPI interface 1 is activated.

2.14 I2S Controller

2.14.1 Features

- I2S transmitter/receiver, which can be configured as master or slave.
- Supports 16-bit data, sampling rates of 8 kHz, 16 kHz, 22.05 kHz, 44.1 kHz, and 48 kHz
- Support stereo audio data transfer.
- 32-byte FIFO are available for data transmission.
- Supports GDMA access
- Supports 12 Mhz bit clock from external source (when in slave mode)

2.14.2 Block Diagram

The I²S transmitter block diagram is shown as below.

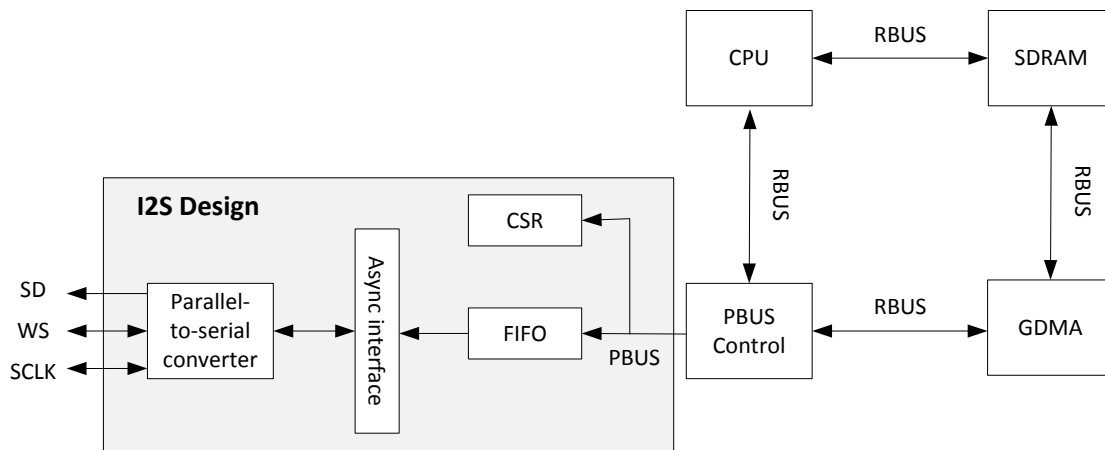


Figure 2-14 I²S Transmitter Block Diagram

The I²S interface consists of two separate cores, a transmitter and a receiver. Both can operate in either master or slave mode. The transmitter is only shown here in master or slave mode.

2.14.3 I²S Signal Timing For I²S Data Format

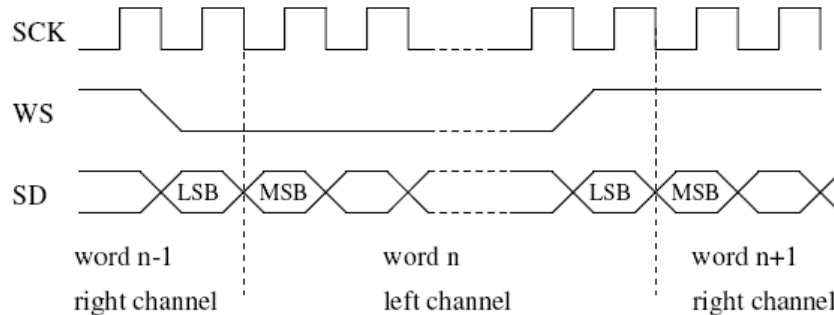


Figure 2-15 I2S Transmit/Receive

Serial data is transmitted in 2's complement with the MSB first. The transmitter always sends the MSB of the next word one clock period after the WS changes. Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left)
- WS = 1; channel 2 (right)

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next Word.

2.14.4 List of Registers

No.	Offset	Register Name	Description	Page
191	0x0000	I2S_CFG	I ² S Configuration	155
192	0x0004	INT_STATUS	Interrupt Status	156
193	0x0008	INT_EN	Interrupt Enable	156
194	0x000C	FF_STATUS	FIFO Status	157
195	0x0010	TX_FIFO_WREG	Transmit FIFO Write to Register	157
196	0x0014	RX_FIFO_RREG	Receive FIFO Read Register	157
197	0x0018	I2S_CFG1	I ² S Configuration 1	157
198	0x0020	DIVCOMP_CFG	Integer Part of the Divisor Register 1	158
199	0x0024	DIVINT_CFG	Integer Part of the Divisor Register 2	158

2.14.5 Register Descriptions (base: 0x1000_0A00)

191. I2S_CFG: I²S Tx/Rx Configuration Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31	RW	I2S_EN	I ² S Enable Enables I ² S. When disabled, all I ² S control registers are cleared to their initial values. 0: Disable 1: Enable	0x0
30	RW	DMA_EN	DMA Enable Enables DMA access. 0: Disable 1: Enable	0x0
29	-	-	Reserved	0x0
28	RW	BYTE_SWAP	Swaps the order of data bytes in each 16-bit channel. 0: No data swap 1: Data byte swap	0x0
27:25	-	-	Reserved	0x0
24	RW	TX_EN	Transmitter on/off control 0: Disable 1: Enable	0x0
23:21	-	-	Reserved	0x0
20	RW	RX_EN	Receiver on/off control 0: Disable 1: Enable	0x0
19:17	-	-	Reserved	0x0
16	RW	SLAVE_MODE	Sets master or slave mode. 0: Master: using internal clock 1: Slave: using external clock	0x1
15	-	-	Reserved	0x0
14:12	RW	RX_FF_THRES	Rx FIFO Threshold When the threshold is reached, the host/DMA is notified to fill FIFO. 2<RX_FF_THRES<6 (unit: word)	0x4
11:7	-	-	Reserved	0x0
6:4	RW	TX_FF_THRES	Tx FIFO Threshold When the threshold is reached, the host/DMA is notified to fill FIFO. 2<TX_FF_THRES<6 (unit: word)	0x4
3:0	-	-	Reserved	0x0

192. INT_STATUS: I²S Interrupt Status (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:8	R	-	Reserved	0x0
7	R/ W1C	RX_DMA_FAULT	Rx DMA Fault Detected Interrupt Asserts when a fault is detected in Rx DMA signals.	0x0
6	R/ W1C	RX_OVRUN	Rx Overrun Interrupt Asserts when the Rx FIFO is overrun.	0x0
5	R/ W1C	RX_UNRUN	Rx Underrun Interrupt Asserts when the Rx FIFO is underrun.	0x0
4	R/ W1C	RX_THRES	Rx FIFO Below Threshold Interrupt Asserts when the Rx FIFO is lower than the defined threshold.	0x0
3	R/ W1C	TX_DMA_FAULT	Tx DMA Fault Detected Interrupt Asserts when a fault is detected in Tx DMA signals.	0x0
2	R/ W1C	TX_OVRUN	Tx FIFO Overrun Interrupt Asserts when the Tx FIFO is overrun.	0x0
1	R/ W1C	TX_UNRUN	Tx FIFO Underrun Interrupt Asserts when the Tx FIFO is underrun.	0x0
0	R/ W1C	TX_THRES	Tx FIFO Below Threshold Interrupt Asserts when the FIFO is lower than the defined threshold.	0x0

NOTE:

Read

0: Interrupt not asserted

1: Interrupt asserted

Write

1: Clear this bit

193. INT_EN: I²S Interrupt Enable Control Register (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:9	-	-	Reserved	0x0
7	RW	RX_INT3_EN	INT_STATUS[7] Enable Enables the Rx DMA Fault Detected Interrupt. This interrupt asserts when a fault is detected in Rx DMA signals.	0x0
6	RW	RX_INT2_EN	INT_STATUS[6] Enable Enables the Rx Overrun Interrupt. This interrupt asserts when the Rx FIFO is overrun.	0x0
5	RW	RX_INT1_EN	INT_STATUS[5] Enable Enables the Rx Underrun Interrupt. This interrupt asserts when the Rx FIFO is underrun.	0x0
4	RW	RX_INT0_EN	INT_STATUS[4] Enable Enables the Rx FIFO Below Threshold Interrupt. This interrupt asserts when the Rx FIFO is lower than the defined threshold.	0x0

Bits	Type	Name	Description	Initial Value
3	RW	TX_INT3_EN	INT_STATUS[3] Enable Enables the Tx DMA Fault Detected Interrupt. This interrupt asserts when a fault is detected in Tx DMA signals.	0x0
2	RW	TX_INT2_EN	INT_STATUS[2] Enable Enables the Tx FIFO Overrun Interrupt. This interrupt asserts when the Tx FIFO is overrun.	0x0
1	RW	TX_INT1_EN	INT_STATUS[1] Enable Enables the Tx FIFO Underrun Interrupt. This interrupt asserts when the Tx FIFO is underrun.	0x0
0	RW	TX_INT0_EN	INT_STATUS[0] Enable Enables the Tx FIFO Below Threshold Interrupt. This interrupt asserts when the FIFO is lower than the defined threshold.	0x0

NOTE:

0: Disable

1: Enable

194. FF_STATUS: I²S Tx/Rx FIFO Status (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:4	RO	RX_AVCNT	Rx FIFO Available Space Count Counts the available space for reads in Rx FIFO. (unit: word)	0x0
3:0	RO	TX_EPCNT	Tx FIFO Available Space Count Counts the available space for writes in Tx FIFO. (unit: word)	0x8

195. TX_FIFO_WREG: Tx Write Data Buffer (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:0	WO	TX_FIFO_WDATA	Tx FIFO Write Data Buffer Buffers data to be written to the Tx FIFO.	0x0

196. RX_FIFO_RREG: Rx Read Data Buffer (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:0	RO	RX_FIFO_RDATA	Rx FIFO Read Data Buffer Buffers data read from the Rx FIFO.	0x0

197. I2S_CFG1: I²S Loopback Test Control Register (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31	RW	LBK_EN	Enables loopback mode. 0: Normal mode 1: Loopback mode ASYNC_TXFIFIO → Tx → Rx → ASYNC_RXFIFIO	0x0

Bits	Type	Name	Description	Initial Value
30	RW	EXT_LBK_EN	Enables external loopback. 0: Normal mode 1: Enables external loop back. External A/D → Rx → Tx → External D/A	0x0
29:0	-	-	Reserved	0x0

198. DIVCOMP_CFG: Integer Part of Divisor Register (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31	RW	CLK_EN	Enables setting of the I ² S clock based on DIVCOMP and DIVINT parameters. 0: Disable 1: Enable	0x0
30:9	-	-	Reserved	0x0
8:0	RW	DIVCOMP	A parameter in an equation which determines FREQOUT. See DIVINT_CFG.	0x0

199. DIVINT_CFG: Integer Part of Divisor Register (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:10	-	-	Reserved	0x0
9:0	RW	DIVINT	Integer Divider A parameter in an equation which determines FREQOUT: FREQOUT = FREQIN * (1/2) * {1 / [DIVINT+DIVCOMP/(512)]} FREQIN is always fixed to 40 MHz.	0x0

2.15 Memory Controller

2.15.1 Features

- 1 SDRAM/DDR2 (16 b) chip selection
- 128 MB (SDRAM)/128 MB (DDR1)/256 MB (DDR2) per chip selection
- SDRAM transaction overlapping by early active and hidden pre-charge
- User SDRAM Init commands
- 4 banks per SDRAM chip select
- SDRAM burst length: 4 (fixed)
- DDR2 burst length: 4/8 (programmable)
- Wrap-4 transfer
- Bank-Row-Column and Raw-Bank-Column address mapping

2.15.2 Block Diagram

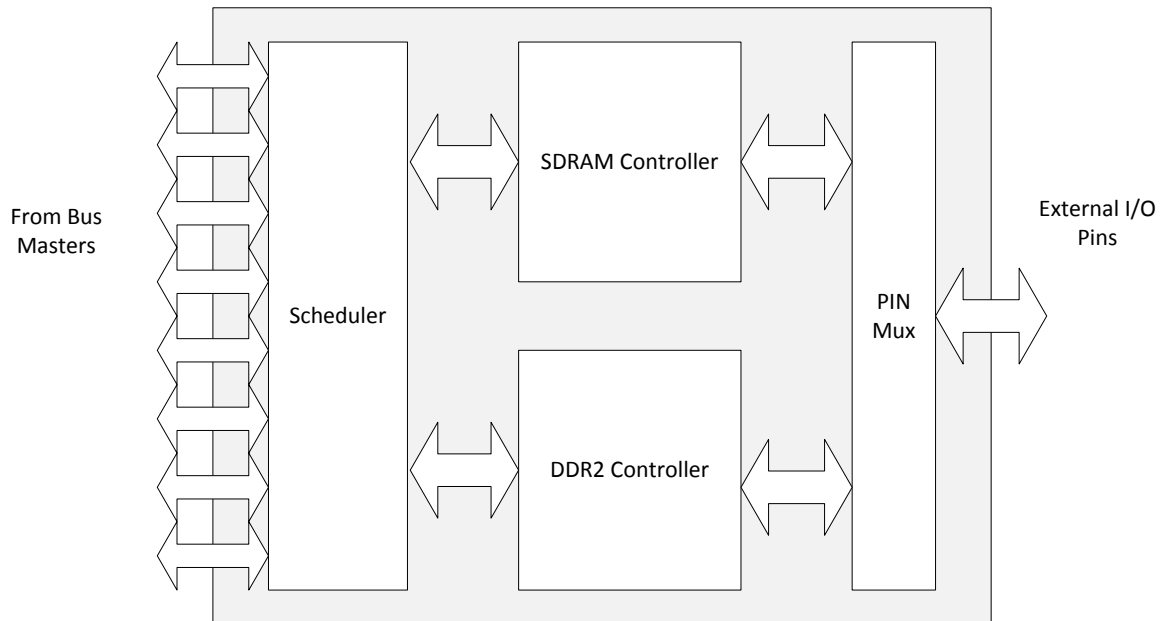


Figure 2-16 SRAM/SDRAM Controller Block Diagram

2.15.3 SDRAM Initialization Sequence

SDRAMs require an initialization sequence before they are ready for reading and writing. The initialization sequence is described below.

1. Set SDRAM related timing in SDRAM_CFG0.
2. Set SDRAM size and refresh time in SDRAM_CFG1 register with SDRAM_INIT_START = 1.
3. Read SDRAM_INIT_DONE in SDRAM_CFG1 register.
4. If SDRAM_INIT_DONE !=1, go to step 3, else the SDRAM initialization sequence is finished.

2.15.4 SDRAM Power Saving Configuration

To configure power-saving, use the registers provided for each DRAM size.

Size	DRAM width (16-bit), total bus width 16
16 Mb	SDRAM0: 0x11825282 SDRAM1: 0xFB000E7E
64 Mb	SDRAM0: 0x12825282 SDRAM1: 0xC00103A9
128 Mb	SDRAM0: 0x51B283B3 SDRAM1: 0xC01103A9
256 Mb	SDRAM0: 0x51B283B3 SDRAM1: 0xC01203A9
512 Mb	SDRAM0: 0x51B283B3 SDRAM1: 0xC02203A9
1024 Mb	N/A
2048 Mb	N/A

2.15.5 DDR Initialization Sequence

DDR devices require an initialization sequence before they are ready for re-write access. The initialization sequence is described below.

1. Wait for 200 μ s to set bit[10] to 0 in address 0x1000_0034.
2. Read bit[21] of DDR_CFG1 and wait for it to become 1.
3. Set DDR size and data width in DDR_CFG1 (Please refer to the table).

For DDR Performance, follow the settings provided in these two tables for DDR_CFG0 and DDR_CFG1 according to their DDR sizes. The tables are based on a DDR frequency of 193 MHz.

DDR1: DDR_CFG0/1

DDR SIZE	WIDTH	Total Width	DDR_CFG0 (trFC/trEFI)	DDR_CFG1	MT7620N (DRQFN)	MT7620A (TFBGA)5
64 Mb	16	16	32'h34A1EB59	32'h20262324	V	V
128 Mb	16	16	32'h34A1EB59	32'h202A2324	V	V
256 Mb	16	16	32'h34A1E5AC	32'h202E2324	V	V
512 Mb	16	16	32'h3421E5AC	32'h20322324	V	V
1 Gb	16	16	32'h241B05AC	32'h20362334		V

DDR2: DDR_CFG0/1

DDR SIZE	WIDTH	Total Width	DDR_CFG0 (trFC/trEFI)	DDR_CFG1	MT7620N (DRQFN)	MT7620A (TFBGA)
128 Mb	16	16	32'h2499E5AC	32'h222A2323	V	V
256 Mb	16	16	32'h2519E2D6	32'h222e2323	V	V
512 Mb	16	16	32'h249AA2D6	32'h22322323	V	V
1 Gb	16	16	32'h249B22D6	32'h22362323		V
2 Gb	16	16	32'h249CE2D6	32'h223A2323		V

DDR1: DDR_CFG2: 32'h28000033

DDR2: DDR_CFG2: 32'h68000C43

DDR1: DDR_CFG3: 32'h00000002

DDR2: DDR_CFG3: 32'h00000416

DDR1:DDR_CFG4:32'h00000000

DDR2:DDR_CFG4:32'h0000000A

2.15.6 List of Registers

No.	Offset	Register Name	Description	Page
200	0x0000	SDRAM_CFG0	SDRAM Configuration 0	163
201	0x0004	SDRAM_CFG1	SDRAM Configuration 1	163
202	0x0008	TCH_ARB_CFG	Two Channel Arbiter Configuration	165
203	0x0010	ILL_ACC_ADDR	Illegal Access Address Capture	165
204	0x0014	ILL_ACC_TYPE	Illegal Access Type Capture	165
205	0x0018	DDR_SELF_REFRESH	DDR Self Refresh	166
206	0x001C	SDR_DDR_PWR_SAVE_CNT	SDR DDR Power Save Counter	167
207	0x0020 to 0024	Reserved	-	168
208	0x0040	DDR_CFG0	DDR Configuration 0	168
209	0x0044	DDR_CFG1	DDR Configuration 1	169
210	0x0048	DDR_CFG2	DDR Configuration 2	171
211	0x004C	DDR_CFG3	DDR Configuration 3	173
212	0x0050	DDR_CFG4	DDR Configuration 4	174
213	0x0054 to 005C	Reserved	-	174
214	0x0060	DDR_CFG8	DDR Configuration 8	175
215	0x0064	DDR_CFG9	DDR Configuration 9	175
216	0x0068	DDR_CFG10	DDR Configuration 10	175
217	0x006C	DDR_CFG11	DDR Configuration 11	176

2.15.7 Register Descriptions (base: 0x1000_0300)

200. SDRAM_CFG0: SDRAM Configuration 0 (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31	RW	DIS_CLK_GT	Disable Clock Gating Disables clock gating of the SDR DRAM controller. 0: Enable 1: Disable	0x0
30:29	-	-	Reserved	0x0
28	RW	TWR	Write Recovery Time (unit: system clock cycles – 1)	0x1
27:24	RW	TMRD	Load Mode Register command to any other command delay. (unit: system clock cycles – 1)	0x01
23:20	RW	TRFC	Auto Refresh period (unit: system clock cycles – 1)	0x9
19:18	-	-	Reserved	0x0
17:16	RW	TCAS	CAS Latency Time (unit: system clock cycles – 1)	0x2
15:12	RW	TRAS	The Active To Precharge command delay. (unit: system clock cycles – 1)	0x5
11:10	-	-	Reserved	0x0
9:8	RW	TRCD	Active To Read or Write delay (RAS to CAS delay) (unit: system clock cycles – 1)	0x2
7:4	RW	TRC	Active To Active command period (unit: system clock cycles – 1)	0x8
3:2	-	-	Reserved	0x0
1:0	RW	TRP	Precharge command period (unit: system clock cycles – 1)	0x2

NOTE: For more information on SDRAM timing, see the vendor datasheet supplied.

201. SDRAM_CFG1: SDRAM Configuration 1 (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31	RW	SDRAM_INIT_START	SDRAM Initialization Start Performs the SDRAM initialization sequence. Can not set this bit to 0 after initialization. 1: Start initialization	0x0
30	RO	SDRAM_INIT_DONE	SDRAM Initialization Done Indicates the SDRAM has been initialized. 0: Not initialized. 1: Initialized.	0x0

Bits	Type	Name	Description	Initial Value
29	RW	RBC_MAPPING	RBC Mapping Selects the address mapping scheme. 0: {BANK ADDR, ROW ADDR, COL ADDR} address mapping scheme 1: {ROW ADDR, BANK ADDR, COL ADDR} address mapping scheme	0x0
28	RW	PWR_DOWN_EN	Power Down Enable Enables the SDRAM precharge power-down mode to save standby power. 0: Disable 1: Enable	0x0
27	RW	PWR_DOWN_MODE	Power Down Mode 0: Precharge power down mode 1: Active power down	0x0
26:25	-	-	Reserved	0x0
24	RW	SDRAM_WIDTH	SDRAM Width Selects the number of SDRAM data bus bits. 0: 16 bits 1: 32 bits	0x1
23:22	-	-	Reserved	0x0
21:20	RW	NUMCOLS	Number of Columns Selects the number of column address bits. 0: 8 Column address bits 1: 9 Column address bits (default) 2: 10 Column address bits 3 11 Column address bits	0x1
19:18	-	-	Reserved	0x0
17:16	RW	NUMROWS	Number of Rows Selects the number of row address bits. 0: 11 Row address bits 1: 12 Row address bits (default) 2: 13 Row address bits 3: 14 Row address bits	0x2
15:0	RW	TREFR	AUTO REFRESH period (unit: SDRAM clock cycles – 1).	0x600

NOTE: SDRAM Self Refresh Mode and Power Down will be supported later.

202. TCH_ARB_CFG: (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	PREEMPT_EN	Preemption Enable Requests preemption. A higher priority requestor may interrupt a lower priority channel. 0: Disable 1: Enable	0x1
25:0	-	-	Reserved	0x0

203. ILL_ACC_ADDR: Illegal Access Address Capture (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:0	RO	ILL_ACC_ADDR	Illegal Access Address If any bus masters (including CPU) issue illegal accesses (e.g. accesses to reserved memory space, or non-double-word accesses to configuration registers), the address of the illegal transaction is captured in this register. An illegal interrupt is generated to indicate this exception.	0x0

204. ILL_ACC_TYPE: Illegal Access Type Capture (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31	W1C	ILL_INT_STATUS	Illegal Access Interrupt Status Indicates whether the illegal access interrupt is cleared or pending. <i>Read</i> 0: Cleared 1: Pending <i>Write</i> 1: Clear both the ILL_ACC_ADDR and ILL_ACC_TYPE registers and thus clear ILL_INT_STATUS.	0x0
30	RO	ILL_ACC_WR	Illegal Access Write Indicates the illegal access is a read or a write. 0: A read access 1: A write access	0x0
29:20	-	-	Reserved	0x0
19:16	RO	ILL_ACC_BSEL	Illegal Access Byte Select Indicates which bytes were illegally accessed.	0x0
15:11	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
10:8	RO	ILL_IID	Illegal Access Initiator ID Indicates the initiator ID of the illegal access. 0: CPU 1: DMA 2: PPE 3: Ethernet PDMA Rx 4: Ethernet PDMA Tx 5: PCI/PCIE 6: Embedded WLAN MAC/BBP 7: USB	0x0
7:0	RO	ILL_ACC_LEN	Illegal Access Length Indicates the access size of the illegal access. (unit: bytes)	0x0

NOTE: Except for ILL_INT_STATUS, these interrupts are reset to 0 when ILL_ACC_ADDR is written.

205. DDR_SELF_REFRESH: (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:24	RW	ODT_SRC_SEL	ODT Source Select Sets the DDR pad ODT control source. 0: Dasavtive[0] 1: Dasavtive[1] ... 11: Dasavtive[11] 12: DQS_WINDOW 13: ODT_LOCAL 14: Always on 15: Always off	0xE
23:20	RW	ODT_OFF_DLY	ODT Off Delay Sets the delay time of the ODT_OFF signal based on the ODT_ON signal. 0: 0 T 1: 0.5 T 2: 1.5 T 3: 2.5 T ... 15: 14.5 T	0x1
19:16	RW	ODT_ON_DLY	ODT On Delay Sets the delay time of the ODT_ON signal based on the ODT source signal. 0: 0 T 1: 1 T 2: 2 T ... 15: 15 T	0x2
15:5	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
4	RW	SR_AUTO_EN	Auto Self-Refresh Enable Enables auto self-refresh for power saving. 0: Disable 1: Enable	0x0
3:2	-	-	Reserved	0x0
1	RO	SRACK_B	Self-Refresh Acknowledge Status Indicates whether DDR2 is in self-refresh mode or has exited from self-refresh mode. When DDR2 changes from self-refresh mode to normal mode, it takes about 200 clock cycles. 0: The DDR2 is in self-refresh mode. 1: The DDR2 has exited from self-refresh mode.	0x1
0	RW	SRREQ_B	Self-Refresh Request Control Requests DDR2 to enter or exit self-refresh mode. It is low active. 0: Enter self-refresh mode. 1: Exit self-refresh mode.	0x1

206. SDR_DDR_PWR_SAVE_CNT: (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:24	RO	PD_CNT	Power Down Count Counts the times self-refresh mode is entered (only for DDR2)	0x0

Bits	Type	Name	Description	Initial Value
23:0	RW	SR_TAR_CNT	Self-Refresh Time Count This counter is only referenced when the SDR (PWR_DOWN_EN) or DDR2 (SR_AUTO_EN) is set. This counter measures the period SDR or DDR2 is in IDLE status. When the IDLE period has reached the specified time period, the SDR or DDR2 automatically enter power-saving or self-refresh mode. Use the following equations to configure the counter. DRAM_CLK_FREQ is PLL_CLK (384 MHz or 400 MHz) divided by 3 DDR2: $(SR_TAR_CNT * 256 + 255) / DRAM_CLK_FREQ$ SDR: $(SR_TAR_CNT * 256) / DRAM_CLK_FREQ$ SDRAM reference table 166 MHz: $24'h03FFFF * 256 * 6.02\ ns \approx 404\ ms$ 160 MHz: $32'h03FFFF * 256 * 6.25\ ns \approx 419\ ms$ 125 MHz: $32'h03FFFF * 256 * 8.0\ ns \approx 536\ ms$	0x3FFFF

207. Reserved: (offset: 0x0020 to 0024)

208. DDR_CFG0: (offset: 0x0040)

Bits	Type	Name	Description	Initial Value
31:28	RW	Active-to-Active delay of different banks	The minimum number of clock cycles from an active command to the next active command for different banks (T_{RRD}). For DDR2 devices, this is required to be a minimum of 2 regardless of the cycle time.	0x2
27:23	RW	Active to Pre- charge time	The number of clock cycles from an active command until a pre-charge command is allowed. To obtain this value, one should divide the minimum RAS# to pre-charge delay of the SDRAM by the clock cycle time (T_{RAS}). The sum of Active-to-Pre-charge and Pre-charge-to-Active should be equal or larger than active-to-active delay of the same ban (T_{RC})	0x9

Bits	Type	Name	Description	Initial Value
22:19	RW	Pre-charge to Active command time	The number of clock cycles needed for the SDRAM to recover from a pre-charge command and ready to accept the next active command. To obtain this value, one should divide the RAS# pre-charge time of the SDRAM (T_{RP}) by the clock cycle time. The sum of Active-to-Pre-charge and Pre-charge-to-Active should be equal or larger than active-to-active delay of the same bank (T_{RC})	0x3
18:13	RW	Refresh to Refresh or Active command delay	Half the number of clock cycles needed for the SDRAM to recover from a refresh signal to be ready to take the next command. To obtain this value, one should divide the SDRAM row cycle time (T_{RFC}) by the clock cycle time.	0x1A
12:0	RW	Refresh Interval	The number of clock cycles from one refresh command to the next refresh command. To obtain this value, one should divide the periodic refresh interval (T_{REFI}) by the clock cycle time. The actual timing of issuing a pre-charge command may be delayed by if the SDRAM is processing a normal access. However, the delay is not accumulative so there is no need to shorten the refresh interval to account for memory access time. The non-accumulative refresh delay typically increases memory bandwidth by a few percentage points.	0x258

209. DDR_CFG1: (offset: 0x0044)

Bits	Type	Name	Description	Initial Value
31:28	RW	Write-to-Read delay	The write-to-read delay (T_{WTR}) (last write data to the next read command) as specified by the DDR2 data sheet	0x2
27:24	RW	Read-to-Pre-charge delay	The read-to-pre-charge delay (T_{RTP}) as specified by the DDR2 data sheet. Note that this is a DDR2 requirement, and requires a minimum of 2 cycles. These bits are ignored in DDR mode.	0x2
23:22	-	-	Reserved	0x0
21	RW	User data width	0: 32-bit user data width 1: 64-bit user data width When user data width is 32-bit, DDR2 width (bit[13:12]) must be 10 to indicate DDR2 data width 16. NOTE: This system is always 64-bit. Please do not modify this setting.	0x1

Bits	Type	Name	Description	Initial Value
20:18	RW	DDR2 size	000: Reserved 001: Individual DDR2 is 64 Mbit, (DDR only) 010: Individual DDR2 is 128 Mbit, (DDR only) 011: Individual DDR2 is 256 Mbit. 100: Individual DDR2 is 512 Mbit. 101: Individual DDR2 is 1 Gbit. 110: Individual DDR2 is 2 Gbit, (DDR2 only). 111: Reserved	0x3
17:16	RW	DDR2 width	00: Reserved 01: Individual DDR2 is 8-bit wide. 10: Individual DDR2 is 16-bit wide. 11: Reserved	0x2
15:14	RW	External banks	00: 1 external bank, 1 module. (CS#[0]) 01: 2 external bank, 1 module. (CS#[1:0]), 10: Reserved 11: 2 external banks, 2 modules. (CS#[1:0]) NOTE: In MT7620, there is only one CS pin.	0x0
13:12	RW	Total DDR2 data path width	This field specifies the total data width to the DDR2. For example, if four 8-bit wide DDR2 chips are used in parallel to form a 32-bit DDR2 data width, this field should be defined as 11 to indicate a 32-bit width. In this case, bit[17:16] should be defined as 01. 00: Reserved 01: Reserved 10: 16-bit 11: 32-bit. Allowed only when user data width is 64-bit (bit21 is 1).	0x2
11:8	RW	Write Recovery Time	The clock cycles needed for the DDR to recover from a write command and be able to accept a pre-charge command. To obtain this value, divide the SDRAM write recovery time by the clock cycle time (T_{WR})	0x4
7:4	RW	Mode register set to active	The number of clock cycles after the setting of the mode registers in the DDR and before the issue of the next command. To obtain this value, divide the Mode Register Set Cycle time (T_{MRD}) by the clock cycle time.	0x2
3:0	RW	RAS# to CAS# delay time	The number of clock cycles from an active command to a read/write assertion. To obtain this value, divide the RAS# to CAS# delay time (T_{RCD}) by the clock cycle time.	0x4

210. DDR_CFG2: (offset: 0x0048)

Bits	Type	Name	Description	Initial Value
31	RW	REGE	This bit should be high when external registers are inserted in the controller and address signals are sent between the controller and the DDR SDRAM. One example of such instance is when register mode SDRAM DIMM is used. This bit should be low when the control and address signals from the controller is connected to the SDRAM without register delay.	0x0
30	RW	DDR2 Mode	This bit determines whether the memory controller is in DDR1 or DDR2 mode. 0: DDR1 mode 1: DDR2 mode	0x1
29:28	RW	DQS window control for DQS0	Controls the mask for the data strobe 0 (DQS0) window leading and trailing edge. 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No extended cycle for leading and trailing edge of DQS window (minimum window)	0x0
27:26	RW	DQS window control for DQS1	Controls the mask for the data strobe 1 DQS1 window leading and trailing edge. 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No extended cycle for leading and trailing edge of DQS window (minimum window)	0x0
25:24	RW	DQS window control for DQS2	Controls the mask of data strobe 2 (DQS2) window leading and trailing edge. 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No extended cycle for leading and trailing edge of DQS window (minimum window)	0x0

Bits	Type	Name	Description	Initial Value
23:22	RW	DQS window control for DQS3	Controls the mask of data strobe 3 (DQS3) window leading and trailing edge. 00: Half extended cycle for the leading and trailing edge of DQS window (maximum window) 01: Only half extended cycle for leading edge of DQS window 10: Only half extended cycle for trailing edge of DQS window 11: No extended cycle for leading and trailing edge of DQS window (minimum window)	0x0
21:13	-	-	Reserved	0x0
12	RW	PD	Active Memory Power Down Exit Time 0: Fast exit time (T_{XARD}) 1: Slow exit time(T_{XARDS}) This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR1 SDRAM.	0x0
11:9	RW	WR	Auto Pre-charge Write Recovery (T_{DAL}) These bits must be 0 for DDR1 SDRAM.	0x2
8	RW	DLLRESET	Delay Locked Loop (DLL) Reset 0: Normal operation 1: Normal operation with DLL reset	0x0
7	RW	TESTMODE	Sets DDR to run in test mode. 0: Normal operation. 1: Test mode. The user must keep this bit at 0 if the SDRAM does not support the TESTMODE bit.	0x0
6:4	RW	CAS Latency	Specifies the number of the clock cycles from the assertion of a read/write signal to the SDRAM until the first valid data on the output from the SDRAM. The valid numbers are: 101: 1.5 for DDR1 or 5 for DDR2. 010: 2 110: 2.5 (DDR1 only) 011: 3 100: 4 (DDR2 only)	0x4
3	RO	Burst Type	This register is hardwired to 0 to indicate a sequential burst type.	0x0

Bits	Type	Name	Description	Initial Value
2:0	RW	Burst Length	Indicates the burst length of the read/write transaction. 010: 4 bursts 011: 8 bursts NOTE: 1. A burst of 4 is not allowed when user data is 64-bit while SDRAM data is 16-bit. 2. A burst of 8 is allowed in all user/SDRAM data width combination. 3. Other values for burst length are not allowed.	0x3

211. DDR_CFG3: (offset: 0x004C)

Bits	Type	Name	Description	Initial Value
31:13	-	-	Reserved	0x0
12	RW	Qoff	Output Buffer Disable 0: Enabled 1: Disabled This bit is used for DDR2 SDRAM only. This bit must be 0 for DDR1 SDRAM.	0x0
11	RW	RDQS	Redundant Data Strobe (DQS) This bit enables the redundant DQS function if supported by the SDRAM. 0: Disable 1: Enable This bit is used for DDR2 SDRAM only and must be 0 for DDR1 SDRAM.	0x0
10	RW	Differential DQS	Disables differential DQS 0: Enable 1: Disable This bit is used for DDR2 SDRAM only and must be 0 for DDR1 SDRAM.	0x1
9:7	RW	OCD	Off-Chip Driver Impedance Calibration (OCD) These bits support the OCD function if supported by the SDRAM. The value programmed in these register bits will be programmed into the SDRAM at EMR1 programming. Settings are vendor-dependant.	0x0

Bits	Type	Name	Description	Initial Value
6	RW	RTT bit 1	Internal Termination Resistor (RTT) bit 1 Used together with bit 2 (RTT0) to control On-Die Termination (ODT). Combine values for (RTT1, RTT0) to select ODT settings. 00: ODT disabled. 01: 75 ohm 10: 150 ohm 11: Reserved This bit is used for DDR2 SDRAM only and must be 0 for DDR1 SDRAM.	0x0
5:3	RW	Additive Latency	Additive Latency 000: 0 cycle 001: 1 cycle 010: 2 cycles 011: 3 cycles 100: 4 cycles 101: 5 cycles Others: Reserved This bit is used for DDR2 SDRAM only and must be 0 for DDR1 SDRAM.	0x2
2	RW	RTT bit 0	Internal Termination Resistor (RTT) bit 0 Used together with bit 6 (RTT1) to control ODT. This bit is used for DDR2 SDRAM only and must be 0 for DDR1 SDRAM.	0x0
1	RW	DS	Drive Strength 0: 100% drive strength. 1: 60% drive strength.	0x1
0	RW	DLL	Delay Locked Loop (DLL) Enable 0: Disable 1: Enable	0x0

212. DDR_CFG4: (offset: 0x0050)

Bits	Type	Name	Description	Initial Value
31:5	-	-	Reserved	0x0
4:0	RW	FAW	Four Activated Windows (FAW) Period DDR2 devices impose a restriction in that no more than 4 ACTIVE commands may be issued in a given FAW period. To obtain this value, one should divide the Four Bank Activate period (T_{FAW}) of the DDR by the clock cycle time. These bits are ignored in 4 bank devices.	0x14

213. Reserved: (offset: 0x0054 to 005C)

214. DDR_CFG8: (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:8	RW	DQ_GROUP1_DELAY_SEL	Data Output Delay Adjustment For Group1 (MD8 to MD15) 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8
7:4	-	-	Reserved	0x0
3:0	RW	DQ_GROUP0_DELAY_SEL	Data Output Delay Adjustment For Group0 (MD0 to MD7) 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8

215. DDR_CFG9: (offset: 0x0064)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:8	RW	DQS1_DELAY_SEL	Memory Data Strobe 1 (MDQS1) Input Delay Adjustment 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8
7:4	-	-	Reserved	0x0
3:0	RW	DQS0_DELAY_SEL	Memory Data Strobe 0 (MDQS0) Input Delay Adjustment 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8

216. DDR_CFG10: (offset: 0x0068)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30:28	RW	DQS1_CD_ADJ	Delay Locked Loop (DLL) Coarse-Grain Delay Adjustment for MDQS1 0x0 to 0x3: Decrease delay by 250 ps per step. 0x4: Keep DLL master delay. 0x5 to 0x7: Increase delay by 250 ps per step.	0x4
27:24	RW	DQS1_FD_ADJ	DLL Fine-Grain Delay Adjustment for MDQS1 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL master delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8
23	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
22:20	RW	DQS0_CD_ADJ	DLL Coarse-Grain Delay Adjustment for MDQS0 0x0 to 0x3: Decrease delay by 250 ps per step. 0x4: Keep DLL master delay. 0x5 to 0x7: Increase delay by 250 ps per step.	0x4
19:16	RW	DQS0_FD_ADJ	DLL Fine-Grain Delay Adjustment for MDQS0 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL master delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8
15	-	-	Reserved	0x0
14:12	RW	DQ_GROUP1_CD_ADJ	DLL Coarse-Grain Delay Adjustment for MD8 to MD15 0x0 to 0x3: Decrease delay by 250 ps per step. 0x4: Keep DLL master delay. 0x5 to 0x7: Increase delay by 250 ps per step.	0x4
11:8	RW	DQ_GROUP1_FD_ADJ	DLL Fine-Grain Delay Adjustment for MD8 to MD15 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL master delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8
7	-	-	Reserved	0x0
6:4	RW	DQ_GROUP0_CD_ADJ	DLL Coarse-Grain Delay Adjustment for MD0 to MD7 0x0 to 0x3: Decrease delay by 250 ps per step. 0x4: Keep DLL master delay. 0x5 to 0x7: Increase delay by 250 ps per step.	0x4
3:0	RW	DQ_GROUP0_FD_ADJ	DLL Fine-Grain Delay Adjustment for MD0 to MD7 0x0 to 0x7: Decrease delay by 30 ps per step. 0x8: Keep DLL master delay. 0x9 to 0xF: Increase delay by 30 ps per step.	0x8

217. DDR_CFG11: (offset: 0x006C)

Bits	Type	Name	Description	Initial Value
31	RW	DLL_MAS_RELOCK_EN	Delayed Locked Loop (DLL) Master Relock Enable 0: Disable relocking scheme. 1: Enable relocking scheme. DLL supports restarting locking from initial value if DLL is not locked after waiting 512 cycles.	0x0
30	RW	DLL_UPDATE_MODE	Sets the DLL update mode. 0: Update is delayed only when bank is activated. 1: Continuous update	0x0
29:26	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
25	RW	DLL_MAS_BYPASS_FD	DLL Bypass Fine Grain Delay 0: Fine-grain delay code is determined by DLL. 1: Fine-grain delay code is fixed by DLL_MAS_FIXED_FD.	0x0
24	RW	DLL_MAS_BYPASS_CD	DLL Bypass Coarse Grain Delay 0: Coarse-grain delay code is determined by DLL 1: Coarse-grain delay code is fixed by DLL_MAS_FIXED_CD.	0x0
23:12	-	-	Reserved	0x0
11:8	RW	DLL_MAS_FIXED_FD	DLL Fixed Fine Grain Delay Specifies the fine-grain delay. The effective range is 0 to 15. Each step is about 30 ps.	0x0
7	-	-	Reserved	0x0
6:0	RW	DLL_MAS_FIXED_CD	DLL Fixed Coarse Grain Delay Specifies the coarse-grain delay. The delay = $((x-2)/4 - 1) * 250$ ps, the effective range of x is 10 to 66.	0x0

2.16 RBUS Matrix and QoS Arbiter

2.16.1 Features

- 8 channel QoS Arbiter
- Configurable Bandwidth and Duedate for each agent
- QoS classifier can be programmed for RR, BW RR, Fixed Priority and QoS Arb

2.16.2 Block Diagram

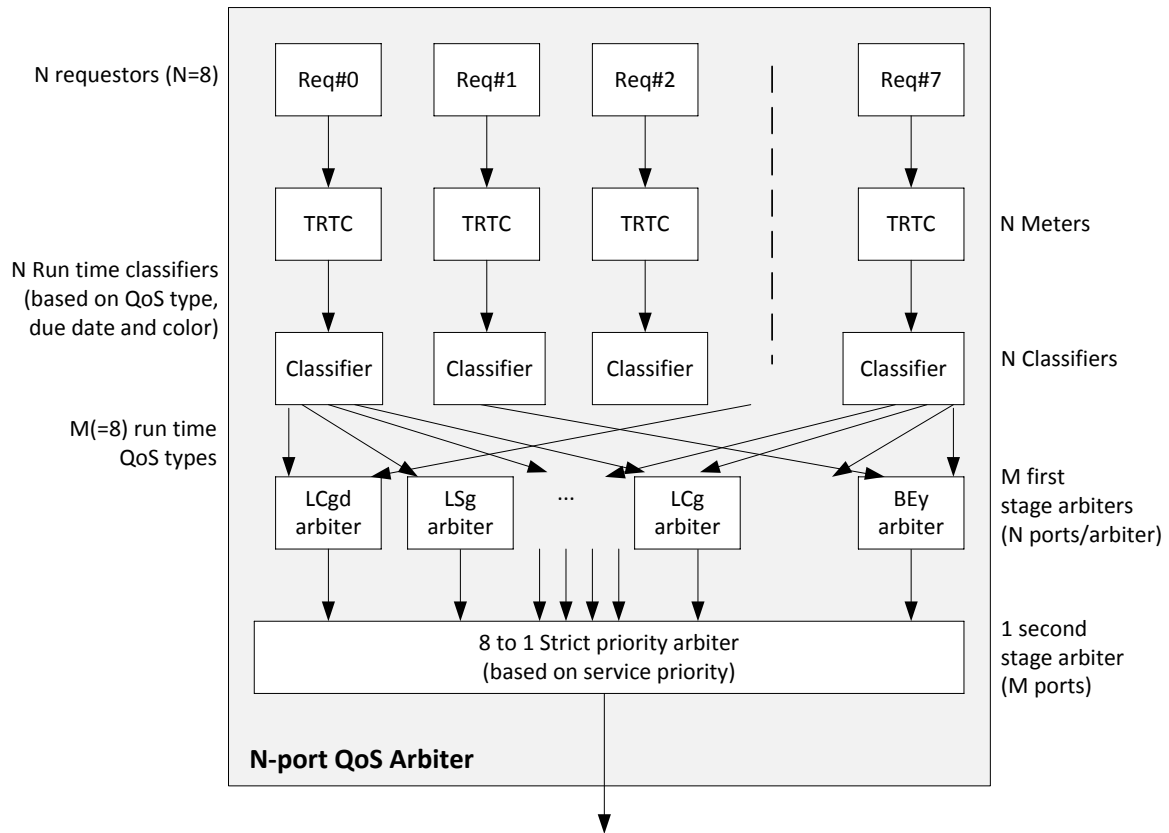


Figure 2-17 QoS Arbitration Block Diagram

2.16.3 List of Registers

No.	Offset	Register Name	Description	Page
218	0x0000	DMA_ARB_CFG	DMA Arbiter Configuration	180
219	0x0004	DMA_AG_BW	DMA Agent Bandwidth	180
220	0x0010	OCP_CFG0	OCP Configuration0	181
221	0x0014	OCP_CFG1	OCP Configuration1	182
222	0x0024	R2P_MONITOR	Rbus to Pbus Monitor	182
223	0x0028	ERR_ADDR	Rbus to Pbus ERR Address	182

2.16.4 Register Descriptions (base: 0x1000_0400)

218. DMA_ARB_CFG: (offset: 0x0000)

Bits	Type	Name	Description	Initial Value									
31:27	-	-	Reserved	0x0									
26	RW	PREEMPT_EN	Preemption Enable Request preemption, higher priority requestor may change current request transaction 0: Disable Preemption 1: Enable Preemption	0x1									
25	RW	TRTC_EN	Two Rate Three Color Bandwidth (TRTC) Meter Enable 0: Disable TRTC 1: Enable TRTC	0x0									
24	RW	CLASS_EN	QoS Classifier Enable 0: Disable CLASS 1: Enable CLASS <table><tr><td></td><td>TRTC (0)</td><td>TRTC (1)</td></tr><tr><td>CLASS (0)</td><td>Round Robin</td><td>BW RR</td></tr><tr><td>CLASS (1)</td><td>Fixed Priority</td><td>QoS Arb</td></tr></table>		TRTC (0)	TRTC (1)	CLASS (0)	Round Robin	BW RR	CLASS (1)	Fixed Priority	QoS Arb	0x0
	TRTC (0)	TRTC (1)											
CLASS (0)	Round Robin	BW RR											
CLASS (1)	Fixed Priority	QoS Arb											
23:0	RW	CLS_PRIORITY	Class Priority This field is used for class priority for second arbitration. {BEy(3'd7), LCg(3'd6), BSy(3'd5), LSy(3'd4), BEg(3'd3), BSG(3'd2), LSG(3'd1), LCGd(3'd0)}	0xfac688									

219. DMA_AG_BW: (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31	WO	AG_WR	Agent Write 0: Read 1: Write	0x0
30:28	RW	AG_NUM	DMA Agent Select Selects a DMA agent to configure. 0: SDHC 1: GDMA 2: PPE 3: GSW PDMA 4: WPDMA 5: PCIe 6: Reserved 7: USB	0x0
27:26	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
25:24	RW	AG_QOS_TYPE	Agent QoS Type 0: Latency critical 1: Latency sensitive 2: Bandwidth sensitive (default) 3: Best Effort	0x2
23:16	RW	AG_DUEDATE	Due date for latency critical agent (unit: system bus clock cycle - system bus is 200 MHz or 120 MHz depending on DRAM type.)	0x20
15:8	RW	AG_PIR	Peak Information Rate (PIR) for the Agent The PIR is greater than or equal to the CIR. Bandwidth which exceeds PIR is marked red. 0x00: 0 MB/s 0x01: 4 MB/s ... 0x80: 512 MB/s (default) ... 0xFF: 1020 MB/s (Max)	0x80
7:0	RW	AG_CIR	Committed Information Rate for the Agent Bandwidth which falls below the CIR is marked green. BW which exceeds the CIR but is below the EIR is marked yellow. 0x00: 0 MB/s 0x01: 4 MB/s ... 0x20: 128 MB/s (default) ... 0xFF: 1020 MB/s (Max)	0x20

220. OCP_CFG0: OCP Configuration0 (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	-
3	RW	SYNC_METHOD	OCP Synchronization Command Method 0: All empty (Wait until all FIFOs are empty) 1: CMD empty (Wait until the CMD FIFO is empty)	0x0
2	RW	OCP_SYNC_CMD	OCP Synchronization Command Method Enable Remaps this RD CMD to address 0x0000_0000. Initiate DRAM control before enabling this option. 0: Disable 1: Enable	0x0
1	RW	RBUS_ASYNC	Async Mode for RBUS 0: Set HW to switch between sync or async mode dynamically. 1: Force RBUS to A.sync mode.	0x0

Bits	Type	Name	Description	Initial Value
0	RW	RD_BYPASS_WR	Read Bypass Write Enable Allows read commands to bypass write commands for OCP_IF when the address does not conflict. 0: Disable 1: Enable	0x1

221. OCP_CFG1: OCP Configuration1 (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:0	RW	RD_BYPASS_WR_MASK	Mask for read bypass write address 0: No mask 1: Mask	0xFFFF_FFFF

222. R2P_MONITOR: Rbus to Pbus Monitor (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	-
16	W1C	R2P_INT_CLR	R2P Interrupt Clear Write 1 to clear this interrupt.	0x0
15:10	RO	R2P_ERR_CNT	R2P error counter	-
9:0	RW	R2P_INT_CNT	R2P Interrupt Countdown Timer Sets a delay timer which begins counting down when an R2P error is detected. When the timer reaches zero the R2P interrupt is then triggered. 10'd0: Disable R2P monitoring 10'd1: 20 μ s 10'd2: 40 μ s 10'd1023: 40 ms	0x1023

223. ERR_ADDR: Rbus to Pbus ERR Address (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:0	RO	R2P_ERR_ADDR	R2P address record for previous error found	0x0

2.17 USB Host Controller & PHY

2.17.1 Features

- Complies with the USB 2.0 Specifications
- Complies with Host Controller Interface (OHCI) Specifications, Version 1.0a.
- Supports ping and split transactions
- Descriptor and data prefetching.
- Complies with Enhanced Host Controller Interface (EHCI) Specifications, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

2.17.2 Block Diagram

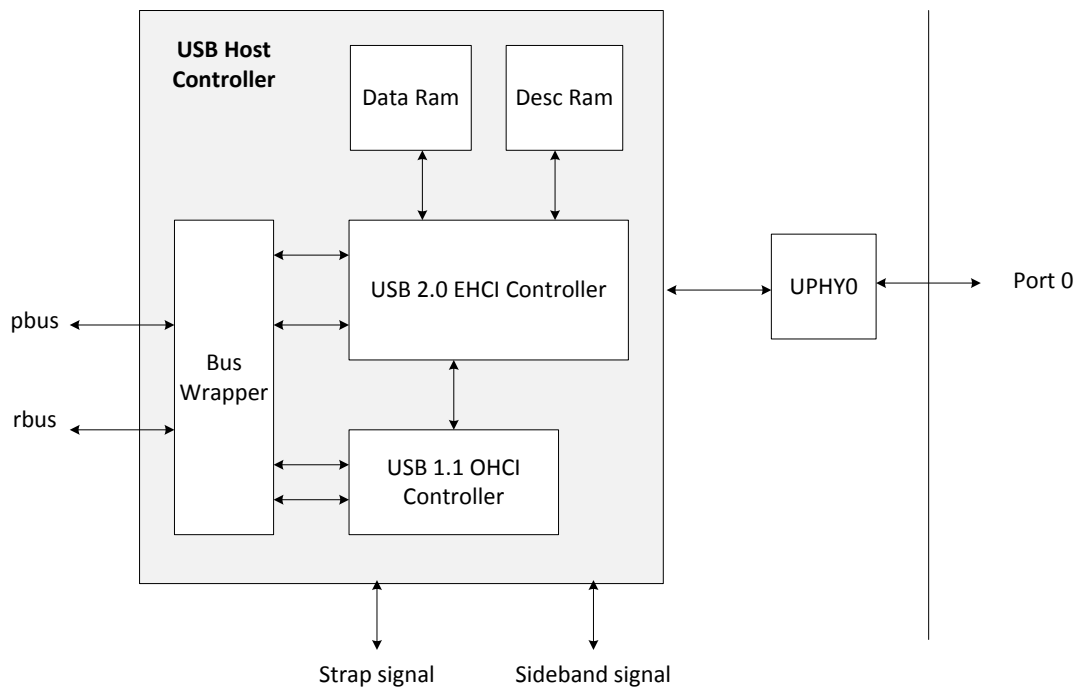


Figure 2-18 USB Host Controller & PHY Block Diagram

2.17.3 Register Description (base: 0x101C.0000)

NOTE: To program EHCI and OHCI registers and initialize the core, refer to the Enhanced Host Controller Interface Specification for Universal Serial Bus and Open Host Controller Interface Specification for USB, respectively.

2.17.4 EHCI Operation Registers (base: 0x101C.0000)

2.17.4.1 EHCI Capability Register

Mnemonic	Register Name	Offset from EHCI AHB Slave Start Address	Default Value
HCCAPBASE	Capability Register	USBBASE + 00h (see NOTE 1)	32'h01000010
HCSPARAMS	Structural Parameter	USBBASE + 04h	32'h00001116
HCCPARAMS	Capability Parameter	USBBASE + 08h	32'h0000A010 (see NOTE 2)

NOTE:

1. USBBASE is fixed to the EHCI slave start address = 0x101C.0000
2. The isochronous Scheduling Threshold value is set to 1 by default. If Descriptor/Data Prefetch is selected, the value is set to 2.

2.17.4.2 EHCI Operational Registers

Mnemonic	Register Name	Offset from EHCI AHB Slave Start Address	Default Value
USBCMD	USB Command	USBOPBASE + 00h (see NOTE 1)	32'h00080000 or 32'h00080B00 (see NOTE 2)
USBSTS	USB Status	USBOPBASE + 04h	32'h00001000
USBINTR	USB Interrupt Enable	USBOPBASE + 08h	32'h00000000
FRINDEX	USB Frame Index	USBOPBASE + 0Ch	32'h00000000
CTRLDSSEGMENT	4G Segment Selector	USBOPBASE + 10h	32'h00000000
PERIODICLISTBASE	Periodic Frame List Base Address Register	USBOPBASE + 14h	32'h00000000
ASYNCLISTADDR	Asynchronous List Address	USBOPBASE + 18h	32'h00000000

NOTE:

1. USBOPBASE is fixed to the EHCI slave start address + 'h10 (offset = 'h10).
2. The default value depends on whether Async park capability is enabled (through coreConsultant). Disabled = 32'h0008_0000 and enabled = 32'h0008_0B00.

2.17.4.3 EHCI Auxiliary Power Well Registers

Mnemonic	Register Name	Offset from EHCI AHB Slave Start Address	Default Value
CONFIGFLAG	Configured Flag Register	USBOPBASE + 40h	32'h00000000
PORTSC_1 to PORTSC_15	Port Status/Control	USBOPBASE + 44h	32'h00002000

2.17.5 OHCI Operation Registers (base: 0x101C.1000)

Offset	31	00
0	HcRevision	
4	HcControl	
8	HcCommandStatus	
C	HcInterruptStatus	
10	HcInterruptEnable	
14	HcInterruptDisable	
18	HcHCCA	
1C	HcPeriodCurrentED	
20	HcControlHeadED	
24	HcControlCurrentED	
28	HcBulkHeadED	
2C	HcBulkCurrentED	
30	HcDoneHead	
34	HcFmInterval	
38	HcFmRemaining	
3C	HcFmNumber	
40	HcPeriodicStart	
44	HcLSThreshold	
48	HcRHDescriptor A	
4C	HcRhDescriptor B	
50	HcRhStatus	
54	HcRhPortStatus[1]	
...	...	
54+4*NDP	HcRhPortStatus[NDP]	

2.18 USB Device Controller

2.18.1 Features

- Supports the USB 2.0 Specification (Revision 1.0a), operates in High-Speed (HS, 480 Mbps)
- Supports up to 2 bulk-in and 2 bulk-out endpoints, and including control endpoint 0.
- Packet DMA (PDMA) is integrated for efficient data transfer.
- Supports bulk-out aggregation features. More than one packet can be aggregated to single bulk transfer.
- Supports two Rx descriptor rings and two Tx descriptor rings for QoS service.

2.18.2 Block Diagram

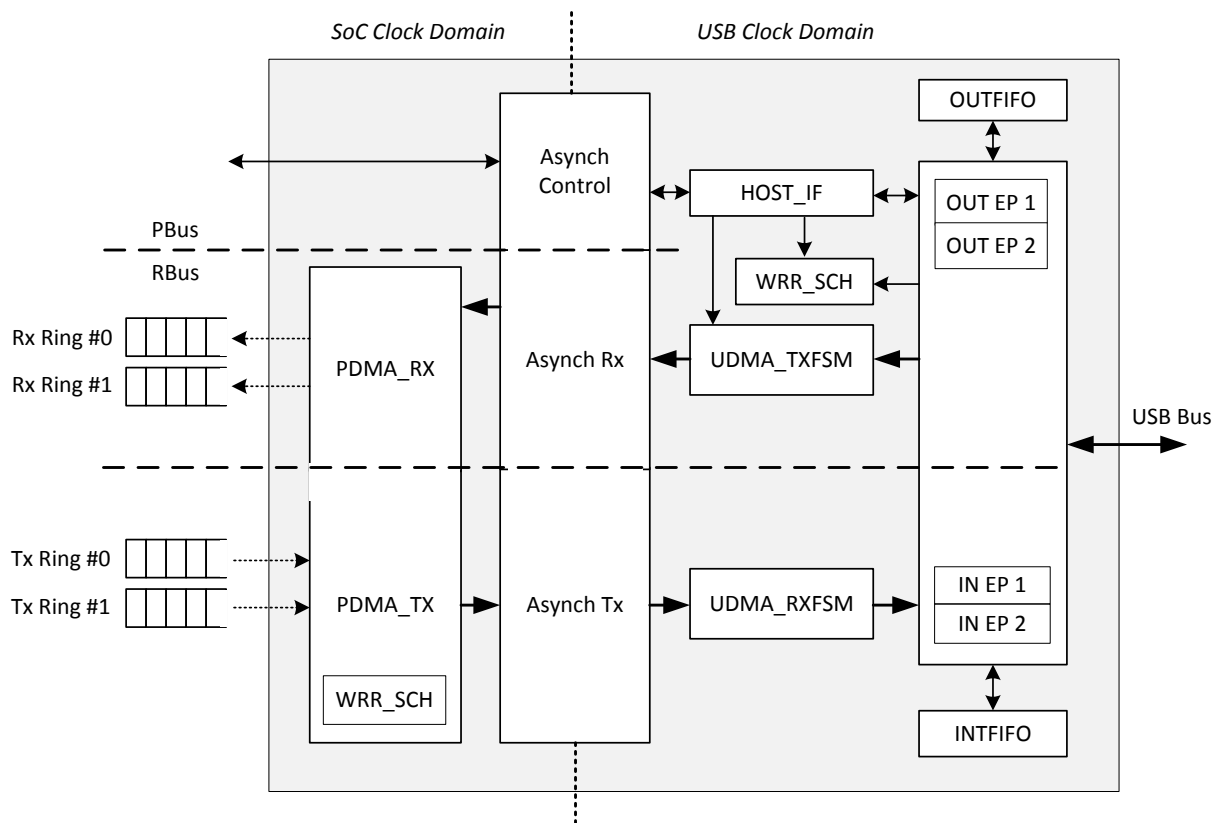


Figure 2-19 USB Device Controller Block Diagram

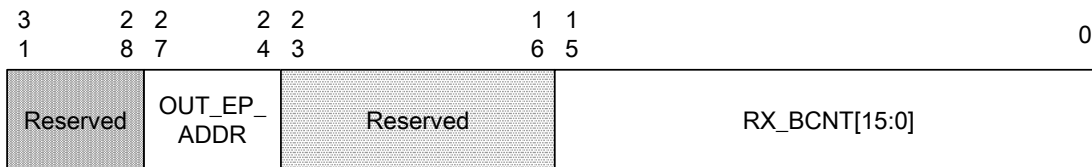
2.18.3 Bulk Out

USB device core supports two modes in BULK_OUT direction. These are aggregation mode and legacy mode, and are controlled by register EPOUT_AGGEN (UDMA_CTRL[20:16]).

2.18.4 Legacy Mode

USB device core operates in legacy mode when EPOUT_AGGEN = 0. In this mode, Host driver does not need to do anything but send a non-full bulk as the end of a packet. On PDMA side, 4 bytes of PDMA_RX_INFO will be added at the beginning of received packets to indicate the actual received byte count.

PDMA_RX_INFO



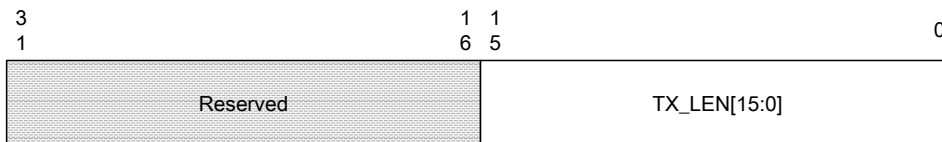
OUT_EP_ADDR: OUT endpoint address

RX_BCNT[15:0]: Received byte count.

2.18.5 Aggregation Mode

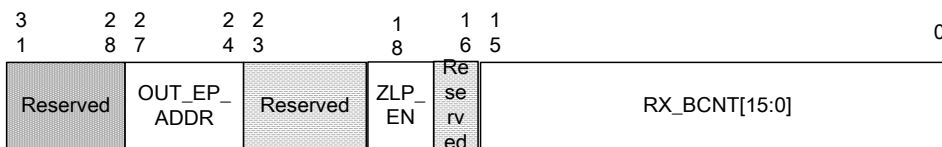
USB device core operates in aggregation mode when EPOUT_AGGEN = 1. In this mode, the host driver has to add four bytes header to specify the next aggregated packet length, then UDMA_TXFSM will de-aggregate packets automatically. In addition, the host driver has to pad the packet length to multiples of four bytes. After the last aggregated packet, the host driver needs to add 4 bytes of zeroes to indicate the packet is the last. Regarding the PDMA, packets will be de-aggregated automatically and added with PDMA_RX_INFO to indicate the received packet length.

USB_TX_INFO (EPOUT de-aggregation enabled)



TX_LEN[15:0]: Next aggregated Tx packet length

PDMA_RX_INFO



OUT_EP_ADDR: OUT endpoint address

RX_BCNT[15:0]: Received byte count.

2.18.6 De-Aggregation Mode

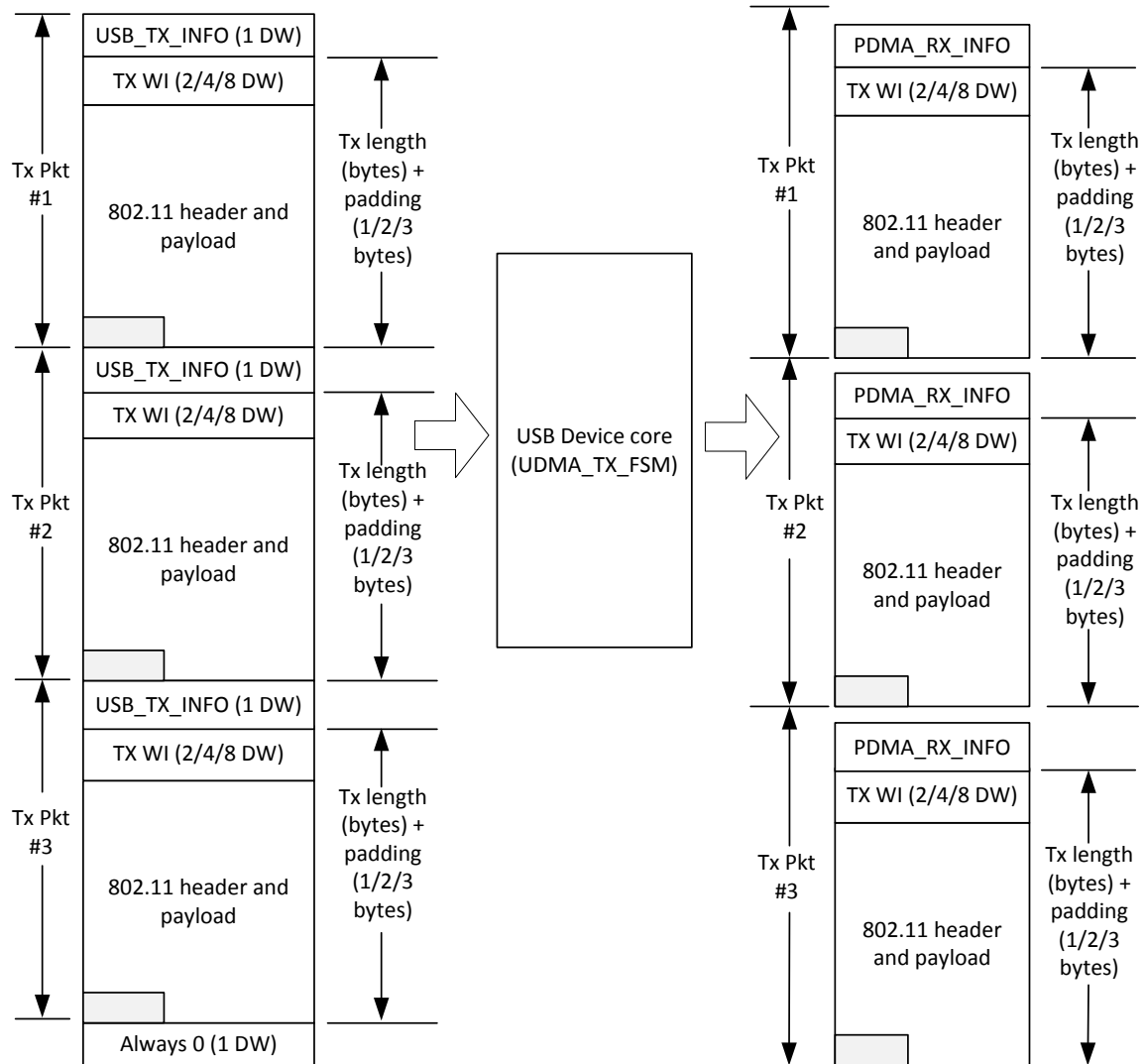
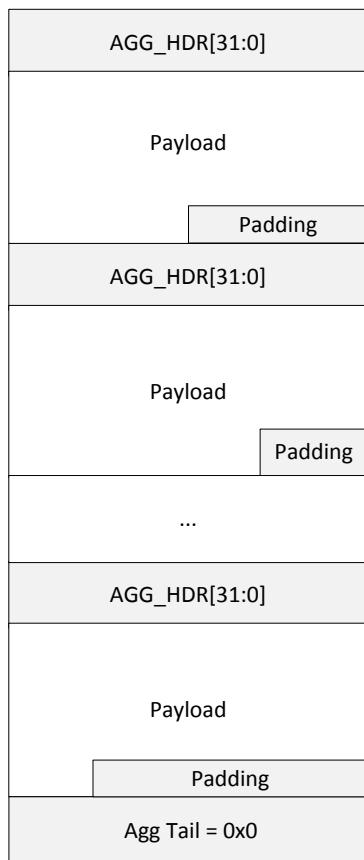


Figure 2-20 De-aggregation Flow

Please note that in both modes, PDMA may transfer more bytes than RX_BCNT. On chip F/W should take the RX_BCNT in PDMA_RX_INFO as the actual received packet length.

2.18.7 Bulk-out Aggregation Format



AGG_HDR[31:0]
AGG_HDR[31:16] reserved;
AGG_HDR[15:0] payload_length;

NOTE:

- 1) Each aggregation frame should add padding to align with the 4-byte boundary.
- 2) The payload_length indicates the length of payload (padding not included).

Figure 2-21 Bulk-out Aggregation Format

2.18.8 Bulk IN

In BULK_IN direction, only legacy mode is supported by USB device core. H/W does nothing but to send the packets from PDMA to host.

2.18.9 PDMA Descriptor Format

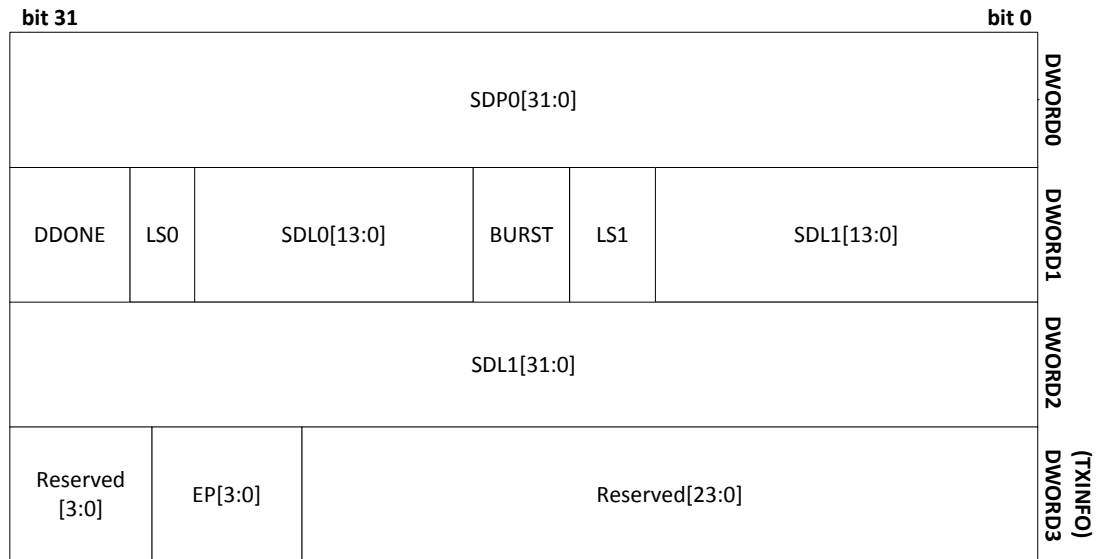


Figure 2-22 PDMA Tx Descriptor Format

The following is a detailed description of each field in the PDMA TXD.

2.18.9.1 PDMA Tx Field Descriptions

Bit	Name	Description
DWORD0		
31:0	SDP0	Segment Data Pointer0
DWORD1		
31	DDONE	DMA Done: Indicates DMA has transferred the segment pointed to by this Tx descriptor.
30	LS0	Last Segment0: Data pointed to by SDP0 is the last segment.
29:16	SDL0	Segment Data Length0: Segment data length for the data pointed to by SDP0.
15	BURST	When set, the scheduler cannot hand over to other Tx queues. Should not transmit the next packet.
14	LS1	Last Segment1: Data pointed to by SDP1 is the last segment.
13:0	SDL1	Segment Data Length1: Segment data length for the data pointed to by SDP1.
DWORD2		
31:0	SDP1	Segment Data Pointer1
DWORD3 (TXINFO)		
31:28	-	Reserved
24:27	EP	End Point: Indicates the endpoint that issues this packet.
23:0	-	Reserved

2.18.9.2 PDMA Rx Descriptor Format

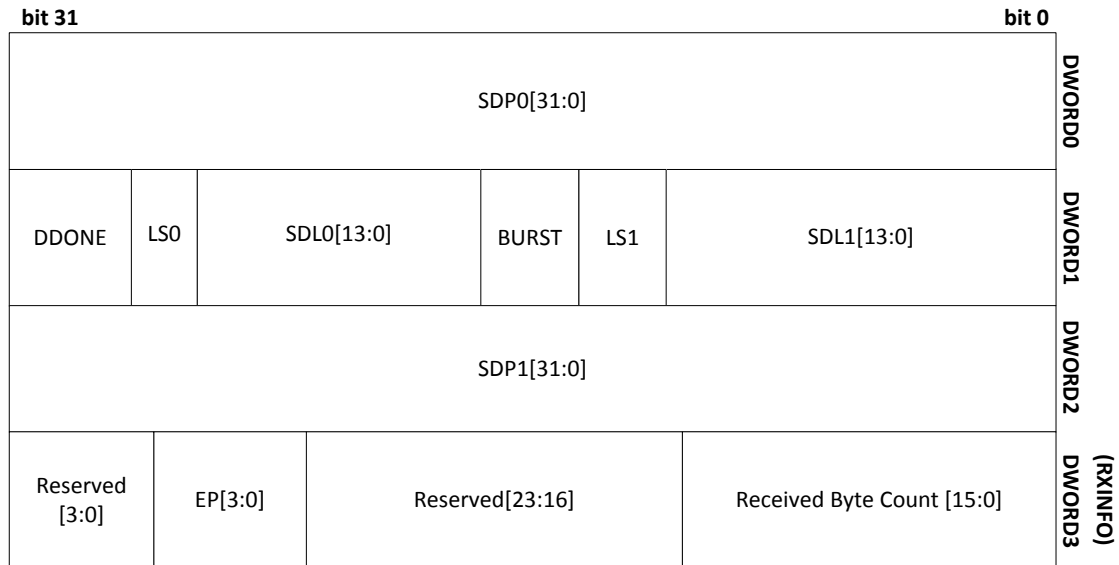


Figure 2-23 PDMA Rx Descriptor Format

The following is a detailed description of each field in the PDMA RXD.

Bit	Name	Description
DWORD0		
31:0	SDP0	Segment Data Pointer0
DWORD1		
31	DDONE	Indicates DMA has transferred the segment pointed to by this Rx descriptor.
30	LS0	Last Segment0: Data pointed to by SDP0 is the last segment.
29:16	SDL0	Segment Data Length0: Segment data length for the data pointed to by SDP0.
15	BURST	When set, the scheduler can not hand over to other Tx queues. Should not transmit the next packet.
14	LS1	Last Segment1: Data pointed to by SDP1 is the last segment.
13:0	SDL1	Segment Data Length1: Segment data length for the data pointed to by SDP1.
DWORD2		
31:0	SDP1	Segment Data Pointer1
DWORD3 (RXINFO)		
31:28	-	Reserved
24:27	EP	Indicates the endpoint that issues this packet.
23:16	-	Reserved
15:0	Received Byte Count	Indicates the number of bytes received in this packet.

Table 2-2 PDMA Rx Field Descriptions

2.18.10 Register Descriptions (base: 0x1012_0000)

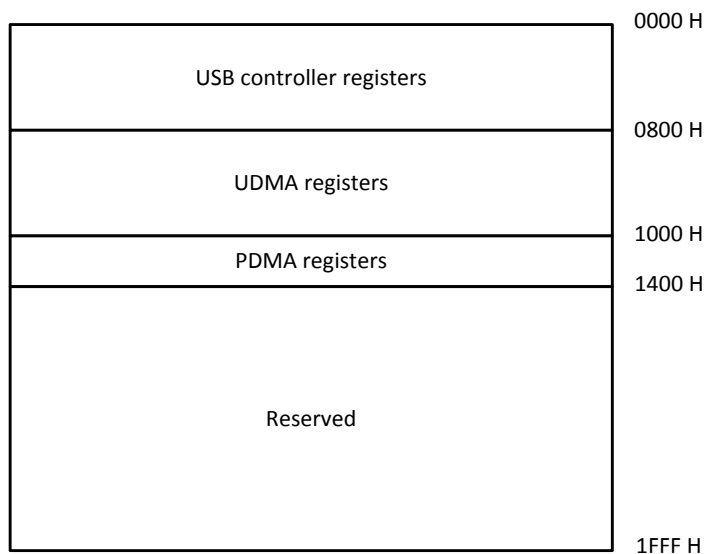


Figure 2-24 USB Device Register Mapping

2.18.11 USB Device Controller Registers

Refer to CAST CUSB2 Core USB2.0 function controller technical specification.
Register address = Byte address * 4.

2.18.12 UDMA Registers

224. UDMA_CTR: (offset: 0x0800, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:26	-	-	Reserved	
25	RW	EPOUT1_DMAEN	Enables EPOUT1 UDMA.	0
24	RW	EPOUT0_DMAEN	Enables EPOUT0 UDMA.	0
23:18	-	-	Reserved	
17	RW	EPOUT1_AGGEN	Enables EPOUT1 UDMA De-aggregation.	0
16	RW	EPOUT0_AGGEN	Enables EPOUT0 UDMA De-aggregation.	0
15:10	-	-	Reserved	-
9	RW	EPOUT1_QSEL	EPOUT1 Rx ring mapping	0
8	RW	EPOUT0_QSEL	EPOUT0 Rx ring mapping	0
7	-	-	Reserved	-
6	RW	TX_NOT_WAIT_ZLP	Sets Tx DMA to not wait until a zero length packet is sent before combining packets.	0
5	RW	RX_DIS_AUTO_ZLP	Disable the Rx AUTO ZLP function. 0: Enable 1: Disable	0
4	RW	WAKEUP_EN	Enables the USB Wakeup Host.	0
3:2	-	-	Reserved	0
1	RW	UDMA_RX_EN	Enables UDMA Rx.	0
0	RW	UDMA_TX_EN	Enables UDMA Tx.	0

NOTE: Where applicable,
0: Disable
1: Enable

225. UDMA_WRR: (offset: 0x0804, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	-
29:28	RW	SCH_MODE	Scheduling Mode 00: WRR 01: Strict priority, EP1 > EP2 > EP3 > EP4 > EP5 > EP6 10: Mixed mode, EP1 > EP2 > WRR (EP3, EP4, EP5, EP6)	0
27:7	-	-	Reserved	-
6:4	RW	SCH_WT_EP2	Scheduling weight of EPOUT2	0
3	-	-	Reserved	-
2:0	RW	SCH_WT_EP1	Scheduling weight of EPOUT1	0

2.18.13 PDMA Registers

2.18.13.1 List of Registers

No.	Offset	Register Name	Description	Page
226	0x1000, 0x1010	TX_BASE_PTRn	Tx Ring n Base Address Pointer	195
227	0x1004, 0x1014	TX_MAX_CNTn	Tx Ring n Maximum Count	195
228	0x1008, 0x1018	TX_CTX_IDXn	Tx Ring n CPU TXD Index	195
229	0x100C, 0x101C	TX_DTX_IDXn	Tx Ring n DMA TXD Index	195
230	0x1100, 0x1110	RX_BASE_PTRn	Rx Ring n Base Address Pointer	195
231	0x1104, 0x1114	RX_MAX_CNTn	Rx Ring n Maximum Count	195
232	0x1108, 0x1118	RX_CALC_IDXn	Rx Ring n CPU Allocate RXD Index	195
233	0x110C, 0x111C	RX_DRX_IDXn	Rx Ring n DMA RXD Index	196
234	0x1200	PDMA_INFO	PDMA Information	196
235	0x1204	PDMA_GLO_CFG	PDMA Global Configuration	196
236	0x1208	PDMA_RST_IDX	PDMA Reset Index	197
237	0x120C	DELAY_INT_CFG	Delay Interrupt Configuration	198
238	0x1210	FREEQ_THRES	Free Queue Threshold	199
239	0x1220	INT_STATUS	Interrupt Status	199
240	0x1228	INT_MASK	Interrupt Mask	200

2.18.13.2 Register Descriptions

226. TX_BASE_PTRn: (offset: 0x1000, 0x1010) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:0	RW	TX_BASE_PTRn	Tx Base Pointer n Points to the base address of TX_Ring n (4-DWORD aligned address).	0

227. TX_MAX_CNTn: (offset: 0x1004, 0x1014) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RW	TX_MAX_CNTn	Tx Maximum TXD Count n The maximum TXD count in TXD_Ring n.	0

228. TX_CTX_IDXn: (offset: 0x1008, 0x1018) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RW	TX_CTX_IDXn	Tx CPU TXD Index n Points to the next TXD to be used by the CPU.	0

229. TX_DTX_IDXn: (offset: 0x100C, 0x101C) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RO	TX_DTX_IDXn	Tx DMA TXD Index n Points to the next TXD to be used by the DMA.	0

230. RX_BASE_PTRn: (offset: 0x1100, 0x1110) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:0	RW	RX_BASE_PTRn	Rx Base Pointer n Points to the base address of RXD Ring n (GE ports). It should be a 4-DWORD aligned address.	0

231. RX_MAX_CNTn: (offset: 0x1104, 0x1114) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RW	RX_MAX_CNTn	Rx Maximum Count n The maximum RXD count in RXD Ring n.	0

232. RX_CALC_IDXn: (offset: 0x1108, 0x1118) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
11:0	RW	RX_CALC_IDXn	Rx CPU RXD Index n Points to the next RXD the CPU will allocate to RXD Ring n.	0

233. RX_DRX_IDXn: (offset: 0x110C, 0x111C) (n=0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	
11:0	RW	RX_DRX_IDXn	Rx DMA RXD Index n Points to the next RXD that the DMA will use in FDS Ring 0. It should be a 4-DWORD aligned address.	0

234. PDMA_INFO: (offset: 0x1200)

Bits	Type	Name	Description	Initial Value
31:28	RO	VERSION	PDMA Controller Version	2
27:24	RO	INDEX_WIDTH	Ring Index Width	12
23:16	RO	BASE_PTR_WIDTH	Base Pointer Width BASE_ADDR[31:32-x] is shared with all ring base addresses (where BASE_PTR_WIDTH = x). Only Ring0's base address [31:32-x] field is writable. 0: No bit of BASE_ADDR is shared.	0
15:8	RO	RX_RING_NUM	Rx Ring Number	2
7:0	RO	TX_RING_NUM	Tx Ring Number	2

235. PDMA_GLO_CFG: (offset: 0x1204)

Bits	Type	Name	Description	Initial Value
31	RW	RX_2B_OFFSET	Rx 2 Byte Offset Sets the byte size of the Rx buffer offset. 0: 4 bytes 1: 2 bytes.	0
30	RW	CSR_CLKGATE	Clock Gating Control Status Register Controls gating of the PDMA clock. 0: PDMA clock operates in freerun mode. 1: PDMA clock is gated when idle.	0
29	RW	BYTE_SWAP	Byte Swap The DMA applies the endian rule to convert the descriptor. 0: Byte swap not applied. 1: Apply byte swap.	0
28:9	-	-	Reserved	-
8	RW	DESC_32B	Support 32Byte Descriptor Enables support for 32 Byte PDMA descriptors. 0: Disable 1: Enable	0

Bits	Type	Name	Description	Initial Value
7	RW	BIG_ENDIAN	Selects the Endian mode for the SoC platform section. DMA applies the endian rule to convert payload and Tx/Rx information. DMA does not apply the endian rule to registers or descriptors. 0: Little endian 1: Big endian	0
6	RW	TX_WB_DDONE	Tx Write Back DDONE Enables TX_DMA writing back DDONE into TXD. 0: Disable 1: Enable	1
5:4	RW	PDMA_BT_SIZE	PDMA Burst Size Defines the burst size of PDMA. 0: 4 DWORD (16 bytes) 1: 8 DWORD (32 bytes) 2, 3: Reserved	1
3	RO	RX_DMA_BUSY	Indicates whether Rx DMA is busy. 0: Not busy 1: Busy	0
2	RW	RX_DMA_EN	Rx DMA Enable Enables Rx DMA. When disabled, Rx DMA finishes the current receiving packet, and then stops. 0: Disable 1: Enable	0
1	RO	TX_DMA_BUSY	Indicates whether Tx DMA is busy. 0: Not busy 1: Busy	0
0	RW	TX_DMA_EN	Tx DMA Enable Enables Tx DMA. When disabled, Tx DMA finishes the current sending packet, and then stops. 0: Disable 1: Enable	0

236. PDMA_RST_IDX: (offset: 0x1208)

Bits	Type	Name	Description	Initial Value
31:18			Reserved	
17	W1C	RST_DRX_IDX1	Reset RX_DMARX_IDX1 Resets index 1 of the Rx link table to 0.	0
16	W1C	RST_DRX_IDX0	Reset RX_DMARX_IDX0 Resets index 0 of the Rx link table to 0.	0
15:2	-	-	Reserved	-
1	W1C	RST_DTX_IDX1	Reset TX_DMATX_IDX1 Resets index 1 of the Tx link table to 0.	0

Bits	Type	Name	Description	Initial Value
0	W1C	RST_DTX_IDX0	Reset TX_DMATX_IDX0 Resets index 0 of the Tx link table to 0.	0

NOTE:

0: Disassert reset

1: Reset

237. DELAY_INT_CFG: (offset: 0x120C)

Bits	Type	Name	Description	Initial Value
31	RW	TXDLY_INT_EN	Tx Delay Interrupt Enable Enables the Tx delayed interrupt mechanism. 0: Disable 1: Enable	0
30:24	RW	TXMAX_PINT	Tx Maximum Pending Interrupts Specifies the maximum number of pending interrupts. When the number of pending interrupts is equal to or greater than the value specified here or the interrupt pending time has reached the limit (see below), a final TX_DLY_INT is generated. 0: Disable this feature.	0
23:16	RW	TXMAX_PTIME	Tx Maximum Pending Time Specifies the maximum pending time for the internal TX_DONE_INT0 and TX_DONE_INT1. When the pending time is equal to or greater than TXMAX_PTIME x 20 μ s or the number of pended TX_DONE_INT0 and TX_DONE_INT1 is equal to or greater than TXMAX_PINT (see above), a final TX_DLY_INT is generated 0: Disable this feature.	0
15	RW	RXDLY_INT_EN	Rx Delay Interrupt Enable Enables the Rx delayed interrupt mechanism. 0: Disable 1: Enable	0
14:8	RW	RXMAX_PINT	Rx Maximum Pending Interrupts Specifies the maximum number of pending interrupts. When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pending time has reached the limit (see below), a final RX_DLY_INT is generated. 0: Disable this feature.	0

Bits	Type	Name	Description	Initial Value
7:0	RW	RXMAX_PTIME	Rx Maximum Pending Time Specifies the maximum pending time for the internal RX_DONE_INT. When the pending time is equal to or greater than RXMAX_PTIME x 20 μ s, or the number of pended RX_DONE_INT is equal to or greater than RXMAX_PCNT (see above), a final RX_DLY_INT is generated. 0: Disable this feature.	0

238. FREEQ_THRES: (offset: 0x1210)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	
4:0	RW	FREEQ_THRES	Blocks this interface when Rx descriptors reach this threshold.	0x2

239. INT_STATUS: (offset: 0x1220, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31	R/ W1C	RX_COHERENT	Rx Coherent Interrupt Asserts when the Rx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0
30	R/ W1C	RX_DLY_INT	Rx Delay Interrupt Asserts when the number of pended Rx interrupts has reached a specified level, or when the pending time is reached. Configure this interrupt using the DELAY_INT_CFG register.	0
29	R/ W1C	TX_COHERENT	Tx Coherent Interrupt Asserts when the Tx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0
28	R/ W1C	TX_DLY_INT	Tx Delay Interrupt Asserts when the number of pended Tx interrupts has reached a specified level, or when the pending time is reached. Configure this interrupt using the DELAY_INT_CFG register.	0
27	RW	MCU_CMD_INT3	MCU command interrupt 3: Reserved	0
26	RW	MCU_CMD_INT2	MCU command interrupt 2: Reserved	0
25	RW	MCU_CMD_INT1	MCU command interrupt 1: Reserved	0
24	RW	MCU_CMD_INT0	MCU command interrupt 0: Reserved	0
23:18	-	-	Reserved	-
17	R/ W1C	RX_DONE_INT1	Rx Queue 1 Done Interrupt Asserts when an Rx packet is received on Queue 1.	0

Bits	Type	Name	Description	Initial Value
16	R/ W1C	RX_DONE_INT0	Rx Queue 0 Done Interrupt Asserts when an Rx packet is received on Queue 0.	0
15:2	-	-	Reserved	-
1	R/ W1C	TX_DONE_INT1	Tx Queue 1 Done Interrupt Asserts when a Tx Queue 1 packet is transmitted.	0
0	R/ W1C	TX_DONE_INT0	Tx Queue 0 Done Interrupt Asserts when a Tx Queue 0 packet is transmitted.	0

NOTE:

Read:

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

240. INT_MASK: (offset: 0x1228)

Bits	Type	Name	Description	Initial Value
31	RW	RX_COHERENT_INT_MSK	Masks the Rx Coherent interrupt. This interrupt asserts when the Rx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0
30	RW	RX_DLY_INT_MSK	Masks the Rx Delay interrupt. This interrupt asserts when the number of pending Rx interrupts has reached a specified level, or when the pending time is reached.	0
29	RW	TX_COHERENT_INT_MSK	Masks the Tx Coherent interrupt. This interrupt asserts when the Tx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0
28	RW	TX_DLY_INT_MSK	Masks the Tx Delay interrupt. This interrupt asserts when the number of pending Tx interrupts has reached a specified level, or when the pending time is reached.	0
27	RW	MCU_CMD_INT3_MSK	MCU command interrupt 3 enable: Reserved	0
26	RW	MCU_CMD_INT2_MSK	MCU command interrupt 2 enable: Reserved	0
25	RW	MCU_CMD_INT1_MSK	MCU command interrupt 1 enable: Reserved	0
24	RW	MCU_CMD_INT0_MSK	MCU command interrupt 0 enable: Reserved	0
23:18	-	-	Reserved	-
17	RW	RX_DONE_INT_MSK1	Masks the Rx Queue 1 Done interrupt. This interrupt asserts when an Rx packet is received on Queue 1.	0
16	RW	RX_DONE_INT_MSK0	Masks the Rx Queue 0 Done interrupt. This interrupt asserts when an Rx packet is received on Queue 0.	0

Bits	Type	Name	Description	Initial Value
15:2	-	-	Reserved	-
1	RW	TX_DONE_INT_MSK1	Masks the Tx Queue 1 Done interrupt. This interrupt asserts when a Tx packet is transmitted on Queue 1.	0
0	RW	TX_DONE_INT_MSK0	Masks the Tx Queue 0 Done interrupt. This interrupt asserts when a Tx packet is transmitted on Queue 0.	0

NOTE: Where applicable,
0: Unmasks the interrupt.
1: Masks the interrupt.

2.19 Frame Engine

2.19.1 PSE Features

- Wire-speed (1000 Mbps) Ethernet LAN/WAN NAT/NAPT routing
- Egress rate limiting/shaping (by GDMA)
- Flow control for no-packet-loss guarantee
- Emulated multicast support for keep-alive (can mirror a Tx packet to CPU)
- IP/TCP/UDP Checksum offload (by GDMA)
- IP/TCP/UDP Checksum Generation (by CDMA)
- VLAN & PPPOE header insertion (by CDMA)
- TCP Segmentation Offload (by CDMA)
- Auto-Padding for sub-64 B packets

2.19.2 PPE Features

- IPV4 NAT/NAPT, ipv6 Routing and Tunnel IP (DS-Lite, 6RD)
- 1/2/4/8/16 K flows
- Virtual server, port-triggering & port forwarding
- All types of IPV4 NAT(NAPT, Twice NAT)
- All types of MAC/VLAN/PPPOE/IP/TCP/UDP binding
- 4 VLAN tagging (Q-in-Q)
- VID Swapping
- Support for 65536 PPPOE sessions
- PPPOE pass-through
- Cone-NAT, port-restricted NAT & Symmetric NAT
- Per flow accounting or rate limiting
- DDOS avoidance by rate limiting
- Stateful packet filtering (SPI)
- Patent-pending flow offloading technology for flexible/high performance packet L3/L4 packet processing.
- Multi-WAN load balancing with hardware and software cooperation
- QoS for multimedia traffic
- Within 16 flows, 2 Gbps wire-speed is supported for any packet size.

NOTE: All PPE features mentioned above require software porting to function.

2.19.3 Packet DMA (PDMA) Features

- Supports 4 Tx descriptor rings and two Rx descriptor rings
- Scatter/Gather DMA
- Delayed interrupt
- Configurable 4/8 32-bit word burst length

2.19.4 Block Diagram

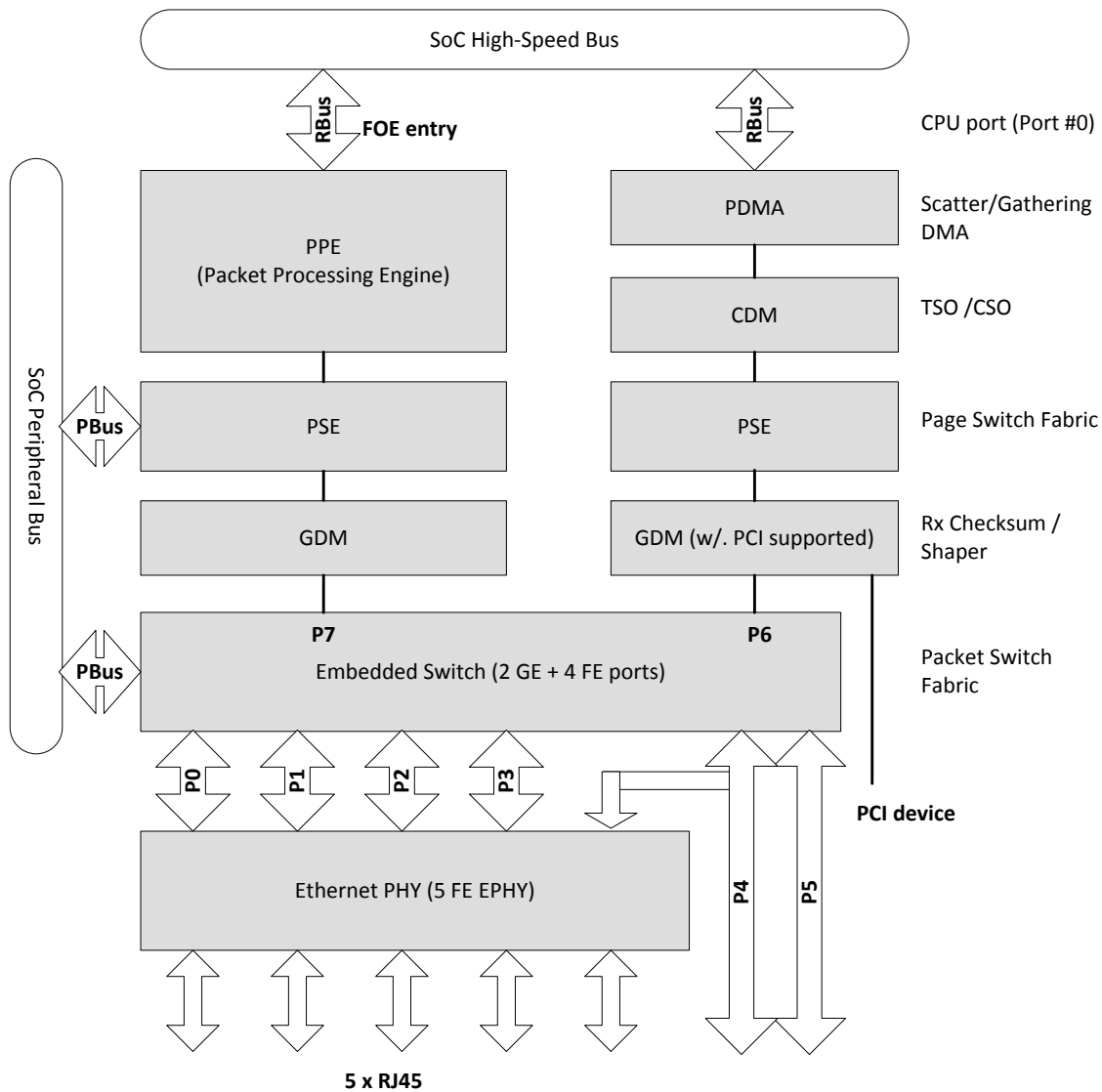
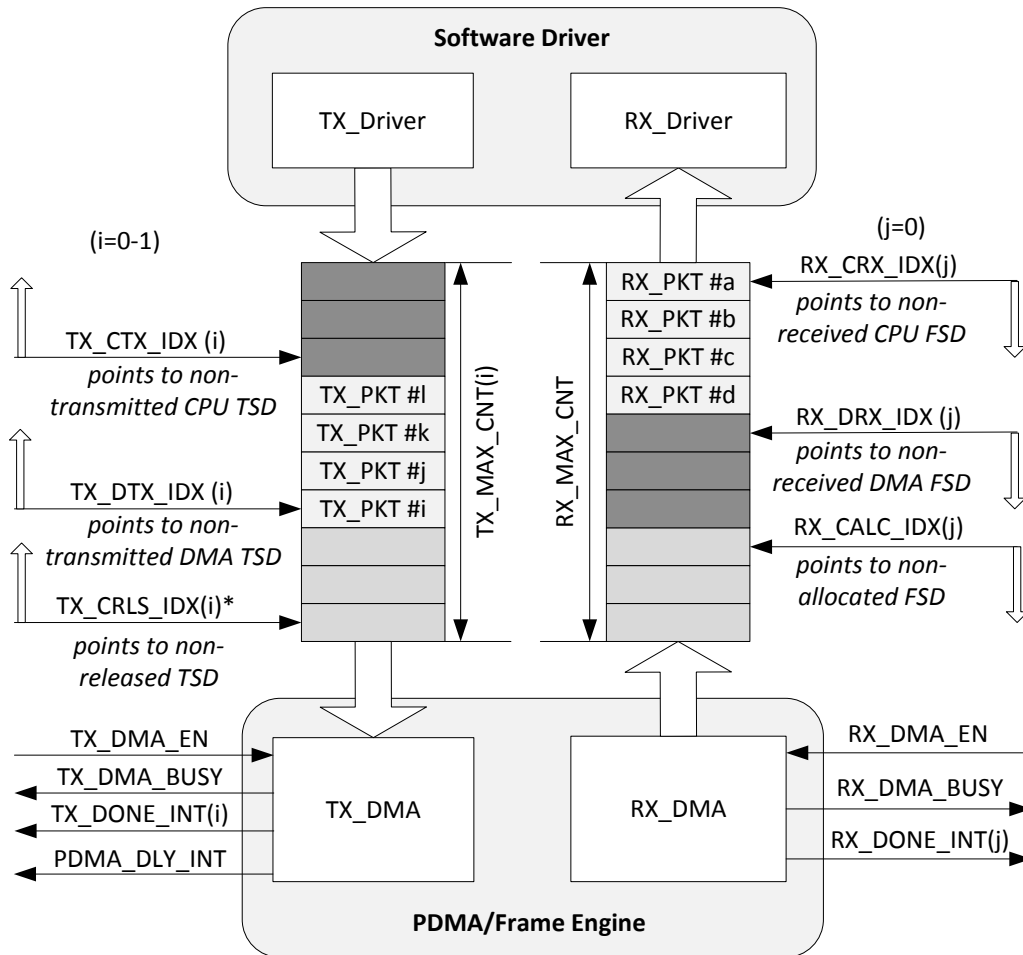


Figure 2-25 Frame Engine Block Diagram

2.19.5 PDMA FIFO-like Ring Concept



NOTE:

1. TX_CRLS_IDX(i) and RX_CRX_IDX (j) are not Located in PDMA hardware, they are resident in CPU local memory.
2.
 - RXQ0: For GE MAC receive
 - TXQ0: GE MAC low priority queue
 - TXQ1: GE MAC high priority queue

Figure 2-26 PDMA FIFO-like Ring Concept

2.19.6 PDMA Tx Descriptor Format

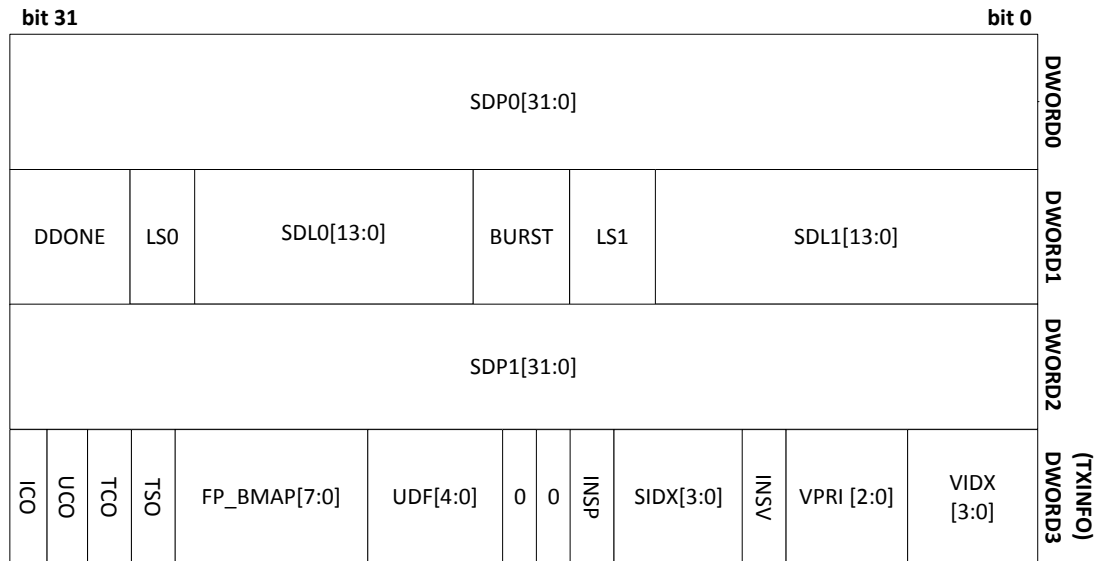


Figure 2-27 PDMA Tx Descriptor Format

The following is a detailed description of each field in the PDMA TXD.

2.19.6.1 PDMA Tx Field Descriptions

Bit	Name	Description
DWORD0		
31:0	SDP0	Segment Data Pointer0
DWORD1		
31	DDONE	DMA Done: Indicates DMA has transferred the segment pointed to by this Tx descriptor.
30	LS0	Last Segment0: Data pointed to by SDP0 is the last segment.
29:16	SDL0	Segment Data Length0: Segment data length for the data pointed to by SDP0.
15	BURST	When set, the scheduler cannot hand over to other Tx queues. Should not transmit the next packet.
14	LS1	Last Segment1: Data pointed to by SDP1 is the last segment.
13:0	SDL1	Segment Data Length1: Segment data length for the data pointed to by SDP1.
DWORD2		
31:0	SDP1	Segment Data Pointer1
DWORD3 (TXINFO)		
31	ICO	IP checksum offload enable
30	UCO	UDP checksum offload enable
23	TCO	TCP checksum offload enable
28	TSO	TCP segmentation offload
27:20	FP_BMAP	Forced destination port on GSW bit[0:5]: Ports 0 to 5 bit[6]: CPU bit[7]: PPE FP_BMAP = 0: routing by DA
19:15	UDF	User defined field
14	0	Reserved
13	0	Reserved
12	INSP	Insert PPPoE header
11:8	SIDX	PPPoE session index
7	INSV	Insert VLAN tag
6:4	VPRI	VLAN priority tag to be inserted
3:0	VIDX	VLAN ID index

2.19.7 PDMA Rx Descriptor Format

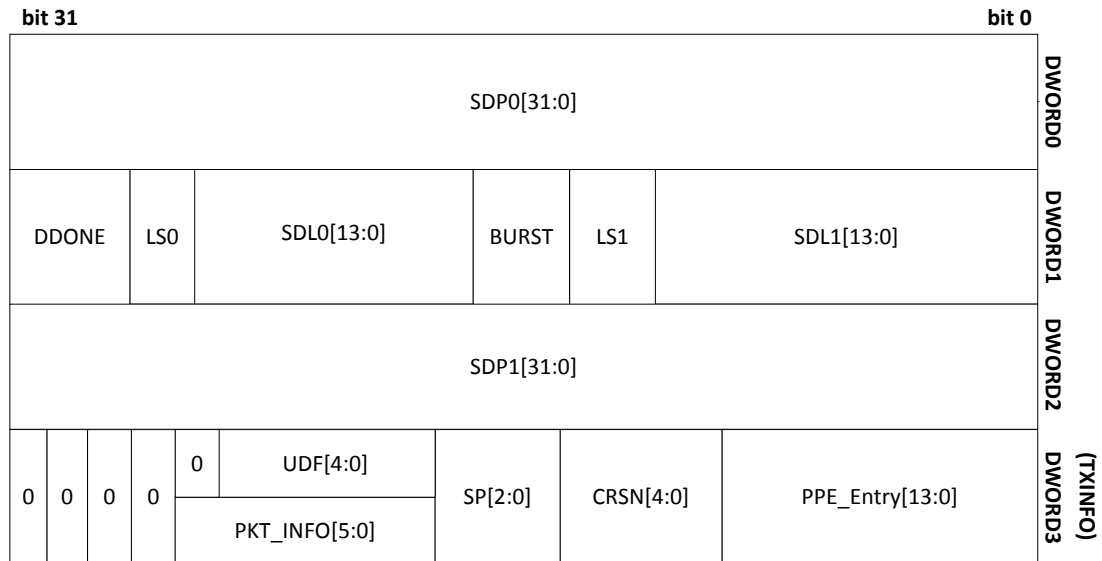


Figure 2-28 PDMA Rx Descriptor Format

The following is a detailed description of each field in the PDMA RXD.

2.19.7.1 PDMA Rx Field Descriptions

Bit	Name	Description
DWORD0		
31:0	SDP0	Segment Data Pointer 0 for header (if HP_SEP_EN = 1) or the whole packet (if HP_SEP_EN = 0).
DWORD1		
31	DDONE	DMA Done: Indicates DMA has received the segments pointed to by this Rx descriptor.
30	LS0	Last Segment0: Data pointed to by SDP0 is the last segment.
29:1 6	SDL0	Segment Data Length0: Segment data length for the data pointed to by SDP0.
15	0	Reserved
14	1	Reserved
13:0	SDL1	Segment Data Length1: Segment data length for the data pointed to by SDP1.
DWORD2		
31:0	SDP1	Segment Data Pointer1 for payload (if HP_SEG_LEN! = 0), or RXWI + Packet Length (if HP_SEG_LEN! = 0)
DWORD3 (TXINFO)		
31	0	Reserved
30	0	Reserved
29	0	Reserved
28	0	Reserved
27	0	Reserved
26:22	UDF	User defined field (when SP = 3'd6 from CPU port)
27:22	PKT _INFO	Packet information Bit[5]: IPv6 packet Bit[4]: IPv4 packet Bit[3]: IPV4 checksum error Bit[2]: TCP packet with ACK flag Bit[1]: L4 TCP or UDP packet without fragmented flag Bit[0]: L4 checksum error
21:19	SP	GSW source port
18:14	CRSN	PPE to CPU reason
13:0	PPE _Entry	PPE Entry number 14'h3FFF: Invalid entry

2.19.8 Global Registers (base: 0x1010_0000)

2.19.8.1 List of Registers

No.	Offset	Register Name	Description	Page
241	0x0000	FE_GLO_CFG	Frame Engine Global Configuration	210
242	0x0004	FE_RST_GLO	Frame Engine Global Reset	210
243	0x0008	FE_INT_STATUS	Frame Engine Interrupt Status	210
244	0x000C	FE_INT_ENABLE	Frame Engine Interrupt Enable	212
245	0x0010	FOE_TS_T	Frame Offload Engine Time Stamp	213
246	0x0014	IPV6_EXT	IPv6 Extension Header	214
247	0x0018	G2P_FC	GSW to PDMA Flow Control	214
248	0x001C	P2G_FC	PDMA to GSW Flow Control	215

2.19.8.2 Register Descriptions

241. FE_GLO_CFG: Frame Engine Global Configuration (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:16	RW	EXT_VLAN	Extended VLAN protocol ID	0x8100
15:8	-	-	Reserved	0x7D
7:4	RW	L2_SPACE	L2 Space (unit: 8 bytes)	0xB
3:1	-	-	Reserved	0x0
0	RW	RATE_MINUS	Minus byte counts for incoming frame 1'b0: A specific byte count is added to the frame length according to FOE_TS_T.ADD_RATE_BYTE. 1'b1: A specific byte count is subtracted from the incoming frame length.	0x0

242. FE_RST_GLO: Frame Engine Global Reset (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:24	RC	PPE_DROP_CNT	PPE Flow Control Drop Packet Count Counts the number of packets dropped by the PSE when packets go through the PPE port.	0x0
23:16	RC	CPU_DROP_CNT	CPU Flow Control Drop Packet Count Counts the number of packets dropped by the PSE when packets go through the CPU port.	0x0
15:1	-	-	Reserved	0x0
0	RW	PSE_RESET	Resets the Packet Switch Engine (PSE) 0: Disassert reset 1: Reset	0x0

243. FE_INT_STATUS: Frame Engine Interrupt Status (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31	W1C	CNT_PPE_AF	PPE Counter Table Almost Full Interrupt Asserts when the PPE counter table is almost full.	0x0
30	-	-	Reserved	0x0
29	W1C	CNT_GDM1_AF	GDMA1 Counter Table Almost Full Interrupt Asserts when the GDMA1 counter table is almost full.	0x0
28:22	-	-	Reserved	0x0
21	W1C	PPE_OTHER_DROP	PPE GE1 Packet Dropped for Other Reason Interrupt Asserts when GE1 drops a packet due to other reasons (e.g. too short, too long, FIFO overflow, checksum error, etc.)	0x0

Bits	Type	Name	Description	Initial Value
20	W1C	PPE_CRC_DROP	PPE GE1 CRC Error Dropped Packet Interrupt Asserts when the GE1 discards a packet due to CRC error.	0x0
19	W1C	PPE_P1_FC	PPE Port 1 Flow Control Asserted Interrupt Asserts when flow control is asserted on port 1 (GDMA1).	0x0
18	W1C	PPE_P0_FC	PPE Port 0 Flow Control Asserted Interrupt Asserts when flow control is asserted on port 0 (CDMA).	0x0
17	W1C	PPE_BUF_DROP	PPE Buffer Limitation Dropped Packet Interrupt Asserts when the PSE discards a packet due to a buffer sharing limitation (flow control).	0x0
16	W1C	PPE_FQ_EMPTY	PPE Free Queue Empty Threshold Interrupt Asserts when the remaining buffers on the free queue are lower than the empty threshold and a forced drop condition has occurred.	0x0
15	RW	TSO_ILLEGAL	TCP Segmentation Offload (TSO) Illegal packet Asserts when the packet format is not supported by TSO (e.g., not TSO or IPv4/v6) but when TSO is enabled for that packet.	0x0
14	-	-	Reserved	0x0
13:8	-	-	Reserved	0x0
7	W1C	PDMA_RXRING_FC	PDMA 2 Rx Ring Flow Control Interrupt Asserts when any Rx ring is congested and pauses the received queue on the switch.	0x0
6	W1C	PDMA_TXRING_FC	PDMA 4 Tx Ring Flow Control Interrupt Asserts when the transmitted queue on switch is congested and pauses PDMA Tx ring.	0x0
5	W1C	CPU_OTHER_DROP	CPU GE1 Packet Dropped for Other Reason Interrupt Asserts when GE1 drops a packet due to other reasons (e.g. too short, too long, FIFO overflow, checksum error, etc.)	0x0
4	W1C	CPU_CRC_DROP	CPU GE1 CRC Error Dropped Packet Interrupt Asserts when the GE1 discards a packet due to CRC error.	0x0
3	W1C	CPU_P1_FC	CPU Port1 (GDM) Flow Control Interrupt Asserts when flow control is asserted on port 1 (GDM).	0x0
2	W1C	CPU_P0_FC	CPU Port0 (CDM) Flow Control Interrupt Asserts when flow control is asserted on port 0 (CDM).	0x0
1	W1C	CPU_BUF_DROP	CPU PSE Buffer Sharing Packet Drop Interrupt Asserts when the CPU PSE discards a packet due to buffer sharing limitations (flow control).	0x0

Bits	Type	Name	Description	Initial Value
0	W1C	CPU_FQ_EMPTY	CPU PSE Free Queue Empty Threshold Reached Interrupt Asserts when the remaining buffers on the free queue are lower than the empty threshold and a forced drop condition has occurred.	0x0

NOTE:

Read:

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

244. FE_INT_ENABLE: Frame Engine Interrupt Enable (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31	RW	CNT_PPE_AF	Enables the PPE Counter Table Almost Full interrupt. This interrupt asserts when the PPE counter table is almost full.	0x0
30	-	-	Reserved	0x0
29	RW	CNT_GDM1_AF	Enables the GDMA1 Counter Table Almost Full interrupt. This interrupt asserts when the GDMA1 counter table is almost full.	0x0
28:22	-	-	Reserved	0x0
21	RW	PPE_OTHER_DROP	Enables the GE1 Packet Dropped for Other Reason interrupt. This interrupt asserts when GE1 drops a packet due to other reasons (e.g. too short, too long, FIFO overflow, checksum error, etc.)	0x0
20	RW	PPE_CRC_DROP	Enables the GE1 CRC Error Dropped Packet interrupt. This interrupt asserts when the GE1 discards a packet due to CRC error.	0x0
19	RW	PPE_P1_FC	Enables the PSE Port 1 Flow Control Asserted interrupt. This interrupt asserts when flow control is asserted on port 1 (GDMA1).	0x0
18	RW	PPE_P0_FC	Enables the PSE Port 0 Flow Control Asserted interrupt. This interrupt asserts when flow control is asserted on port 0 (CDMA).	0x0
17	RW	PPE_BUF_DROP	Enables the CPU PSE Buffer Limitation Dropped Packet interrupt. This interrupt asserts when the PSE discards a packet due to a buffer sharing limitation (flow control).	0x0
16	RW	PPE_FQ_EMPTY	Enables the CPU PSE Free Queue Empty Threshold interrupt. This interrupt asserts when the remaining buffers on the free queue are lower than the empty threshold and a forced drop condition has occurred.	0x0

Bits	Type	Name	Description	Initial Value
15	RW	TSO_ILLEGAL	Enables the TCP Segmentation Offload (TSO) Illegal packet interrupt. This interrupt asserts when the packet format is not supported by TSO (e.g., not TSO or IPv4/v6) but when TSO is enabled for that packet.	0x0
14	-	-	Reserved	0x0
13:8	-	-	Reserved	0x0
7	RW	PDMA_RXRING_FC	Enables the PDMA 2 Rx Ring Flow Control Interrupt. This interrupt asserts when any Rx ring is congested and pauses the receive queue on the switch.	0x0
6	RW	PDMA_TXRING_FC	Enables the PDMA 4 Tx Ring Flow Control Interrupt. This interrupt asserts when the transmitted queue on the switch is congested and pauses the PDMA Tx ring.	0x0
5	RW	GE1_OTHER_DROP	Enables the GE1 Packet Dropped for Other Reason interrupt. This interrupt asserts when GE1 drops a packet due to other reasons (e.g. too short, too long, FIFO overflow, checksum error, etc.)	0x0
4	RW	GE1_CRC_DROP	Enables the GE1 CRC Error Dropped Packet interrupt. This interrupt asserts when the GE1 discards a packet due to CRC error.	0x0
3	RW	CPU_P1_FC	Enables the CPU Port1 (GDM) Flow Control Interrupt. This interrupt asserts when flow control is asserted on port 1 (GDM).	0x0
2	RW	CPU_P0_FC	Enables the CPU Port0 (CDM) Flow Control Interrupt. This interrupt asserts when flow control is asserted on port 0 (CDM).	0x0
1	RW	CPU_BUF_DROP	Enables the CPU PSE Buffer Sharing Packet Drop Interrupt. This interrupt asserts when the CPU PSE discards a packet due to buffer sharing limitations (flow control).	0x0
0	RW	CPU_FQ_EMPTY	Enables the CPU PSE Free Queue Empty Threshold Reached Interrupt. This interrupt asserts when the remaining buffers on the free queue are lower than the empty threshold and a forced drop condition has occurred.	0x0

NOTE:

0: Disable the interrupt.

1: Enable the interrupt.

245. FOE_TS_T: Time Stamp (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
23:16	RW	ADD_RATE_BYTE	Add Rate Byte The number of bytes that should be added to the frame byte length while calculating the rate limit.	0x18
15:0	RW	FOE_TS_T	Frame Offload Engine Time Stamp (unit: sec)	0x0

246. IPV6_EXT: IPv6 Extension Header (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:24	RW	IP6_EXT3	IPv6 Extension Header #3	0x0
23:16	RW	IP6_EXT2	IPv6 Extension Header #2	0x0
15:8	RW	IP6_EXT1	IPv6 Extension Header #1	0x0
7:0	RW	IP6_EXT0	IPv6 Extension Header #0	0x0

247. G2P_FC: GSW to PDMA Flow Control (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:28	RW	WAN_TR3_FCON	PDMA Tx Ring #3 Flow Control by WAN port of the switch Selects when to pause Tx ring #3. Bit[19]: When GSW WAN Q3 is full. Bit[18]: When GSW WAN Q2 is full. Bit[17]: When GSW WAN Q1 is full. Bit[16]: When GSW WAN Q0 is full.	0xF
27:24	RW	WAN_TR2_FCON	PDMA Tx Ring #2 Flow Control by WAN port of the switch Selects when to pause Tx ring #2. Bit[19]: When GSW WAN Q3 is full. Bit[18]: When GSW WAN Q2 is full. Bit[17]: When GSW WAN Q1 is full. Bit[16]: When GSW WAN Q0 is full.	0xF
23:20	RW	WAN_TR1_FCON	PDMA Tx Ring #1 Flow Control by WAN port of the switch Selects when to pause Tx ring #1. Bit[19]: When GSW WAN Q3 is full. Bit[18]: When GSW WAN Q2 is full. Bit[17]: When GSW WAN Q1 is full. Bit[16]: When GSW WAN Q0 is full.	0xF
19:16	RW	WAN_TR0_FCON	PDMA Tx Ring #0 Flow Control by WAN port of the switch Selects when to pause Tx ring #0. Bit[19]: When GSW WAN Q3 is full. Bit[18]: When GSW WAN Q2 is full. Bit[17]: When GSW WAN Q1 is full. Bit[16]: When GSW WAN Q0 is full.	0xF

Bits	Type	Name	Description	Initial Value
15:12	RW	LAN_TR3_FCON	PDMA Tx Ring #3 Flow Control by LAN port of the switch Selects when to pause Tx ring #3. Bit[19]: When GSW LAN Q3 is full. Bit[18]: When GSW LAN Q2 is full. Bit[17]: When GSW LAN Q1 is full. Bit[16]: When GSW LAN Q0 is full.	0xF
11:8	RW	LAN_TR2_FCON	PDMA Tx Ring #2 Flow Control by LAN port of the switch Selects when to pause Tx ring #2. Bit[19]: When GSW LAN Q3 is full. Bit[18]: When GSW LAN Q2 is full. Bit[17]: When GSW LAN Q1 is full. Bit[16]: When GSW LAN Q0 is full.	0xF
7:4	RW	LAN_TR1_FCON	PDMA Tx Ring #1 Flow Control by LAN port of the switch Selects when to pause Tx ring #1. Bit[19]: When GSW LAN Q3 is full. Bit[18]: When GSW LAN Q2 is full. Bit[17]: When GSW LAN Q1 is full. Bit[16]: When GSW LAN Q0 is full.	0xF
3:0	RW	LAN_TR0_FCON	PDMA Tx Ring #0 Flow Control by LAN port of the switch Selects when to pause Tx ring #0. Bit[19]: When GSW LAN Q3 is full. Bit[18]: When GSW LAN Q2 is full. Bit[17]: When GSW LAN Q1 is full. Bit[16]: When GSW LAN Q0 is full.	0xF

248. P2G_FC: PDMA to GSW Flow Control (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RW	RR1_GSW_FCON	PDMA Rx Ring #1 Pause GSW CPU Queue Selects which GSW queue to pause when PDMA Rx ring 1 is almost full. Bit[0]: Queue 0 ... Bit[7]: Queue 7	0x0
7:0	RW	RR0_GSW_FCON	PDMA Rx Ring #0 Pause GSW CPU Queue Selects which GSW queue to pause when PDMA Rx ring 0 is almost full. Bit[0]: Queue 0 ... Bit[7]: Queue 7	0x0

2.19.9 CPU Port Registers (base: 0x1010_0400)

2.19.9.1 List of Registers

No.	Offset	Register Name	Description	Page
249	0x0000	CDM_CSG_CFG	CDMA Checksum Generation Configuration	217
250	0x0010	PPPOE_SID_0001	PPPoE Session ID Index 0, 1	217
251	0x0014	PPPOE_SID_0203	PPPoE Session ID Index 2,3	217
252	0x0018	PPPOE_SID_0405	PPPoE Session ID Index 4, 5	217
253	0x001C	PPPOE_SID_0607	PPPoE Session ID Index 6, 7	217
254	0x0020	PPPOE_SID_0809	PPPoE Session ID Index 8, 9	217
255	0x0024	PPPOE_SID_1011	PPPoE Session ID Index 10, 11	218
256	0x0028	PPPOE_SID_1213	PPPoE Session ID Index 12, 13	218
257	0x002C	PPPOE_SID_1415	PPPoE Session ID Index 14, 15	218
258	0x0030	VLAN_ID_0001	VLAN 0, 1 ID	218
259	0x0034	VLAN_ID_0203	VLAN 2, 3 ID	218
260	0x0038	VLAN_ID_0405	VLAN 4, 5 ID	218
261	0x003C	VLAN_ID_0607	VLAN 6, 7 ID	218
262	0x0040	VLAN_ID_0809	VLAN 8, 9 ID	219
263	0x0044	VLAN_ID_1011	VLAN 10, 11 ID	219
264	0x0048	VLAN_ID_1213	VLAN 12, 13 ID	219
265	0x004C	VLAN_ID_1415	VLAN 14, 15 ID	219
266	0x0100	PSE_FQFC_CFG	PSE Free Queue Flow Control Configuration	219
267	0x0104	PSE_IQ_CFG	PSE Input Queue Configuration	220
268	0x0108	PSE_QUE_STA	PSE Queue Status	220
269	0x0200	GDM_FWD_CFG	GDM Forwarding Configuration	220
270	0x0204	GDM_SHPR_CFG	GDM Output Shaper Configuration	221

2.19.9.2 Register Descriptions

249. CDM_CSG_CFG: CDM Checksum Generation Configuration (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:16	RW	INS_VLAN	Inserted VLAN protocol ID	0x8100
15:8	RW	SP_RING	Source Port to PDMA Ring selection Selects the source port for packets entering the PDMA Ring #1. Bit[8]: Source port #0 will enter PDMA Ring#1 ... Bit[15]: Source port #7 will enter PDMA Ring#1	0x0
7:3	-	-	Reserved	0x0
2	RW	ICS_GEN_EN	Enables IPv4 header checksum generation.	0x0
1	RW	UCS_GEN_EN	Enables UDP checksum generation.	0x0
0	RW	TCS_GEN_EN	Enables TCP checksum generation.	0x0

NOTE: Where applicable,
0: Disable
1: Enable

250. PPPOE_SID_0001: PPPoE Session Identification (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID1	PPPoE Session ID for SID INDEX#1	0x0
15:0	RW	PPPOE_SID0	PPPoE Session ID for SID INDEX#0	0x0

251. PPPOE_SID_0203: PPPoE Session Identification (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID3	PPPoE Session ID for SID INDEX#3	0x0
15:0	RW	PPPOE_SID2	PPPoE Session ID for SID INDEX#2	0x0

252. PPPOE_SID_0405: PPPoE Session Identification (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID5	PPPoE Session ID for SID INDEX#5	0x0
15:0	RW	PPPOE_SID4	PPPoE Session ID for SID INDEX#4	0x0

253. PPPOE_SID_0607: PPPoE Session Identification (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID7	PPPoE Session ID for SID INDEX#7	0x0
15:0	RW	PPPOE_SID6	PPPoE Session ID for SID INDEX#6	0x0

254. PPPOE_SID_0809: PPPoE Session Identification (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID9	PPPoE Session ID for SID INDEX#9	0x0

Bits	Type	Name	Description	Initial Value
15:0	RW	PPPOE_SID8	PPPoE Session ID for SID INDEX#8	0x0

255. PPPOE_SID_1011: PPPoE Session Identification (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID11	PPPoE Session ID for SID INDEX#11	0x0
15:0	RW	PPPOE_SID10	PPPoE Session ID for SID INDEX#10	0x0

256. PPPOE_SID_1213: PPPoE Session Identification (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID13	PPPoE Session ID for SID INDEX#13	0x0
15:0	RW	PPPOE_SID12	PPPoE Session ID for SID INDEX#12	0x0

257. PPPOE_SID_1415: PPPoE Session Identification (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:16	RW	PPPOE_SID15	PPPoE Session ID for SID INDEX#15	0x0
15:0	RW	PPPOE_SID14	PPPoE Session ID for SID INDEX#14	0x0

258. VLAN_ID_0001: VLAN Identification (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID1	VLAN ID of VLAN1	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID0	VLAN ID of VLAN0	0x0

259. VLAN_ID_0203: VLAN Identification (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID3	VLAN ID of VLAN3	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID2	VLAN ID of VLAN2	0x0

260. VLAN_ID_0405: VLAN Identification (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID5	VLAN ID of VLAN5	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID4	VLAN ID of VLAN4	0x0

261. VLAN_ID_0607: VLAN Identification (offset: 0x003C)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID7	VLAN ID of VLAN7	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID6	VLAN ID of VLAN6	0x0

262. VLAN_ID_0809: VLAN Identification (offset: 0x0040)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID9	VLAN ID of VLAN9	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID8	VLAN ID of VLAN8	0x0

263. VLAN_ID_1011: VLAN Identification (offset: 0x0044)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID11	VLAN ID of VLAN11	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID10	VLAN ID of VLAN10	0x0

264. VLAN_ID_1213: VLAN Identification (offset: 0x0048)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID13	VLAN ID of VLAN13	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID12	VLAN ID of VLAN12	0x0

265. VLAN_ID_1415: VLAN Identification (offset: 0x004C)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	VLAN_ID15	VLAN ID of VLAN15	0x0
15:12	-	-	Reserved	0x0
11:0	RW	VLAN_ID14	VLAN ID of VLAN14	0x0

266. PSE_FQFC_CFG: PSE Free Queue Flow Control Configuration (offset: 0x0100)

Bits	Type	Name	Description	Initial Value
31:24	RO	FQ_PCNT	Free Queue Page Count The free buffer page count on the free queue of the PSE block.	0x18

Bits	Type	Name	Description	Initial Value
23:16	RW	FQ_MAX_PCNT	Maximum Free Queue Page Count Please reset PSE after re-programming this register.	0x18
15:8	RW	FQ_FC_RLS	Free Queue Flow Control Release Page Count	0x1
7:0	RW	FQ_FC_ASRT	Free Queue Flow Control Assertion Page Count	0x1

267. PSE_IQ_CFG: PSE Input Queue Configuration (offset: 0x0104)

Bits	Type	Name	Description	Initial Value
31:24	RW	P1_IQ_RLS	P1 Virtual Input Queue Flow Control Release Page Count	0xc
23:16	RW	P1_IQ_ASRT	P1 Virtual Input Queue Flow Control Assertion Page Count	0xc
15:8	RW	P0_IQ_RLS	P0 Virtual input Queue Flow Control Release Page Count	0xc
7:0	RW	P0_IQ_ASRT	P0 Virtual input Queue Flow Control Assertion Page Count	0xc

268. PSE_QUE_STA: PSE Queue Status (offset: 0x0108)

Bits	Type	Name	Description	Initial Value
31:24	RO	P1_IQ_PCNT	P1 Virtual Input Queue Page Count	0x0
23:16	RO	P0_IQ_PCNT	P0 Virtual Input Queue Page Count	0x0
15:8	RO	P1_OQ_PCNT	P1 Output Queue Page Count	0x0
7:0	RO	P0_OQ_PCNT	P0 Output Queue Page Count	0x0

269. GDM_FWD_CFG: GDM Forwarding Configuration (offset: 0x0200)

Bits	Type	Name	Description	Initial Value
31:28	RW	GDM_JMB_LEN	GDM Jumbo Packet Length When GDM_JMB_EN=1, this parameter defines the maximum packet length (including CRC) that the GDM could receive in a 1024-byte unit. Valid values are from 0 to 2.	0x2
27:26	-	-	Reserved	0x0
25	RW	GDM_20US_TICK_SLT	GDM 20 μ s Tick Select Sets the interval the GDMA traffic shaper adds a token. 0: Every 1 ms. 1: Every 20 μ s. This configures the GDM_TK_RATE (bit[13:0]) in GDM_SHPR_CFG register.	0x0
24	RW	GDM_TCI_81xx	GDM Check 2-byte Special Tag 0: No special tag within EXT_VLAN[15:0] 1: Check 2-Byte special tag within EXT_VLAN[15:0]	0x0

Bits	Type	Name	Description	Initial Value
23	RW	GDM_DROP_256B	GDM Drop 256-Byte Packets A special mode to drop packets with payload > 256 bytes. 0: Drop packets according to standard Ethernet frame length limitation. 1: Drop packets with payload >256 bytes	0x0
22	RW	GDM_ICS_EN	IPv4 Header Checksum Check Enable 0: Disable 1: Enable	0x1
21	RW	GDM_TCS_EN	TCP Checksum Check Enable 0: Disable 1: Enable	0x1
20	RW	GDM_UCS_EN	UDP Checksum Check Enable 0: Disable 1: Enable	0x1
19	RW	GDM_JMB_EN	GDM Jumbo Frames Enable 0: Drop received frames if length is great than 1518 (1522 for VLAN frames, and 1526 for double VLAN frames) 1: Allow receive jumbo frames length up to 2 KB.	0x0
18:17	-	-	Reserved	0x0
16	RW	GDM_STRPCRC	GDM CRC Stripping Enables GDMA1 automatic Rx CRC stripping. 0: Disable 1: Enable	0x1
15:3	-	-	Reserved	0x0
2:0	RW	GDM_FRC_P	GDMA1 Frames Destination Port 3'd0: Port 0 CPU 3'd1: Port 1 GDM 3'd2 to 6: Reserved 3'd7: Discard	0x7

270. GDM_SHPR_CFG: GDM Output Shaper Configuration (offset: 0x0204)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24	RW	GDM_SHPR_EN	GDM Output Shaper Enable 0: Disable 1: Enable	0x0
23:16	RW	GDM_BK_SIZE	GDM output shaper maximum bucket size (unit: KB)	0x0
15:14	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
13:0	RW	GDM_TK_RATE	GDM Output Shaper Token Rate Based on settings in GDM1_20US_TICK_SLT, bit[25]in the GDM_FWD_CFG register. (unit: 8 B/ms or 8 B/20 μ s)	0x0

2.19.10 PDMA Registers (base: 0x1010_0800)

2.19.10.1 List of Registers

No.	Offset	Register Name	Description	Page
271	0x0000, 0x0010, 0x0020, 0x0030	TX_BASE_PTRn	Tx Ring n Base Address Pointer	224
272	0x0004, 0x0014, 0x0024, 0x0034	TX_MAX_CNTn	Tx Ring n Maximum Count	224
273	0x0008, 0x0018, 0x0028, 0x0038	TX_CTX_IDXn	Tx Ring n CPU Transmit Index	224
274	0x000C, 0x001C, 0x002C, 0x003C	TX_DTX_IDXn	Tx Ring n DMA Transmit Index	224
275	0x0100, 0x0110	RX_BASE_PTRn	Rx Ring n Base Address Pointer	224
276	0x0104, 0x0114	RX_MAX_CNTn	Rx Ring n Maximum Count	224
277	0x0108, 0x0118	RX_CALC_IDXn	Rx Ring n CPU Allocate Index	224
278	0x010C, 0x011C	RX_DRX_IDXn	Rx Ring n DMA Receive Index	225
279	0x0200	PDMA_INFO	PDMA Information	225
280	0x0204	PDMA_GLO_CFG	PDMA Global Configuration	225
281	0x0208	PDMA_RST_IDX	PDMA Reset Index	226
282	0x020C	DELAY_INT_CFG	Delay Interrupt Configuration	227
283	0x0210	FREEQ_THRES	Free Queue Threshold	228
284	0x0220	INT_STATUS	Interrupt Status	228
285	0x0228	INT_MASK	Interrupt Mask	229
286	0x0280	SCH_Q01_CFG	Scheduler Configuration for Queue 0, 1	230
287	0x0284	SCH_Q23_CFG	Scheduler Configuration for Queue 2, 3	232

2.19.10.2 Register Descriptions

271. TX_BASE_PTRn: (offset: 0x0000, 0x0010, 0x0020, 0x0030) (n: 0 to 3)

Bits	Type	Name	Description	Initial Value
31:0	RW	TX_BASE_PTR	Tx Base Pointer Points to the base address of TX_Ring n (4-DWORD aligned address).	0x0

272. TX_MAX_CNTn: (offset: 0x0004, 0x0014, 0x0024, 0x0034) (n: 0 to 3)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RW	TX_MAX_CNT	Tx Maximum TXD Count The maximum TXD count in TXD_Ring n.	0x0

273. TX_CTX_IDXn: (offset: 0x0008, 0x0018, 0x0028, 0x0038) (n: 0 to 3)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RW	TX_CTX_IDX	Tx CPU TXD Index 0 Points to the next TXD to be used by the CPU.	0x0

274. TX_DTX_IDXn: (offset: 0x000C, 0x001C, 0x002C, 0x003C) (n: 0 to 3)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RO	TX_DTX_IDX	Tx DMA TXD Index Points to the next TXD to be used by the DMA.	0x0

275. RX_BASE_PTRn: (offset: 0x0100, 0x0110) (n: 0, 1)

Bits	Type	Name	Description	Initial Value
16:0	RW	RX_BASE_PTR	Rx Base Pointer Points to the base address of RXD Ring n (GE ports). It should be a 4-DWORD aligned address.	0x0

276. RX_MAX_CNTn: (offset: 0x0104, 0x0114) (n: 0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RW	RX_MAX_CNT	Rx Maximum Count The maximum RXD count in RXD Ring n.	0x0

277. RX_CALC_IDXn: (offset: 0x0108, 0x0118) (n: 0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
11:0	RW	RX_CALC_IDX	Rx CPU RXD Index Points to the next RXD the CPU will allocate to RXD Ring n.	0x0

278. RX_DRX_IDXn: (offset: 0x010C, 0x011C) (n: 0, 1)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	-
11:0	RW	RX_DRX_IDX	Rx DMA RXD Index Points to the next RXD that the DMA will use in FDS Ring n. It should be a 4-DWORD aligned address.	0x0

279. PDMA_INFO: (offset: 0x0200)

Bits	Type	Name	Description	Initial Value
31:28	RO	VERSION	PDMA controller version.	0x2
27:24	RO	INDEX_WIDTH	Ring Index Width	0xC
23:16	RO	BASE_PTR_WIDTH	Base Pointer Width, x BASE_ADDR[31:32-x] is shared with all ring base address (where x = BASE_PTR_WIDTH). Only ring0's base address [31:32-x] field is writable. 0: No bit of BASE_ADDR is shared.	0x0
15:8	RO	RX_RING_NUM	Rx Ring Number	0x2
7:0	RO	TX_RING_NUM	Tx Ring Number	0x4

280. PDMA_GLO_CFG: (offset: 0x0204)

Bits	Type	Name	Description	Initial Value
31	RW	RX_2B_OFFSET	Rx 2 Byte Offset Sets the byte size of the Rx buffer offset. 0: 4 bytes 1: 2 bytes.	0x0
30	RW	CSR_CLKGATE	Enables Control Status Register Clock Gate 0: PDMA clock operates in free-run mode 1: PDMA clock is gated when idle	0x1
29	RW	BYTE_SWAP	Byte Swap The DMA applies the endian rule to convert the descriptor. 0: Byte swap not applied. 1: Apply byte swap.	0x0
28:9	-	-	Reserved	-
8	RW	DESC_32B	Support 32Byte Descriptor Enables support for a 32 Byte descriptor. 0: Disable 1: Enable	0x0

Bits	Type	Name	Description	Initial Value
7	RW	BIG_ENDIAN	Selects the Endian mode. Sets the PDMA to perform byte swapping on the Tx/Rx packet header and payload. 0: Little endian 1: Big endian	0x0
6	RW	TX_WB_DDONE	Tx Write Back DDONE Enables TX_DMA writing back DDONE into TXD. 0: Disable 1: Enable	0x1
5:4	RW	PDMA_BT_SIZE	PDMA Burst Size Defines the burst size of PDMA. 0: 4 DWORD (16 bytes) 1: 8 DWORD (32 bytes) 2: 16 DWORD (64 bytes) 3: 32 DWORD (128 bytes)	0x1
3	RO	RX_DMA_BUSY	Indicates whether RX_DMA is busy. 0: Not busy 1: Busy	0x0
2	RW	RX_DMA_EN	Rx DMA Enable Enables RX_DMA. When disabled, RX_DMA finishes the current receiving packet, and then stops. 0: Disable 1: Enable	0x0
1	RO	TX_DMA_BUSY	Indicates whether TX_DMA is busy. 0: Not busy 1: Busy	0x0
0	RW	TX_DMA_EN	Tx DMA Enable Enables TX_DMA. When disabled, TX_DMA finishes the current sending packet, and then stops. 0: Disable 1: Enable	0x0

281. PDMA_RST_IDX: (offset: 0x0208)

Bits	Type	Name	Description	Initial Value
31:18	-	-	Reserved	-
17	W1C	RST_DRX_IDX1	Reset RX_DMARX_IDX1 Resets index 1 of the Rx link table to 0.	0x0
16	W1C	RST_DRX_IDX0	Reset RX_DMARX_IDX0 Resets index 0 of the Rx link table to 0.	0x0
15:4	-	-	Reserved	-
3	W1C	RST_DTX_IDX3	Reset TX_DMATX_IDX3 Resets index 3 of the Tx link table to 0.	0x0

Bits	Type	Name	Description	Initial Value
2	W1C	RST_DTX_IDX2	Reset TX_DMATX_IDX2 Resets index 2 of the Tx link table to 0.	0x0
1	W1C	RST_DTX_IDX1	Reset TX_DMATX_IDX1 Resets index 1 of the Tx link table to 0.	0x0
0	W1C	RST_DTX_IDX0	Reset TX_DMATX_IDX0 Resets index 0 of the Tx link table to 0.	0x0

NOTE:

0: Disassert reset

1: Reset

282. DELAY_INT_CFG: (offset: 0x020C)

Bits	Type	Name	Description	Initial Value
31	RW	TXDLY_INT_EN	Tx Delay Interrupt Enable Enables the Tx delayed interrupt mechanism. 0: Disable 1: Enable	0x0
30:24	RW	TXMAX_PINT	Tx Maximum Pending Interrupts Specifies the maximum number of pending interrupts. When the number of pending interrupts is equal to or greater than the value specified here or interrupt pending time has reached the limit (see below), a final TX_DLY_INT is generated. 0: Disable this feature.	0x0
23:16	RW	TXMAX_PTIME	Tx Maximum Pending Time Specifies the maximum pending time for the internal TX_DONE_INT0 and TX_DONE_INT1. When the pending time is equal to or greater than TXMAX_PTIME x 20 μ s or the number of pended TX_DONE_INT0 and TX_DONE_INT1 is equal to or greater than TXMAX_PINT (see above), a final TX_DLY_INT is generated 0: Disable this feature.	0x0
15	RW	RXDLY_INT_EN	Rx Delay Interrupt Enable Enables the Rx delayed interrupt mechanism. 0: Disable 1: Enable	0x0
14:8	RW	RXMAX_PINT	Rx Maximum Pending Interrupts Specifies the maximum number of pending interrupts. When the number of pended interrupts is equal to or greater than the value specified here or the interrupt pending time has reached the limit (see below), a final RX_DLY_INT is generated. 0: Disable this feature.	0x0

Bits	Type	Name	Description	Initial Value
7:0	RW	RXMAX_PTIME	Rx Maximum Pending Time Specifies the maximum pending time for the internal RX_DONE_INT. When the pending time is equal to or greater than RXMAX_PTIME x 20 μ s, or the number of pended RX_DONE_INT is equal to or greater than RXMAX_PCNT (see above), a final RX_DLY_INT is generated. 0: Disable this feature.	0x0

283. FREEQ_THRES: (offset: 0x0210)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	-
3:0	RW	FreeQ_THRES	Free Buffer Queue Threshold Blocks this interface when Rx descriptors reach this threshold.	0x2

284. INT_STATUS: (offset: 0x0220)

Bits	Type	Name	Description	Initial Value
31	RW	RX_COHERENT	Rx Coherent Interrupt Asserts when the Rx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0
30	RW	RX_DLY_INT	Rx Delay Interrupt Asserts when the number of pended Rx interrupts has reached a specified level, or when the pending time is reached. Configure this interrupt using the register.	0x0
29	RW	TX_COHERENT	Tx Coherent Interrupt Asserts when the Tx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0
28	RW	TX_DLY_INT	Tx Delay Interrupt Asserts when the number of pended Tx interrupts has reached a specified level, or when the pending time is reached. Configure this interrupt using the DELAY_INT_CFG register.	0x0
27:18	-	-	Reserved	-
17	RW	RX_DONE_INT1	Rx Queue 1 Done Interrupt Asserts when an Rx packet is received on Queue 1.	0x0
16	RW	RX_DONE_INT0	Rx Queue 0 Done Interrupt Asserts when an Rx packet is received on Queue 0.	0x0
15:4	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
3	RW	TX_DONE_INT3	Tx Queue 3 Done Interrupt Asserts when a Tx Queue 3 packet is transmitted.	0x0
2	RW	TX_DONE_INT2	Tx Queue 2 Done Interrupt Asserts when a Tx Queue 2 packet is transmitted.	0x0
1	RW	TX_DONE_INT1	Tx Queue 1 Done Interrupt Asserts when a Tx Queue 1 packet is transmitted.	0x0
0	RW	TX_DONE_INT0	Tx Queue 0 Done Interrupt Asserts when a Tx Queue 0 packet is transmitted.	0x0

NOTE:

Read:

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

285. INT_MASK: (offset: 0x0228)

Bits	Type	Name	Description	Initial Value
31	RW	RX_COHERENT_INT_MSK	Rx Coherent Interrupt Mask Masks the Rx coherent interrupt, which indicates that the Rx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0
30	RW	RX_DLY_INT_MSK	Rx Delay Interrupt Mask Masks the the Rx delay interrupt, which indicates the number of delayed Rx interrupts has reached a specified level, or when the delay time is reached.	0x0
29	RW	TX_COHERENT_INT_MSK	Tx Coherent Interrupt Mask Masks the Tx coherent interrupt, which indicates the Tx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0
28	RW	TX_DLY_INT_MSK	Tx Delay Interrupt Mask Masks the Tx delay interrupt, which indicates the number of delayed Tx interrupts has reached a specified level, or when the delay time is reached.	0x0
27:18	-	-	Reserved	-
17	RW	RX_DONE_INT_MSK1	Rx Queue 1 Done Interrupt Mask Masks the Rx Queue 1 Done interrupt, which indicates Rx Queue 1 has transmitted a packet.	0x0

Bits	Type	Name	Description	Initial Value
16	RW	RX_DONE_INT_MSK0	Rx Queue 0 Done Interrupt Mask Masks the Rx Queue 0 Done interrupt, which indicates Rx Queue 0 has received a packet.	0x0
15:2	-	-	Reserved	-
3	RW	TX_DONE_INT_MSK3	Tx Queue 3 Done Interrupt Mask Masks the Tx Queue 3 Done interrupt, which indicates Tx Queue 3 has transmitted a packet.	0x0
2	RW	TX_DONE_INT_MSK2	Tx Queue 2 Done Interrupt Mask Masks the Tx Queue 2 Done interrupt, which indicates Tx Queue 2 has transmitted a packet.	0x0
1	RW	TX_DONE_INT_MSK1	Tx Queue 1 Done Interrupt Mask Masks the Tx Queue 1 Done interrupt, which indicates Tx Queue 1 has transmitted a packet.	0x0
0	RW	TX_DONE_INT_MSK0	Tx Queue 0 Done Interrupt Mask Masks the Tx Queue 0 Done interrupt, which indicates Tx Queue 0 has transmitted a packet.	0x0

NOTE:

0: Unmasked

1: Masked

286. SCH_Q01_CFG: Scheduler Configuration for Queue 0 and 1 (offset: 0x0280)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_BKT_SIZE1	Maximum Bucket Size 1 0: The maximum bucket size (burst size allowed in bytes) is equal to one max size packet + the associated max or min rate per 125 μ s. 1: The max bucket size (burst size allowed in byte) is equal to one max size packet + the associated max or min rate per 125 μ s + 2048 bytes.	0x0
30	RW	MAX_RATE_ULMT1	Maximum Rate Limitation 1 0: Enables the max rate limitation function for queue #1. The max rate for queue #1 is defined by MAX_RATE1. 1: Disables the maximum rate limitation function for queue #1. The max rate for queue #1 is unlimited. The scheduler allocates bandwidth to queue #1 based on MAX_WEIGHT1.	0x1

Bits	Type	Name	Description	Initial Value
29:28	RW	MAX_WEIGHT1	Maximum Weight 1 Defines the auto-reload bucket size if MAX_RATE_ULMT1 is set to 1. It also serves as excess bandwidth allocation ratio for servicing queue #1. 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	0x1
27:26	RW	MIN_RATE_RATIO1	Minimum Rate Ratio 1 Defines the guaranteed minimum rate based on MAX_RATE1. 2'b00: MIN_RATE1 = MAX_RATE1 2'b01: MIN_RATE1 = 1/2 MAX_RATE1 2'b10: MIN_RATE1 = 1/4 MAX_RATE1 2'b11: MIN_RATE1 = 0	0x3
25:16	RW	MAX_RATE1	Maximum Rate 1 Defines the limited maximum rate for queue # 1 if MAX_RATE_ULMT1 = 0. The value specified represents the size of 4-byte quota to be added into the queue #1 bucket per 125 μ s. For example, If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125 \mu\text{s} = 16.384 \text{ MBps}$ or 131 Mbps.	0x0
15	RW	MAX_BKT_SIZE0	Maximum Bucket Size 0 0: The maximum bucket size (burst size allowed in bytes) for both maximum and minimum buckets is equal to one maximum size packet + the associated maximum or minimum rate per 125 μ s. 1: The maximum bucket size (burst size allowed in bytes) for both maximum and minimum buckets is equal to one maximum size packet + the associated maximum or minimum rate per 125 μ s + 2048 bytes.	0x0
14	RW	MAX_RATE_ULMT0	Maximum Rate Limitation 0 0: Enables the maximum rate limitation function for queue #0. The maximum rate for queue #0 is defined by MAX_RATE0. 1: Disables the maximum rate limitation function for queue #0. The maximum rate for queue #0 is unlimited. The scheduler allocates bandwidth to queue #0 based on MAX_WEIGHT0.	0x1

Bits	Type	Name	Description	Initial Value
13:12	RW	MAX_WEIGHT0	Maximum Weight 0 Defines the auto-reload bucket size if MAX_RATE_ULMT0 is set to 1. It also serves as excess bandwidth allocation ratio for servicing queue #0. 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	0x0
11:10	RW	MIN_RATE_RATIO0	Minimum Rate Ratio 0 Define the guaranteed minimum rate based on MAX_RATE0. 2'b00: MIN_RATE0 = MAX_RATE0 2'b01: MIN_RATE0 = 1/2 MAX_RATE0 2'b10: MIN_RATE0 = 1/4 MAX_RATE0 2'b110: MIN_RATE0 = 0	0x3
9:0	RW	MAX_RATE0	Maximum Rate 0 Defines the limited maximum rate for queue #0 if MAX_RATE_ULMT0 is 0. The value specified represents the size of 4-byte quota to be added into the queue #0 bucket per 125 μ s. For example, If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes} / 125 \mu\text{s} = 16.384 \text{ MBps}$ or 131 Mbps.	0x0

287. SCH_Q23_CFG: Scheduler Configuration for Queue 2 and 3 (offset: 0x0284)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_BKT_SIZE3	Maximum Bucket Size 3 0: The maximum bucket size (burst size allowed) for both maximum and maximum buckets is equal to one maximum size packet + the associated maximum or minimum rate per 125 μ s. 1: The maximum bucket size (burst size allowed) for both maximum and maximum buckets is equal to one maximum size packet + the associated maximum or maximum rate per 125 μ s + 2048 bytes.	0x0

Bits	Type	Name	Description	Initial Value
30	RW	MAX_RATE_ULMT3	Maximum Rate Limitation 3 0: Enables the maximum rate limitation function for queue #3. The maximum rate for queue #3 is defined by MAX_RATE3. 1: Disables the maximum rate limitation function for queue #3. The maximum rate for queue #3 is unlimited. The scheduler allocates bandwidth to queue #3 based on MAX_WEIGHT3.	0x1
29:28	RW	MAX_WEIGHT3	Maximum Weight 3 Defines the auto-reload bucket size if MAX_RATE_ULMT3 is set to 1. It also serves as excess bandwidth allocation ratio for servicing queue #3. 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	0x3
27:26	RW	MIN_RATE_RATIO3	Minimum Rate Ratio 3 Defines the guaranteed Min rate based on MAX_RATE3. 2'b00: MIN_RATE3 = MAX_RATE3 2'b01: MIN_RATE3 = 1/2 MAX_RATE3 2'b10: MIN_RATE3 = 1/4 MAX_RATE3 2'b11: MIN_RATE3 = 0	0x3
25:16	RW	MAX_RATE3	Maximum Rate 3 Defines the limited maximum rate for queue #3 if MAX_RATE_ULMT3 is 0. The value specified represents the size of the 4-byte quota to be added into the queue #1 bucket per 125 μ s. For example: If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125 \mu\text{s} = 16.384 \text{ MBps}$ or 131 Mbps.	0x0

Bits	Type	Name	Description	Initial Value
15	RW	MAX_BKT_SIZE2	Maximum Bucket Size 2 Defines the limited maximum rate for queue #3 if MAX_RATE_ULMT3 is 0. The value specified represents the size of the 4-byte quota to be added into the queue #1 bucket per 125 μ s. For example: If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125 \mu\text{s} = 16.384 \text{ MBps}$ or 131 Mbps.	0x0
14	RW	MAX_RATE_ULMT2	Maximum Rate Limitation 2 0: Enable the maximum rate limitation function for queue #2. The maximum rate for queue #2 is defined by MAX_RATE0. 1: Disable the maximum rate limitation function for queue #2. The maximum rate for queue #2 is unlimited. The scheduler allocates bandwidth to queue #2 based on MAX_WEIGHT2.	0x1
13:12	RW	MAX_WEIGHT2	Maximum Weight 2 Defines the auto-reload bucket size if MAX_RATE_ULMT0 is set to 1. It also serves as excess bandwidth allocation ratio for servicing queue #2. 2'b00: 1023 bytes 2'b01: 2047 bytes 2'b10: 4095 bytes 2'b11: 8191 bytes	0x2
11:10	RW	MIN_RATE_RATIO2	Minimum Rate Ratio 2 Defines the guaranteed minimum rate based on MAX_RATE0. 2'b00: MIN_RATE2 = MAX_RATE2 2'b01: MIN_RATE2 = 1/2 MAX_RATE2 2'b10: MIN_RATE2 = 1/4 MAX_RATE2 2'b11: MIN_RATE2 = 0	0x3
9:0	RW	MAX_RATE2	Maximum Rate 2 Defines the limited maximum rate for queue #2 if MAX_RATE_ULMT2 is 0. The value specified represents the size of 4-byte quota to be added into the queue #0 bucket per 125 μ s. For example : If 512 is programmed, then the max rate limited is: $512 * 4 \text{ bytes}/125 \mu\text{s} = 16.384 \text{ MBps}$ or 131Mbps.	0x0

2.19.11 MIB Counter Description (base: 0x1010_1000)

Accounting, Meter and GDMA Counter Table

Offset	Name	Description
0x000	PPE_AC_BCNT0	PPE Accounting Group #0 Byte Counter
0x004	PPE_AC_PCNT0	PPE Accounting Group #0 Packet Counter
....		
0x1F8	PPE_AC_BCNT63	PPE Accounting Group #63 Byte Counter
0x1FC	PPE_AC_PCNT63	PPE Accounting Group #63 Packet Counter
0x200	PPE_MTR_CNT0	PPE Meter Group #0
....		
0x2FC	PPE_MTR_CNT63	PPE Meter Group #63
0x300	GDM1_TX_GBCNT	Transmit good byte count for CPU GDM
0x304	GDM1_TX_GPCNT	Transmit good packet count for CPU GDM (exclude flow control frames)
0x308	GDM1_TX_SKIPCNT	Transmit abort count for CPU GDM
0x30C	GDM1_TX_COLCNT	Transmit collision count for CPU GDM
0x310 – 0x31C	Reserved	-
0x320	GDM1_RX_GBCNT1	Received good byte count for CPU GDM
0x324	GDM1_RX_GPCNT1	Received good packet count for CPU GDM (exclude flow control frame)
0x328	GDM1_RX_OERCNT	Received overflow error packet count for CPU GDM
0x32C	GDM1_RX_FERCNT	Received FCS error packet count for CPU GDM
0x330	GDM1_RX_SERCNT	Received too short error packet count for CPU GDM
0x334	GDM1_RX_LERCNT	Received too long error packet count for CPU GDM
0x338	GDM1_RX_CERCNT	Received IP/TCP/UDP checksum error packet count for CPU GDM
0x33C	GDM1_RX_FCCNT	Received flow control pkt count for CPU GDM
0x340	GDM2_TX_GBCNT	Transmit good byte count for PPE GDM
0x344	GDM2_TX_GPCNT	Transmit good packet count for PPE GDM (exclude flow control frames)
0x348	GDM2_TX_SKIPCNT	Transmit abort count for PPE GDM
0x34C	GDM2_TX_COLCNT	Transmit collision count for PPE GDM
0x350 – 0x35C	Reserved	-
0x360	GDM2_RX_GBCNT	Received good byte count for PPE GDM
0x364	GDM2_RX_GPCNT	Received good packet count for PPE GDM (exclude flow control frame)
0x368	GDM2_RX_OERCNT	Received overflow error packet count for PPE GDM
0x36C	GDM2_RX_FERCNT	Received FCS error packet count for PPE GDM
0x370	GDM2_RX_SERCNT	Received too short error packet count for PPE GDM
0x374	GDM2_RX_LERCNT	Received too long error packet count for PPE GDM

Offset	Name	Description
0x378	GDM2_RX_CERCNT	Received IP/TCP/UDP checksum error packet count for PPE GDM
0x37C	GDM2_RX_FCCNT	Received flow control pkt count for PPE GDM

2.20 Ethernet Switch

2.20.1 Features

- IEEE 802.3 full duplex flow control
- 5x10/100 Mbps PHY
- Supports Spanning Tree port (STP) states
 - IEEE 802.1w Rapid Spanning Tree
 - IEEE 802.1s Multiple Spanning Tree with up to 8 spanning tree instances
- 2 K entries MAC address table indexed by 48-bit MAC address XOR hash
 - Static entries are accessible through registers.
 - IVL/SVL support based on IVL and FID from VLAN table
 - Programmable aging timer – no aging out, 10 to 1 000 000 seconds; default is 300 sec.
- QoS
 - Four priority queues per port and eight priority queues on port 6
 - Packet classification based on incoming port, IEEE 802.1p or IP ToS/DSCP, and ACL rules
 - Per port ingress and egress rate limit control stepping in 64 Kbps steps up to 1 Gbps
 - Per queue MAX-MIN bandwidth control with different schedulers – strict priority (SP), weighted fair queue (WFQ), and mixed SP/WFQ
 - User priority remapping and DSCP remarking
- 16 VLAN ID
 - Port and protocol-based VLAN
 - 802.1q tag VLAN
 - Double VLAN tagging (O in O)
 - Per egress port 1:1 and N:1 VLAN translation
 - Leaky VLAN support
- 32 ACL Rules from Layer 1 to Layer 4
 - Rules include port no., DA/SA, Ether Type, VLAN ID, IP Protocol, SIP/DIP, TCP/UDP, SP/DP and user-defined content
 - Actions support mirror, redirect, dropping, priority adjustment, and traffic rate policing
 - Optional per-port enable/disable of ACL function
- MAC security – Locking a MAC address to an incoming port
 - Disable learning or aging
 - Limit SA learning number
- IEEE 802.1x access control protocol
 - Access policy based on port, MAC address and guest VLAN
 - Access control based on ACL rules
 - Drop frames with unknown source MAC or destination MAC address
- IGMP/MLD snooping support
 - Supports IPv4 IGMP v1/v2 and IPv6 MLD v1 hardware snooping
 - Supports IPv4 IGMP v3 and IPv6 MLD v2 partial snooping – IS_EX(), TO_EX(), TO_IN()
- Broadcast/Multicast/Unknown DA storm prevention

2.20.2 Block Diagram

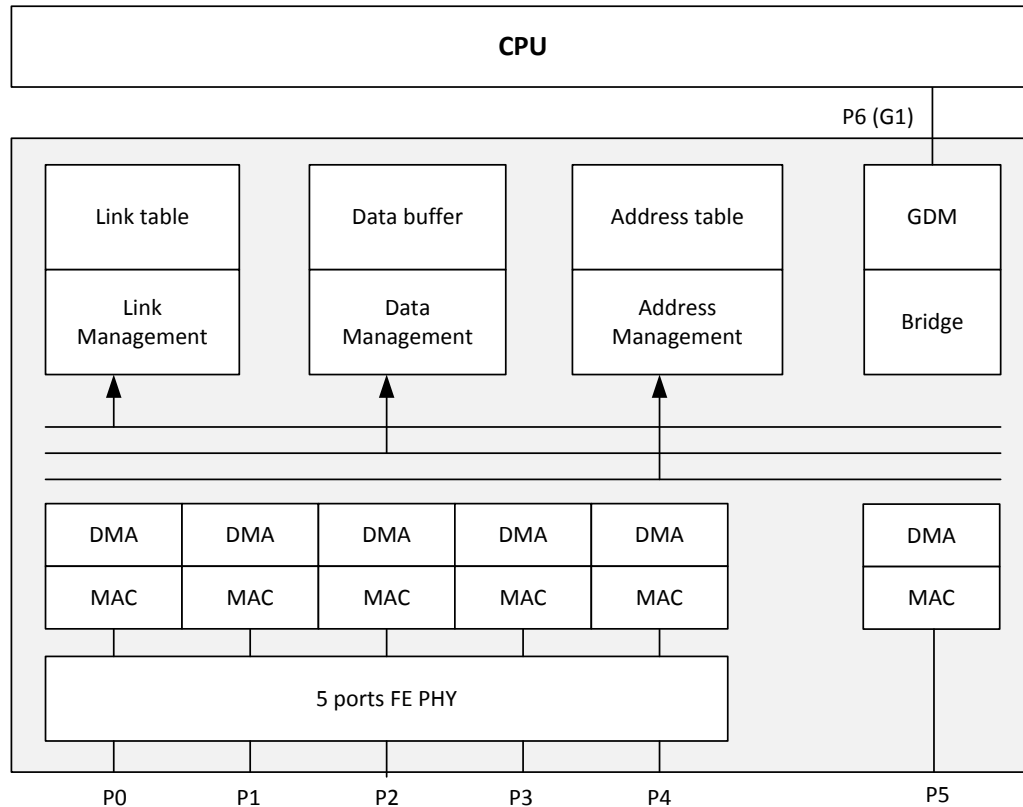


Figure 2-29 Ethernet Switch Block Diagram

2.20.3 Frame Classification

2.20.3.1 Broadcast Frames

FTAG	DA	Type	Description
BC	FF-FF-FF-FF-FF-FF	-	Broadcast Frames
ARP	FF-FF-FF-FF-FF-FF	08-06	ARP Request Frames
	-	08-06	ARP Reply Frames
RARP	FF-FF-FF-FF-FF-FF	80-35	RARP Request Frames
	-	80-35	RARP Reply Frames

2.20.3.2 Multicast Frames

FTAG	DA	Type	IP4/IP6 Protocol	Description
MC	The first bit of MSB is 1'b1.	-	-	Multicast Frames
IGMP	-	08-00	0x02	IGMP Message
IP_MULT	01-00-5E-xx-xx-xx	-	-	IP Multicast (UDP)
MLD	-	86-DD	0x00 0x3A	Hop-by-Hop ICMPv6 (MLDv2)
IPV6_MULT	33-33-xx-xx-xx-xx	-	-	IPv6 Multicast (UDP)
BPDU	01-80-C2-00-00-00	-	-	Bridge Group Address (BPDU)
REV_01	01-80-C2-00-00-01	-	-	Clause 31 (MAC Control) of IEEE Std 802.3
CONTROL (PAUSE)	-	88-08	-	Discarded
	01-80-C2-00-00-01 or Unicast DA	88-08	Followed by 00-01	MAC Control -Pause Frame (< 1518 bytes) (Discarded)
REV_02	01-80-C2-00-00-02	-	-	Clause 43 (Link Aggregation) and Clause 57 (OAM) of IEEE Std 802.3
PAE	01-80-C2-00-00-03 or Other	88-8E	-	IEEE Std 802.1X PAE address
REV_03	01-80-C2-00-00-03	-	-	
REV_UN	01-80-C2-00-00-04 to 05	-	-	Reserved for future standardization—media access method specific
	01-80-C2-00-00-06 to 0D	-	-	Reserved for future standardization—VLAN-aware Bridge specific
REV_0E	01-80-C2-00-00-0E			IEEE Std 802.1AB Link Layer Discovery Protocol multicast address
REV_UN	01-80-C2-00-00-0F			Reserved for future standardization—VLAN-aware Bridge specific
REV_10	01-80-C2-00-00-10			All LANs Bridge Management Group Address
REV_20	01-80-C2-00-00-20			GMRP Address
REV_21	01-80-C2-00-00-21			GVRP Address
REV_UN	01-80-C2-00-00-22 to 01-80-C2-00-00-xx	-	-	Reserved for future standardization

2.20.3.3 Unicast Frames

FTAG	DA	Type	Description
UC	The 1st bit of MSB is 1'b0	-	Unicast Frames
ARP	FF-FF-FF-FF-FF-FF	08-06	ARP Request Frames
	-	08-06	ARP Reply Frames
RARP	FF-FF-FF-FF-FF-FF	80-35	RARP Request Frames
	-	80-35	RARP Reply Frames

2.20.4 Switch L2/L3 Address Table

The switch has a 2 K address table built in for packet look-up forwarding. All the entries can be shared and mixed by L2 MAC address or L3 IP address according to "TYPE" definition. When the entry is regarded as a MAC address table, it is used to forward packets by L2 DA and learn packets by L2 SA. When the entry is regarded as a DIP address table, it is used to process IGMP/MLD snooping. To support IGMPv3/MLDv2, a SIP entry is added to search the Source IP list after DIP look-up.

2.20.4.1 MAC address table

Bytes	Bits	Name	Description
7:0	11:0	CVID	Customer VID [11:0] Customer VLAN ID is learned automatically from VLAN tag or port-based register PPBV#.PORT_VID.
	14:12	FID	Filter ID[2:0] Filter ID is learned automatically from VLAN Table. 0 is the default value if VLAN Table is not applicable.
	15	IVL	Independent VID Learning IVL is learned automatically from VLAN Table. 0 is the default value if VLAN Table is not applicable.
	63:16	ADDRESS	MAC Address[47:0] 48-bit MAC Physical Address is searched by Destination MAC Address and learned from Source MAC Address.
3:0	1:0	TYPE	Layer2/Layer3 Address Entry Type 2'b00: MAC Address Entry 2'b01: DIP Address Entry. 2'b10: Source IP Address Table (See Table 3-28) 2'b11: Reserved
	3:2	STATUS	Address Entry Live Status 2'b00: Entry is empty 2'b01: Entry is dynamic and valid 2'b10: Reserved 2'b11: Entry is static and cannot be aged out or changed by hardware.
	11:4	PORT / FILTER	Destination Port Map Bit4 : Port 0 ... Bit11: Port 7 NOTE: Frame dropped by DA Address through PORT=6'b0.

Bytes	Bits	Name	Description
	12	LEAKY_EN	Leaky VLAN Enable 1'b0: This frame address will be blocked by VLAN (default) 1'b1: This frame address can pass through VLAN NOTE: Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MFC.UC_ARL_LKYV or MFC.MC_ARL_LKYV.
	15:3	EG_TAG	Egress VLAN Tag Attribution 3'b000: System default (Default) 3'b001: Consistent 3'b010,3'b011: Reserved 3'b100: Untagg 3'b101: Swap 3'b110: Tagged 3'b111: Stack
	18:6	USR_PRI	User Priority from Address Table 0: Default
	19	SA_MIR_EN	Source Address Hit to Mirror port 1'b0: No action (default) 1'b1: Frame is copied to mirror port when SA hit
	22:20	SA_PORT_FW	Source Address Hit Frame TO_CPU Forwarding 3'b0xx: System Default (Disable) 3'b100: System Default and CPU Port Excluded 3'b101: System Default and CPU Port Included 3'b110: CPU Port Only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
	23	-	Reserved
	31:24	TIMER	Age Timer Programmable age timer. The age duration can be set from 1 to 1,000,000 seconds. The field value will be reset to the register AAC.AGE_CNT and counted down by one every AAC.AGE_UNIT seconds.

2.20.4.2 DIP address table

Bytes	Bits	Name	Description
7:0	15:0	RESP_CNT	Response Counter[15:0] A response counter for each port is used to count the number of consecutive No IGMP Report Messages received before the Response Timer counts to zero. Bit[49:48]: Port 0 ... Bit[63:62]: Port 7
	23:16	RESP_FLAG	Response Flag[7:0] After receiving the Group Query or Group Specific Query, this flag is used to record any IGMP report message received for the corresponding port before the response interval counts to zero. Bit40: Port 0 ... Bit47: Port 7
	31:24	RESP_TIMER	Response Timer[7:0] This timer is set according to the maximum response time field in the General Specific Query message and counts down every 1 second. The default timer for the General Query message(=0x0) is 10 seconds.
	63:32	ADDRESS	IP Multicast Destination IP Address[31:0] The latest 32-bit DIP(GA) for IPv4 or IPv6 packets
3:0	1:0	TYPE	Layer2/Layer3 Address Entry Type 2'b00: MAC Address Entry 2'b01: DIP Address Entry. 2'b10: Source IP Address Table (See 3.3.2) 2'b11: Reserved
	3:2	STATUS	Address Entry Live Status 2'b00: Group entry is empty 2'b01: Group entry is dynamically valid whenever any IGMP report message received before the response timer counts to zero and the response counter is not bigger than the robustness variable. 2'b10: Entry is static and the final port map will result from the SIP table search. 2'b11: Entry is static and can not be aged out or changed by hardware.
	11:4	PORT / FILTER	Destination Port Map or Filter Mode for IGMPv3/MLDv2 Bit4: Port 0 ... Bit11: Port 7
	12	LEAKY_EN	Leaky VLAN Enable 1'b0: This frame address will be blocked by VLAN (default) 1'b1: This frame address can pass through VLAN NOTE: Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MFC.UC_ARL_LKYV or MFC.MC_ARL_LKYV.

Bytes	Bits	Name	Description
	15:13	EG_TAG	Egress VLAN Tag Attribution 3'b000: System default (Default) 3'b001: Consistent 3'b010 to 3'b011: Reserved 3'b100: Untagg 3'b101: Swap 3'b110: Tagged 3'b111: Stack
	18:16	USR_PRI	User Priority from IGMP Table 0: Default
	31:19	-	Reserved

2.20.4.3 SIP address table

Bytes	Bits	Name	Description
7:0	31:0	SIP_ADR	IP Multicast Source IP Address [31:0] The latest 32-bit IPv4 or IPv6 source address
	63:32	DIP_ADR	IP Multicast Destination IP Address [31:0] The latest 32-bit IPv4 or IPv6 destination or group address
3:0	1:0	TYPE	Layer2/Layer3 Address Entry Type 2'b00: MAC Address Entry 2'b01: DIP Address Entry 2'b10: Source IP Address Table (See 3.3.2) 2'b11: Reserved
	3:2	STATUS	Address Entry Live Status 2'b00: Group entry is empty 2'b01 to 10: Reserved 2'b11: Entry is static and can not be aged out or changed by hardware
	11:4	PORT_MAP	Port Member Bit.4: Port 0 ... Bit.1: Port 7
	31:19	-	Reserved

2.20.5 Virtual LAN

2.20.5.1 VLAN Table

Bits	Name	Description
0	VALID	VLAN Entry Valid
3:1	FID	Filtering Database 3'h0: Default FID for all MAC addresses ... 3'h7
15:4	S_TAG1	(1) Service Tag Identification 12-bit Service Tag ID for VLAN translation or Stack VLAN (2) Service Tag Index bit[6:4]: Port 0 STAG index bit[9:7]: Port 1 STAG index bit[12:10]: Port 2 STAG index bit[15:13]: Port 3 STAG index
23:16	PORT_MEM	VLAN Member Control Port 0 - Bit 0: VID Port Member ... Port 7 - Bit 7: VID Port Member NOTE: Frame dropped through PORT=6'b0.
26:24	USER_PRI	Service Tag User Priority Value from VLAN Table
27	COPY_PRI	Copy User Priority Value from Customer Priority Tag for Service Tag
28	VTAG_EN	Per VLAN Egress Tag Control Enable per-VLAN egress tag attribute by EG_CON and EG_TAG
29	EG_CON	Egress Tag Consistent Keep the original ingress tag attribute. NOTE: When the EG_CON is set, EG_TAG will be invalid for the outgoing frames.
30	IVL_MAC	MAC Address Learned by Individual CVID 1'b0: MAC address will be learned by MAC and FID 1'b1: MAC address will be learned by MAC and CVID
31	PORT_STAG	Port-based STAG 1'b0: S_TAG1 shows 12-bit VID 1'b1: S_TAG1 and S_TAG2 show 3-bit STAG index on per port.
47:32	EG_TAG	VLAN Egress Tag Control Bit.41 to Bit.40 (Port 0) – 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack ... Bit.55 to Bit.54 (Port 7)

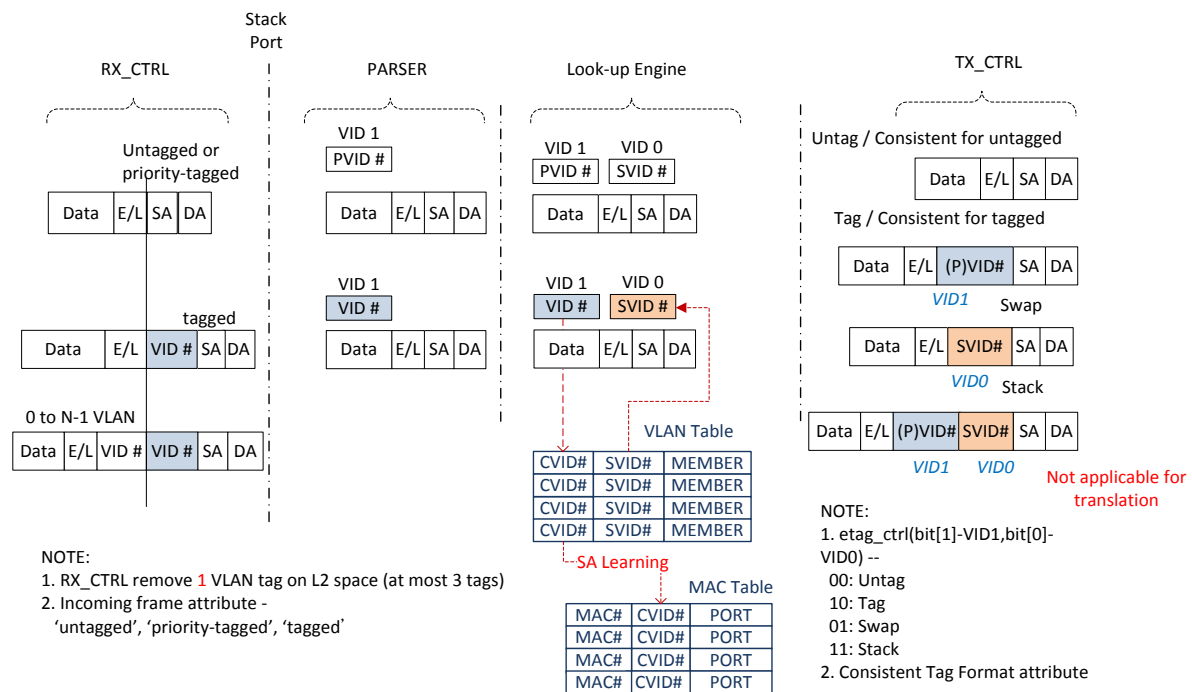
Bits	Name	Description
59:48	S_TAG2	(2) Service Tag Index b[50:48]: Port 4 STAG index b[53:51]: Port 5 STAG index b[56:54]: Port 6 STAG index b[59:57]: Port 7 STAG index

2.20.5.2 VLAN tagging

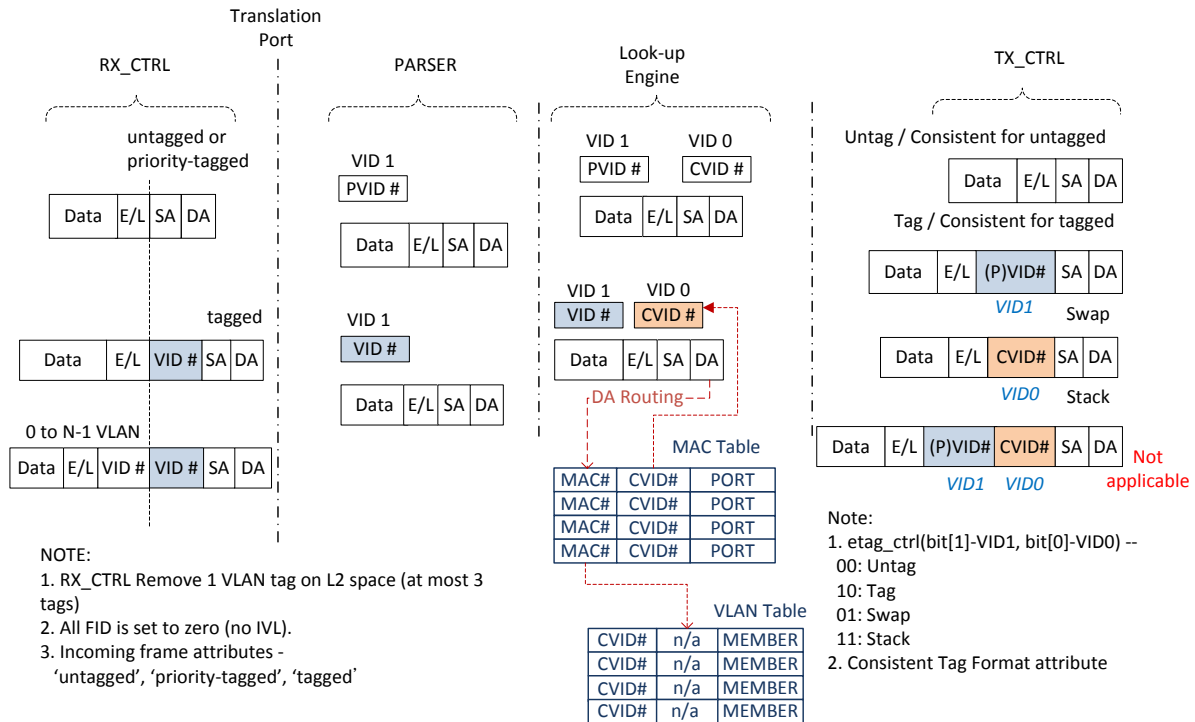
The switch can support customer and service VLAN tags (inner/ outer VLAN tags) inside a frame. When a frame is incoming, its VLAN tags will be stripped by one or two based on different ingress port attributes – PVC.VLAN_ATTR. Similarly, their tags will be used for VLAN table search or MAC table search according to the incoming port attribute.

Finally, the per-port egress tag control will be carried on the TX_CTRL side. The transmitted frame will follow the egress control and carry the processed VLAN tags - VID0 (service tag) and VID1 (customer tag).

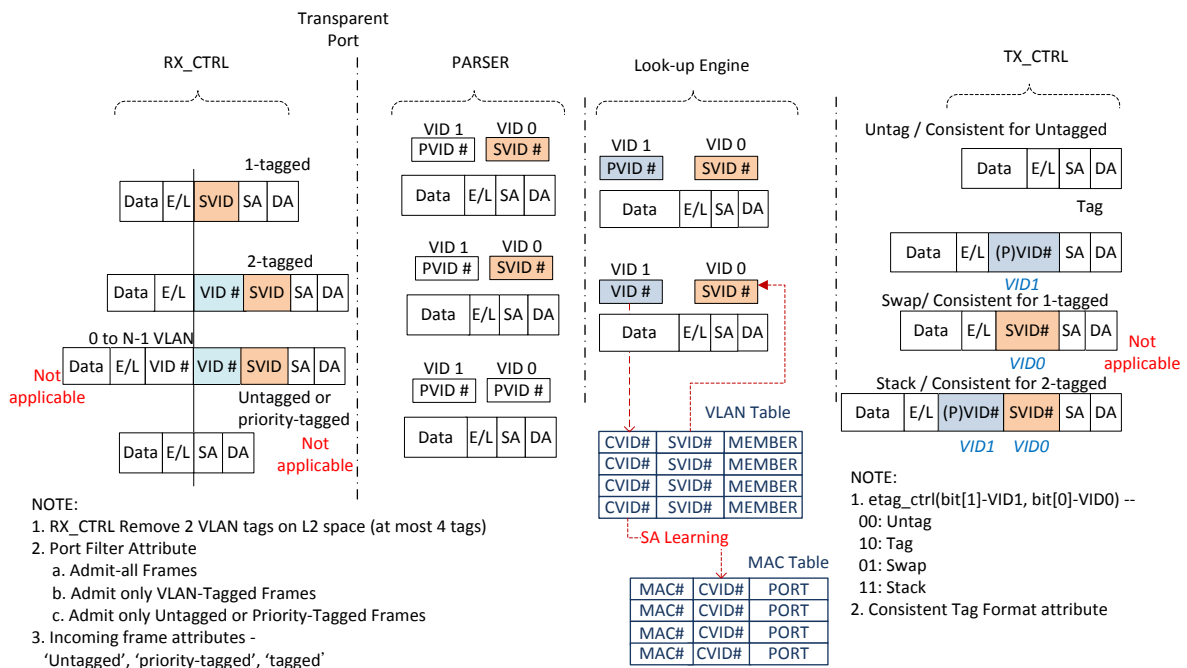
2.20.5.3 User port



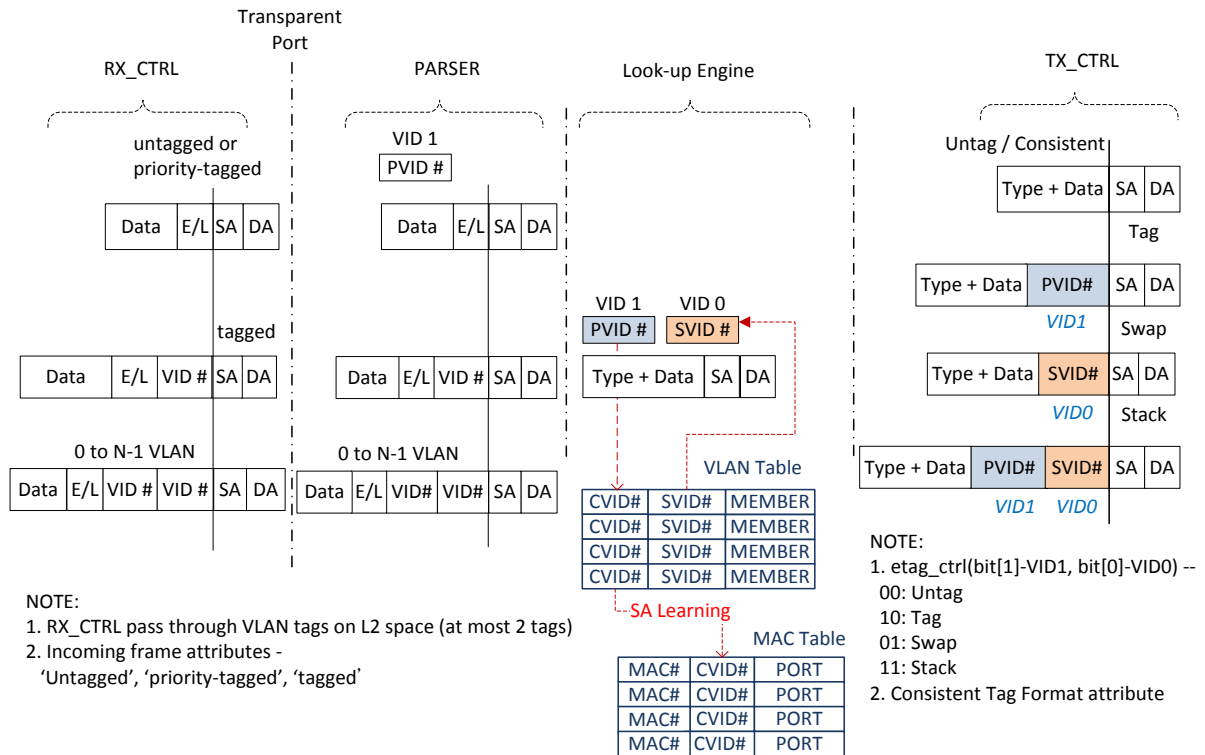
2.20.5.4 Translation port



2.20.5.5 Stack port



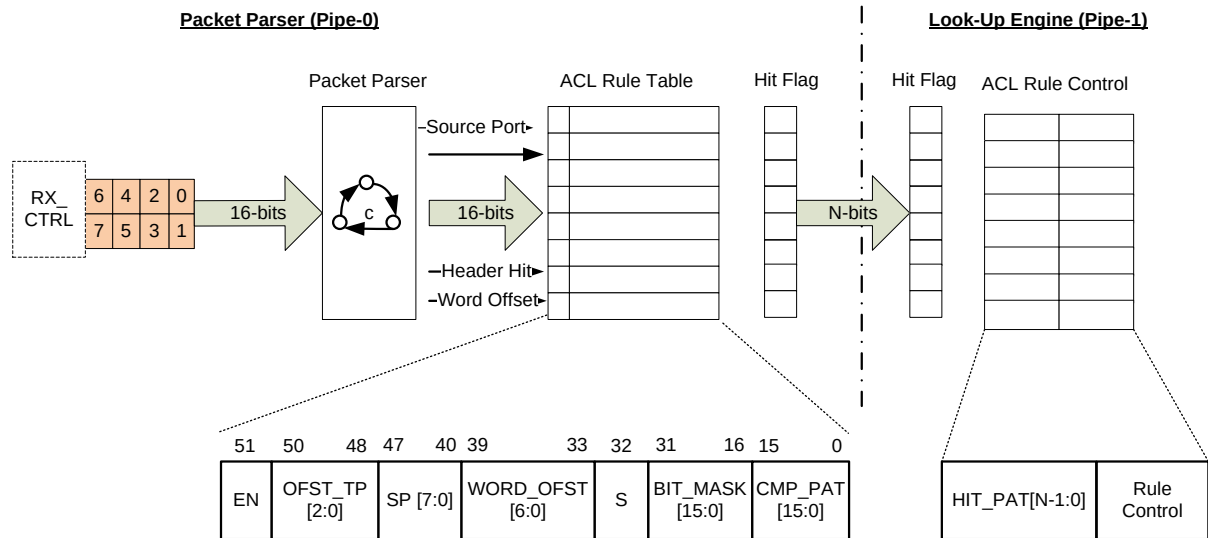
2.20.5.6 Transparent port



2.20.6 Access Control Logic

ACL Rule Control is a 32-entry table with a linear look-up engine. Each packet can find single or multiple hit entries from the ACL rule control. For general packet control, the first hit entry will be taken and followed on the packet process. As for the rate limit, multiple entries can be applied to the same packet.

2.20.6.1 ACL Block Diagram



2.20.6.2 ACL Rule Table

Bytes	Bits	Name	Description
1:0	15:0	CMP_PAT	Comparison Pattern This field contains the 16-bit data comparison pattern.
3:2	15:0	BIT_CMP	Comparison Pattern Validation This field shows whether the bit-map comparison is valid for the corresponding CMP_PAT bit. 0: Not valid 1: Valid
4	0	RES	Reserved
	7:1	WORD_OFST	Word Offset 2-byte offset in the corresponding OFST_TP. NOTE: 0x3F is the reserved and invalid offset value.
5	7:0	SP	Physical Source Port Bitmap SP[7:0]: Port 7 to port 0
6	2:0	OFST_TP	Format Type for Word Offset Range 3'b000: MAC Header (including VLAN tags and Length/Type) (L2 Offset) 3'b001: L2 Payload (L2 Offset) 3'b010: IP Header (L3 Offset) 3'b011: IP Datagram (L3 Offset) 3'b100: TCP/UDP Header (L4 Offset) 3'b101: TCP/UDP Datagram (L4 Offset) 3'b110: IPv6 Header (L3 Offset) 3'b111: Reserved
	3	EN	ACL Valid Bit

2.20.6.3 ACL Rule Control

Table 2-3 Rule Mask

Bytes	Bits	Name	Description
7:0	63:0	HIT_PAT	Hit Pattern When a valid bit is set in this table, it means that the corresponding pattern in the rule table must be hit and necessary. If all the valid bits can be found in the rule flag, then the rule control can be applied on this packet.

Table 2-4 Rate Control

Bytes	Bits	Name	Description
1:0	13:0	RATE	Per Flow Ingress Rate Limit Control Per the rate limit, multiple rule controls can constrain one packet. Generally, the minimum ingress rate will limit the flow rate. 14'h0: 0 * 64 Kbps 14'h1: 1 * 64 Kbps 14'h2: 2 * 64 Kbps ... 14'h3D09: 15625 * 64 Kbps (1000 Mbps)
	14	RES	Reserved
	15	RATE_EN	Per Flow Ingress Rate Limit Enable (Multi/First)
3:2	14:0	RATE_ACCU	Per Flow Ingress Rate Limit Accumulator
	15	-	Reserved

Table 2-5 Rule Control

Bytes	Bits	Name	Description
0	2:0	PORT_FW	Frame TO_CPU Forwarding 3'b0xx: System Default (Disable) 3'b100: System Default and CPU Port Excluded 3'b101: System Default and CPU Port Included 3'b110: CPU Port Only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
	3	MIR_EN	Frame Copy to Mirror Port
	6:4	PRI_USER	User Priority from ACL
	7	PORT_EN	Force Destination Port Selection 1'b0: Destination port is based on ARL or register 1'b1: Destination port is based on PORT.
1	7:0	PORT	Destination Port Member / VLAN Port Member

Bytes	Bits	Name	Description
2	2:0	EG_TAG	Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
	3	LKY_VLAN	Leaky VLAN
	4	PPP_RM	PPPoE Header Removal
	5	SA_SWAP	Source MAC Address Swap
	6	DA_SWAP	Multicast MAC Destination Address Swap IPv4: 01-00-5E-xx-xx-xx (From Destination IP) IPv6: 33-33-xx-xx-xx-xx (From Destination IP)
	7	VLAN_PORT_EN	Swap VLAN Port Member with PORT
2	2:0	CNT_IDX	Counter Group Index
	3	ACL_CNT_EN	Enable ACL Hit Count (Multi/First)
	4	INT_EN	Interrupt Enable (Multi/First)
	5	ACL_MANG	Management Frame Attribute
	7:6	-	Reserved
3 (Counter)	2:0	CNT_IDX	Counter Group Index
	3	ACL_CNT_EN	Enable ACL Hit Count (Multi/First)
	4	INT_EN	Interrupt Enable (Multi/First)
	5	ACL_MANG	Management Frame Attribute
	7:6	-	Reserved
6:4 (trTCM)	0	DROP_PCD_SEL	Select s the original drop precedence value or ACL control table defined drop precedence value
	1	CLASS_SLR_SEL	Selects the original class_selector value or ACL control table defined class selector value
	4:2	CLASS_SLR	User defined class selector
	7:5	DROP_PCD_R	User defined drop precedence value for red color packet
	2:0	DROP_PCD_Y	User defined drop precedence value for yellow color packet
	5:3	DROP_PCD_G	User defined drop precedence value for green color packet
	6	RED_DROP_R	Red color packet drop according to RED engine. If this bit is reset, the drop precedence is depending on ABS_DROP_R.
	7	ABS_DROP_R	Red color packet drop absolutely.
	0	RED_DROP_Y	Yellow color packet drop according to RED engine. If this bit is reset, the drop precedence is depending on ABS_DROP_Y.
	1	ABS_DROP_Y	Yellow color packet drop absolutely
	2	RED_DROP_G	Green color packet drop according to RED engine
	7:3	ACL_CLASS_IDX	Class index for the 32-entries Meter Table

Table 2-6 trTCM Meter Table

Bytes	Bits	Name	Description	Initial Value
63:48	RW	CIR	Committed Information Rate 16'h0: 0 * 64 Kbps 16'h1: 1 * 64 Kbps ... 16'hFFFF: 65536* 64 Kbps NOTE: 1 * 64 Kbps means that ACL will add 1 token (1-Byte) to the CBS burst bucket every 125 μ s.	0x0
47:32	RW	PIR	Peak Information Rate 16'h0: 0 * 64 Kbps 16'h1: 1 * 64 Kbps ... 16'hFFFF: 65536* 64 Kbps NOTE: 1 * 64 Kbps means that ACL will add 1 token (1-Byte) to the PBS burst bucket every 125 μ s.	0x0
31:16	RW	CBS	Committed Burst Size The maximum number of bytes allowed for incoming packets to burst above the CIR, but still be marked green. The CBS burst size should be larger than CIR for token added.	0x0
15:0	RW	PBS	Peak Burst Size The maximum number of bytes allowed for incoming packets to burst above the CIR and still be marked yellow. The PBS burst size should be larger than PIR for token added.	0x0

2.20.7 ARL Registers (base: 0x1011_0000)

2.20.7.1 List of Registers

No.	Offset	Register Name	Description	Page
288	0x0000	MISC1	MISC I Register	254
289	0x0004	PFC	PPE Forward Control Register	254
290	0x0008	AISR	ACL Interrupt Status Register	254
291	0x000C	AGC	ARL Global Control Register	254
292	0x0010	MFC	MAC Forward Control Register	255
293	0x0014	VTC	VLAN TAG Control Register	256
294	0x0018	ISC	IGMP Snooping Control Register	257
295	0x001C	IMC	IGMP/MLD Message Control Register	258
296	0x0020	APC	ARP and PPPoE Control Register	260
297	0x0024	BPC	BPDU and PAE Control Register	262
298	0x0028	RGAC1	REV_01 and REV_02 Control Register	264
299	0x002C	RGAC2	REV_03 and REV_0E Control Register	266
300	0x0030	RGAC3	REV_10 and REV_20 Control Register	267
301	0x0034	RGAC4	REV_21 and REV_UN Register	269
302	0x0038	PMC	Protocol Match Control Register	271
303	0x003C	PBG1	Protocol Based Group ID-I Register	272
304	0x0040	PBG2	Protocol Based Group ID-II Register	272
305	0x0044	UPW	User Priority Weight Register	272
306	0x0048	PEM1	User Priority Egress Mapping I Register	272
307	0x004C	PEM2	User Priority Egress Mapping II Register	273
308	0x0050	PEM3	User Priority Egress Mapping III Register	273
309	0x0054	PEM4	User Priority Egress Mapping IV Register	273
310	0x0058	PIM1	DSCP Priority Ingress Mapping I Register	274
311	0x005C	PIM2	DSCP Priority Ingress Mapping II Register	274
312	0x0060	PIM3	DSCP Priority Ingress Mapping III Register	274
313	0x0064	PIM4	DSCP Priority Ingress Mapping IV Register	275
314	0x0068	PIM5	DSCP Priority Ingress Mapping V Register	275
315	0x006C	PIM6	DSCP Priority Ingress Mapping VI Register	275
316	0x0070	PIM7	DSCP Priority Ingress Mapping VII Register	276
317	0x0074	ATA1	Address Table Access I Register	276
318	0x0078	ATA2	Address Table Access II Register	276
319	0x007C	ATWD	Address Table Write Data Register	277
320	0x0080	ATC	Address Table Control Register	277
321	0x0084	TSRA1	Table Search Read Address-I Register	279
322	0x0088	TSRA2	Table Search Read Address-II Register	279
323	0x008C	ATRD	Address Table Read Data Register	279

324	0x0090	VTCT	VLAN Table Control Register	280
325	0x0094	VAWD1	VLAN and ACL Write Data-I Register	281
326	0x0098	VAWD2	VLAN and ACL Write Data-II Register	283
327	0x009C	TRTCM	Two Rate Three Color Mark Register	284
328	0x00A0	AAC	Address Age Control Register	285
329	0x00A4	DHCP	DHCPv4 and DHCPv6 Control Register	285
330	0x0100	VTIM1	VID to Table Index Map 1 Register	287
331	0x0104	VTIM2	VID to Table Index Map 2 Register	287
332	0x0108	VTIM3	VID to Table Index Map 3 Register	287
333	0x010C	VTIM4	VID to Table Index Map 4 Register	288
334	0x0110	VTIM5	VID to Table Index Map 5 Register	288
335	0x0114	VTIM6	VID to Table Index Map 6 Register	288
336	0x0118	VTIM7	VID to Table Index Map 7 Register	288
337	0x011C	VTIM8	VID to Table Index Map 8 Register	288
338	0x0200	DBGC	Debug Control Register	288
339	0x0204	DBGD1	Debug Data-I Register	290
340	0x0208	DBGD2	Debug Data-II Register	290
341	0x020C	DBGCNT	Debug Counter Register	290

2.20.7.2 Register Descriptions

288. MISC1: MISC I Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:0	-	-	Reserved	0x0

289. PFC: PPE Forward Control Register (offset: 0x0004)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	0x0
3	RW	PPE_EN	PPE Port Enable 1'b0: No PPE 1'b1: Enable PPE port	0x0
2:0	RW	PPE_PORT	PPE Port Number Sets the PPE port number. 3'h0: Port 0 ... 3'h7: Port 7	0x0

290. AISR: ACL Interrupt Status Register (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:0	W1C	ACL_ISR	32 ACL Interrupt Status (Refer to ACL_Rule_Control)	0x0

291. AGC: ARL Global Control Register (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:19	-	-	Reserved	0x0
18	RO	ACL_INIT	Access Control List (ACL) Table Initialization Done 1'b0: ACL Table is busy. 1'b1: ACL Table is cleared	0x1
17	RO	VLAN_INIT	VLAN Table Initialization Done 1'b0: VLAN Table is busy. 1'b1: VLAN Table is cleaned.	0x1
16	RO	ADDR_INIT	ADDR Table Initialization Done 1'b0: ADDR Table is busy. 1'b1: ADDR Table is cleaned.	0x1
15	RW	RATE_COMP	Rate Limit Compensation Add or subtract the specific byte number while calculating the packet length. 1'b0: Add 1'b1: Minus	0x0
14:8	RW	COMP_BNUM	Compensation Byte Number The added/subtracted byte number for the rate limit or the meter table.	0x18

Bits	Type	Name	Description	Initial Value
7	RW	LOCAL_EN	Local Port Forwarding Enable 1'b0: Drop frames at the local port. 1'b1: Allow frame forwarding to the local port.	0x0
6	RW	ARL_PADDING	ARL Data Padding Sets ARL to add byte padding up to 46 bytes when the length of the data field of the incoming frame is less than 46 bytes. 1'b0: Disable (default) 1'b1: Enable	0x0
5	RW	ACL_MULTI	Enable Multiple ACL Hit 1'b0: Only the first hit ACL entry 1'b1: Allow multiple ACL hit entries on Rate, Interrupt, and MIB.	0x0
4	RW	L2LEN_CHK	Layer 2 Frame Length Check Enables a length check on length-encapsulated frame. Drops length error frames when the value of the ELEN field of this frame is bigger than the length of the data field. 1'b0: Disable 1'b1: Enable	0x1
3	RW	CTRL_DROP	MAC Control Frame Drop Drops MAC control frames with ETYPE=0x8808. 1'b0: Disable (default) 1'b1: Enable	0x1
2	RW	VLAN4CPU	TO_CPU VLAN Member Sets the TO_CPU frame to check VLAN members. 1'b0: Ignore VLAN members. 1'b1: Check VLAN members.	0x0
1	RW	ARL_PRI	ARL Resolution Priority 1'b0: P0 is the lowest priority. 1'b1: P0 is the highest priority.	0x0
0	RW	ARL_RST_N	ARL Enable (Soft Reset) 1'b0: Reset the ARL engine. 1'b1: Enable ARL engine.	0x1

292. MFC: MAC Forward Control Register (offset: 0x0010)

Bits	Type	Name	Description	Initial Value
31:24	RW	BC_FFP	Broadcast Frame Flooding Ports If MAC receives broadcast frames, this field indicates the flooding ports. NOTE: 1. The flooding port excludes the received port on the switch. 2. Frame dropped though BC_FFP=6'b0.	0x7F

Bits	Type	Name	Description	Initial Value
23:16	RW	UNM_FFP	Unknown Multicast Frame Flooding Ports If MAC receives multicast frames which can not be found on the ARL, this field indicates the flooding ports. NOTE: 1. The flooding port will exclude the received port by HW. 2. Frame dropped though UNM_FFP=6'b0.	0x7F
15:8	RW	UNU_FFP	Unknown Unicast Frame Flooding Ports If MAC receives the unicast or multicast frames which can not be found on the ARL. The field indicates the flooding port. NOTE: 1. The flooding port will excludes the received port by HW) 2. Frame dropped though UNM_FFP=6'b0)	0x7F
7	RW	CPU_EN	CPU Port Enable Enables the CPU port specified in CPU_PORT. 1'b0: No CPU port exists. 1'b1: Enable	0x0
6:4	RW	CPU_PORT	CPU Port Number Sets the CPU port number. 3'h0: Port 0 ... 3'h7: Port 7	0x0
3	RW	MIRROR_EN	Mirror Port Enable Enables the mirror port specified in MIRROR_PORT. 1'b0: No mirror available 1'b1: Enable mirror	0x0
2:0	RW	MIRROR_PORT	Mirror Port Number Sets the mirror port number. 3'h0: Port 0 ... 3'h7: Port 7	0x0

293. VTC: VLAN TAG Control Register (offset: 0x0014)

Bits	Type	Name	Description	Initial Value
31:18	-	-	Reserved	0x0
17	RW	MC_ARL_LKYV	Multicast Frame ARL Leaky VLAN Enable 1'b1: Use LEAKY_EN in ARL to control the multicast frames. 1'b0: Use PVC.MC_LKYV_EN in Port Control register to control the multicast frames	0x0

Bits	Type	Name	Description	Initial Value
16	RW	UC_ARL_LKYV	Unicast Frame ARL Leaky VLAN Enable 1'b1: Use LEAKY_EN in ARL to control the unicast frames 1'b0: Use PVC_UC_LKYV_EN in Port Control register to control the unicast frames	0x0
15:8	-	-	Reserved	0x0
7:0	RW	GUEST_MEM	Guest VLAN Member The assigned VLAN member for these frames which can not pass 802.1x authentication.	0xFF

294. ISC: IGMP Snooping Control Register (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:24	RO	LRN_RP	Learned Router Ports Shows the router ports for IGMP/MDL messages including the default and learned ports.	0x7F
23:21	-	-	Reserved	0x0
20	RW	DWN_GRADE_EN	IGMP v2 to v1 Auto-Downgrade Enable Enables an automatic downgrade from IGMPv2 to v1 due to a IGMPv1 report message. 1'b0: Disable 1'b1: Enable	0x0
19	RW	MLD_RP_EN	MLD Router Port Learning Enable Enables automatic router port learning automatically based on MLD queries. 1'b0: Disable 1'b1: Enable	0x0
18	RW	IGMP_RP_EN	IGMP Router Port Learning Enables automatic router port learning based on IGMP queries. 1'b0: Disable 1'b1: Enable	0x0
17:16	RW	ROBUST_VAR	Robustness Variable Defines the maximum allowable number of IGMP Query messages that may be lost consecutively. 0: Reserved 1: One time 2: Two times (default) 3: Three times	0x2

Bits	Type	Name	Description	Initial Value
15:8	RW	QRY_INTL	Query Interval Together with the Robustness Variable, the Query Interval sets the age-out time for router ports automatically learned from IGMP Query frames. Age-out time = (QRY_INTL * ROBUST_VAR) (unit: sec)	0x7D
7:0	RW	DEF_RP	Default Router Port Sets the default router port which will not be aged out when IGMP/MLD router port learning is enabled.	0x7F

295. IMC: IGMP/MLD Message Control Register (offset: 0x001C)

Bits	Type	Name	Description	Initial Value
31	RW	MLD_RPT_MIR	MLD Report/Done Message to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
30:28	RW	MLD_RPT_FW	MLD Report/Done Message TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
27	RW	MLD_MANG_FR	MLD Message as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	MLD_PAE_FR	MLD Message as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
25	RW	MLD_BPDU_FR	MLD Message as BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0
24:22	RW	MLD_EG_TAG	MLD Message Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0

Bits	Type	Name	Description	Initial Value
21	RW	MLD_LKY_VLAN	MLD Leaky VLAN Enable 1'b0: Disable 1'b1: Enable	0x0
20	RW	MLD_PRI_HIGH	MLD Force the Highest Priority 1'b0: System default 1'b1: Assigned to the highest priority queue.	0x1
19	RW	MLD_QUE_MIR	MLD Query Message to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
18:16	RW	MLD_QUE_FW	MLD Query Message TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped	0x0
15	RW	IGMP_RPT_MIR	IGMP Report/Leave Message to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
14:12	RW	IGMP_RPT_FW	IGMP Report/Leave Message TO_CPU Forwarding 3'b0xx: System default (Disable) 3'b100: System default and CPU port excluded 3'b101: System default & CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
11	RW	IGMP_MANG_FR	IGMP Message as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	IGMP_PAE_FR	IGMP Message as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
9	RW	IGMP_BPDU_FR	IGMP Message as BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0

Bits	Type	Name	Description	Initial Value
8:6	RW	IGMP_EG_TAG	IGMP Message Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010,3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
5	RW	IGMP_LKY_VLAN	IGMP Leaky VLAN Enable 1'b0: Disable 1'b1: Enable	0x0
4	RW	IGMP_PRI_HIGH	IGMP Force the Highest Priority 1'b0: System default 1'b1: Assigned to the highest priority queue	0x1
3	RW	IGMP_QUE_MIR	IGMP Query Message to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
2:0	RW	IGMP_QUE_FW	IGMP Query Message TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0

296. APC: ARP and PPPoE Control Register (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	PPP_MANG_FR	PPPoE Discovery as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	PPP_PAE_FR	PPPoE Discovery as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
25	RW	PPP_BPDU_FR	PPPoE Discovery as BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0

Bits	Type	Name	Description	Initial Value
24:22	RW	PPP_EG_TAG	PPPoE Discovery Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
21	RW	PPP_LKY_VLAN	PPPoE Discovery Leaky VLAN Enable 1'b0: Disable 1'b1: Enable	0x0
20	RW	PPP_PRI_HIGH	PPPoE Discovery Force the Highest Priority 1'b0: System default 1'b1: Assigned to the highest priority queue	0x1
19	RW	PPP_MIR	PPPoE Discovery Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
18:16	RW	PPP_PORT_FW	PPPoE Discovery TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded. 3'b101: System default and CPU port included. 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
15:12	-	-	Reserved	0x0
11	RW	ARP_MANG_FR	ARP/RARP as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	ARP_PAE_FR	ARP/RARP as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
9	RW	ARP_BPDU_FR	ARP/RARP as BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0
8:6	RW	ARP_EG_TAG	ARP/RARP Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0

Bits	Type	Name	Description	Initial Value
5	RW	ARP_LKY_VLAN	ARP/RARP Leaky VLAN Enable 1'b0: Disable 1'b1: Enable	0x0
4	RW	ARP_PRI_HIGH	ARP/RARP Force the Highest Priority 1'b0: System default 1'b1: Assigned to the highest priority queue	0x1
3	RW	ARP_MIR	ARP/RARP Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
2:0	RW	ARP_PORT_FW	ARP/RARP TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0

297. BPC: BPDU and PAE Control Register (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	PAE_MANG_FR	PAE as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	PAE_FR	PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x1
25	RW	PAE_BPDU_FR	PAE as BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0
24:22	RW	PAE_EG_TAG	PAE Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
21	RW	PAE_LKY_VLAN	PAE Leaky VLAN Enable 1'b0: Disable 1'b1: Enable	0x0
20	RW	PAE_PRI_HIGH	PAE Force the Highest Priority 1'b0: System Default 1'b1: Assigned to the highest priority queue	0x1

Bits	Type	Name	Description	Initial Value
19	RW	PAE_MIR	PAE to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
18:16	RW	PAE_PORT_FW	PAE TO_CPU Forwarding Ports 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
15:12	-	-	Reserved	0x0
11	RW	BPDU_MANG_FR	BPDU as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	BPDU_PAE_FR	BPDU as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
9	RW	BPDU_FR	BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x1
8:6	RW	BPDU_EG_TAG	BPDU Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
5	RW	BPDU_LKY_VLAN	BPDU Leaky VLAN Enable 1'b0: Disable 1'b1: Leaky VLAN enable	0x0
4	RW	BPDU_PRI_HIGH	BPDU Force the Highest Priority 1'b0: System Default 1'b1: Assigned to the highest priority queue	0x1
19	RW	BPDU_MIR	BPDU to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0

Bits	Type	Name	Description	Initial Value
2:0	RW	BPDU_PORT_FW	BPDU TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0

298. RGAC1: REV_01 and REV_02 Control Register (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	R02_MANG_FR	REV_02 as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	R02_PAE_FR	REV_02 as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
25	RW	R02_BPDU_FR	REV_02 as BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0
24:22	RW	R02_EG_TAG	REV_02 Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
21	RW	R02_LKY_VLAN	REV_02 Leaky VLAN Enable 1'b1: Leaky VLAN enable 1'b0: Disable	0x0
20	RW	R02_PRI_HIGH	REV_02 Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1
19	RW	R02_MIR	REV_02 to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0

Bits	Type	Name	Description	Initial Value
18:16	RW	R02_PORT_FW	REV_02 TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
15:12	-	-	Reserved	0x0
11	RW	R01_MANG_FR	REV_01 as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	R01_PAE_FR	REV_01 as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
9	RW	R01_BPDU_FR	REV_01 as BPDU Frame 1'b0: Disable 1'b1: Regarded as BPDU frame	0x0
8:6	RW	R01_EG_TAG	REV_01 Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
5	RW	R01_LKY_VLAN	REV_01 Leaky VLAN Enable 1'b1: Leaky VLAN enable 1'b0: Disable	0x0
4	RW	R01_PRI_HIGH	REV_01 Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1
3	RW	R01_MIR	REV_01 to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
2:0	RW	R01_PORT_FW	REV_01 TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped	0x0

NOTE: For more information on this register, see Multicast Frames.

299. RGAC2: REV_03 and REV_0E Control Register (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	ROE_MANG_FR	REV_0E as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	ROE_PAE_FR	REV_0E as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
25	RW	ROE_BPDU_FR	REV_0E as BPDU Frame 1'b0: Disable 1'b1: Regarded as BPDU frame	0x0
24:22	RW	ROE_EG_TAG	REV_0E Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
21	RW	ROE_LKY_VLAN	REV_0E Leaky VLAN Enable 1'b1: Enable 1'b0: Disable	0x0
20	RW	ROE_PRI_HIGH	REV_0E Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1
19	RW	ROE_MIR	REV_0E to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
18:16	RW	ROE_PORT_FW	REV_0E TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
15:12	-	-	Reserved	0x0
11	RW	R03_MANG_FR	REV_03 as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	R03_BPDU_FR	REV_03 as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0

Bits	Type	Name	Description	Initial Value
9	RW	R03_BPDU_FR	REV_03 as BPDU Frame 1'b0: Disable 1'b1: Regarded as BPDU frame	0x0
8:6	RW	R03_EG_TAG	REV_03 Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
5	RW	R03_LKY_VLAN	REV_03 Leaky VLAN Enable 1'b1: Enable 1'b0: Disable	0x0
4	RW	R03_PRI_HIGH	REV_03 Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1
3	RW	R03_MIR	REV_03 to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
2:0	RW	R03_PORT_FW	REV_03 TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0

NOTE: For more information on this register, see Multicast Frames.

300. RGAC3: REV_10 and REV_20 Control Register (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	R20_MANG_FR	REV_20 as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	R20_PAE_FR	REV_20 as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
25	RW	R20_BPDU_FR	REV_20 as BPDU Frame 1'b0: Disable 1'b1: Regarded as BPDU frame	0x0

Bits	Type	Name	Description	Initial Value
24:22	RW	R20_EG_TAG	REV_20 Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
21	RW	R20_LKY_VLAN	REV_20 Leaky VLAN Enable 1'b1: Enable 1'b0: Disable	0x0
20	RW	R20_PRI_HIGH	REV_20 Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1
19	RW	R20_MIR	REV_20 to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
18:16	RW	R20_PORT_FW	REV_20 TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
15:12	-	-	Reserved	0x0
11	RW	R10_MANG_FR	REV_10 as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	R10_PAE_FR	REV_10 as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
9	RW	R10_BPDU_FR	REV_10 as BPDU Frame 1'b0: Disable 1'b1: Regarded as BPDU frame	0x0
8:6	RW	R10_EG_TAG	REV_10 Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0

Bits	Type	Name	Description	Initial Value
5	RW	R10_LKY_VLAN	REV_10 Leaky VLAN Enable 1'b1: Enable 1'b0: Disable	0x0
4	RW	R10_PRI_HIGH	REV_10 Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1
3	RW	R10_MIR	REV_10 to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
2:0	RW	R10_PORT_FW	REV_10 TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0

NOTE: For more information on this register, see Multicast Frames.

301. RGAC4: REV_21 and REV_UN Register (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	RUN_MANG_FR	REV_UN as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	RUN_PAE_FR	REV_UN as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
25	RW	RUN_BPDU_FR	REV_UN as BPDU Frame 1'b0: Disable 1'b1: Regarded as BPDU frame	0x0
24:22	RW	RUN_EG_TAG	REV_UN Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
21	RW	RUN_LKY_VLAN	REV_UN Leaky VLAN Enable 1'b1: Enable 1'b0: Disable	0x0
20	RW	RUN_PRI_HIGH	REV_UN Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1

Bits	Type	Name	Description	Initial Value
19	RW	RUN_MIR	REV_UN to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
18:16	RW	RUN_PORT_FW	REV_UN TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
15:12	-	-	Reserved	0x0
11	RW	R21_MANG_FR	REV_21 as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	R21_PAE_FR	REV_21 as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0
9	RW	R21_BPDU_FR	REV_21 as BPDU Frame 1'b0: Disable 1'b1: Regarded as BPDU frame	0x0
8:6	RW	R21_EG_TAG	REV_21 Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
5	RW	R21_LKY_VLAN	REV_21 Leaky VLAN Enable 1'b1: Enable 1'b0: Disable	0x0
4	RW	R21_PRI_HIGH	REV_21 Force the Highest Priority 1'b1: Assigned to the highest priority queue 1'b0: System default	0x1
3	RW	R21_MIR	REV_21 to Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0

Bits	Type	Name	Description	Initial Value
2:0	RW	R21_PORT_FW	REV_21 TO_CPU Forwarding 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0

NOTE: For more information on this register, see Multicast Frames.

302. PMC: Protocol Match Control Register (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29	RW	TYPE3_EN	TYPE 3 Match Enable	0x0
28	RW	TYPE3_VLD	TYPE 3 Value Valid	0x0
27:24	RW	TYPE3_ENCAP	Encapsulated Frame Type Value	0x0
7:6	-	-	Reserved	0x0
21	RW	TYPE2_EN	TYPE 2 Match Enable	0x0
20	RW	TYPE2_VLD	TYPE 2 Value Valid	0x0
19:16	RW	TYPE2_ENCAP	Encapsulated Frame Type Value	0x0
15:14	-	-	Reserved	0x0
13	RW	TYPE1_EN	TYPE 1 Match Enable	0x0
12	RW	TYPE1_VLD	TYPE 1 Value Valid 1'b0: TYPE 1 Value in register PBG.TYPE1 is "don't care", i.e. it has no effect. 1'b1: TYPE 1 Value in register PBG.TYPE1 is valid.	0x0
11:8	RW	TYPE1_ENCAP	Encapsulated Frame Type Bit0: Ethernet II Bit1: RFC_1042 Bit2: IPX Raw 802.3 Bit3: 802.2/802.3 Length Encapsulated	0x0
7:0	-	-	Reserved	0x0

NOTE:

- Where applicable,
0: Disable
1: Enable
- Type 0 is the default group ID (GID) for all unmatched frames.

303. PBG1: Protocol Based Group ID-I Register (offset: 0x003C)

Bits	Type	Name	Description	Initial Value
31:16	RW	TYPE1	TYPE 1 Value Ethernet II: Matched with EtherType RFC_1042: Matched with SNAP Type IPX Raw 802.3: "Don't care" 802.2/802.3 Length Encapsulate: Matched with DSAP[15:8] and SSAP[7:0]	0x0000
15:0	-	-	Reserved	0x0000

NOTE: Type 0 is the default group ID (GID) for all unmatched frames.

304. PBG2: Protocol Based Group ID-II Register (offset: 0x0040)

Bits	Type	Name	Description	Initial Value
31:16	RW	TYPE3	TYPE 3 Value	0x0000
15:0	RW	TYPE2	TYPE 2 Value	0x0000

305. UPW: User Priority Weight Register (offset: 0x0044)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	-
23	-	-	Reserved	-
22:20	RW	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)	0x2
19	-	-	Reserved	-
18:16	RW	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.	0x3
15	-	-	Reserved	-
14:12	RW	DSCP_UPW	DSCP Priority Weight (IPv4)	0x4
11	-	-	Reserved	-
10:8	RW	TAG_UPW	Priority Tag User Priority Weight	0x5
7	-	-	Reserved	-
6:4	RW	PPE_UPW	PPE User Priority Weight	0x6
3	-	-	Reserved	-
2:0	RW	ACL_UPW	ACL User Priority Weight (ACL Hit)	0x7

306. PEM1: User Priority Egress Mapping I Register (offset: 0x0048)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	TAG_PRI_1	User Priority 1 Priority Tag Value	0x1
26:24	RW	QUE_CPU_1	User Priority 1 CPU Queue Selection	0x0
23:22	RW	QUE_LAN_1	User Priority 1 LAN Queue Selection	0x0
21:16	RW	DSCP_PRI_1	User Priority 1 DSCP Value	0x08
15:14	-	-	Reserved	0x0
13:11	RW	TAG_PRI_0	User Priority 0 Priority Tag Value	0x0

Bits	Type	Name	Description	Initial Value
10:8	RW	QUE_CPU_0	User Priority 0 CPU Queue Selection	0x2
7:6	RW	QUE_LAN_0	User Priority 0 LAN Queue Selection	0x1
5:0	RW	DSCP_PRI_0	User Priority 0 DSCP Value	0x0

307. PEM2: User Priority Egress Mapping II Register (offset: 0x004C)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	TAG_PRI_3	User Priority 3 Priority Tag Value	0x3
26:24	RW	QUE_CPU_3	User Priority 3 CPU Queue Selection	0x3
23:22	RW	QUE_LAN_3	User Priority 3 LAN Queue Selection	0x1
21:16	RW	DSCP_PRI_3	User Priority 3 DSCP Value	0x18
15:14	-	-	Reserved	0x0
13:11	RW	TAG_PRI_2	User Priority 2 Priority Tag Value	0x2
10:8	RW	QUE_CPU_2	User Priority 2 CPU Queue Selection	0x1
7:6	RW	QUE_LAN_2	User Priority 2 LAN Queue Selection	0x0
5:0	RW	DSCP_PRI_2	User Priority 2 DSCP Value	0x10

308. PEM3: User Priority Egress Mapping III Register (offset: 0x0050)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	TAG_PRI_5	User Priority 5 Tag Priority Tag Value	0x4
26:24	RW	QUE_CPU_5	User Priority 5 CPU Queue Selection	0x5
23:22	RW	QUE_LAN_5	User Priority 5 LAN Queue Selection	0x2
21:16	RW	DSCP_PRI_5	User Priority 5 DSCP Value	0x28
15:14	-	-	Reserved	0x0
13:11	RW	TAG_PRI_4	User Priority 4 Priority Tag Value	0x4
10:8	RW	QUE_CPU_4	User Priority 4 CPU Queue Selection	0x4
7:6	RW	QUE_LAN_4	User Priority 4 LAN Queue Selection	0x2
5:0	RW	DSCP_PRI_4	User Priority 4 DSCP Value	0x20

309. PEM4: User Priority Egress Mapping IV Register (offset: 0x0054)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	TAG_PRI_7	User Priority 7 Priority Tag Value	0x7
26:24	RW	QUE_CPU_7	User Priority 7 CPU Queue Selection	0x7
23:22	RW	QUE_LAN_7	User Priority 7 LAN Queue Selection	0x3
21:16	RW	DSCP_PRI_7	User Priority 7 DSCP Value	0x38
15:14	-	-	Reserved	0x0
13:11	RW	TAG_PRI_6	User Priority 6 Priority Tag Value	0x6
10:8	RW	QUE_CPU_6	User Priority 6 CPU Queue Selection	0x6

Bits	Type	Name	Description	Initial Value
7:6	RW	QUE_LAN_6	User Priority 6 LAN Queue Selection	0x3
5:0	RW	DSCP_PRI_6	User Priority 6 DSCP Value	0x30

310. PIM1: DSCP Priority Ingress Mapping I Register (offset: 0x0058)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	PRI_DSCP_09	User Priority for Differentiated Services Code Point (DSCP) 0b001_001	0x1
26:24	RW	PRI_DSCP_08	User Priority for DSCP 0b001_000	0x1
23:21	RW	PRI_DSCP_07	User Priority for DSCP 0b000_111	0x0
20:18	RW	PRI_DSCP_06	User Priority for DSCP 0b000_110	0x0
17:15	RW	PRI_DSCP_05	User Priority for DSCP 0b000_101	0x0
14:12	RW	PRI_DSCP_04	User Priority for DSCP 0b000_100	0x0
11:9	RW	PRI_DSCP_03	User Priority for DSCP 0b000_011	0x0
8:6	RW	PRI_DSCP_02	User Priority for DSCP 0b000_010	0x0
5:3	RW	PRI_DSCP_01	User Priority for DSCP 0b000_001	0x0
2:0	RW	PRI_DSCP_00	User Priority for DSCP 0b000_000	0x0

311. PIM2: DSCP Priority Ingress Mapping II Register (offset: 0x005C)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	PRI_DSCP_19	User Priority for DSCP 0b010_011	0x2
26:24	RW	PRI_DSCP_18	User Priority for DSCP 0b010_010	0x2
23:21	RW	PRI_DSCP_17	User Priority for DSCP 0b010_001	0x2
20:18	RW	PRI_DSCP_16	User Priority for DSCP 0b010_000	0x2
17:15	RW	PRI_DSCP_15	User Priority for DSCP 0b001_111	0x1
14:12	RW	PRI_DSCP_14	User Priority for DSCP 0b001_110	0x1
11:9	RW	PRI_DSCP_13	User Priority for DSCP 0b001_101	0x1
8:6	RW	PRI_DSCP_12	User Priority for DSCP 0b001_100	0x1
5:3	RW	PRI_DSCP_11	User Priority for DSCP 0b001_011	0x1
2:0	RW	PRI_DSCP_10	User Priority for DSCP 0b001_010	0x1

312. PIM3: DSCP Priority Ingress Mapping III Register (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	PRI_DSCP_29	User Priority for DSCP 0b011_101	0x3
26:24	RW	PRI_DSCP_28	User Priority for DSCP 0b011_100	0x3
23:21	RW	PRI_DSCP_27	User Priority for DSCP 0b011_011	0x3
20:18	RW	PRI_DSCP_26	User Priority for DSCP 0b011_010	0x3
17:15	RW	PRI_DSCP_25	User Priority for DSCP 0b011_001	0x3

Bits	Type	Name	Description	Initial Value
14:12	RW	PRI_DSCP_24	User Priority for DSCP 0b011_000	0x3
11:9	RW	PRI_DSCP_23	User Priority for DSCP 0b010_111	0x2
8:6	RW	PRI_DSCP_22	User Priority for DSCP 0b010_110	0x2
5:3	RW	PRI_DSCP_21	User Priority for DSCP 0b010_101	0x2
2:0	RW	PRI_DSCP_20	User Priority for DSCP 0b010_100	0x2

313. PIM4: DSCP Priority Ingress Mapping IV Register (offset: 0x0064)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	PRI_DSCP_39	User Priority for DSCP 0b100_111	0x4
26:24	RW	PRI_DSCP_38	User Priority for DSCP 0b100_110	0x4
23:21	RW	PRI_DSCP_37	User Priority for DSCP 0b100_101	0x4
20:18	RW	PRI_DSCP_36	User Priority for DSCP 0b100_100	0x4
17:15	RW	PRI_DSCP_35	User Priority for DSCP 0b100_011	0x4
14:12	RW	PRI_DSCP_34	User Priority for DSCP 0b100_010	0x4
11:9	RW	PRI_DSCP_33	User Priority for DSCP 0b100_001	0x4
8:6	RW	PRI_DSCP_32	User Priority for DSCP 0b100_000	0x4
5:3	RW	PRI_DSCP_31	User Priority for DSCP 0b011_111	0x3
2:0	RW	PRI_DSCP_30	User Priority for DSCP 0b011_101	0x3

314. PIM5: DSCP Priority Ingress Mapping V Register (offset: 0x0068)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	PRI_DSCP_49	User Priority for DSCP 0b110_001	0x6
26:24	RW	PRI_DSCP_48	User Priority for DSCP 0b110_000	0x6
23:21	RW	PRI_DSCP_47	User Priority for DSCP 0b101_111	0x5
20:18	RW	PRI_DSCP_46	User Priority for DSCP 0b101_110	0x5
17:15	RW	PRI_DSCP_45	User Priority for DSCP 0b101_101	0x5
14:12	RW	PRI_DSCP_44	User Priority for DSCP 0b101_100	0x5
11:9	RW	PRI_DSCP_43	User Priority for DSCP 0b101_011	0x5
8:6	RW	PRI_DSCP_42	User Priority for DSCP 0b101_010	0x5
5:3	RW	PRI_DSCP_41	User Priority for DSCP 0b101_001	0x5
2:0	RW	PRI_DSCP_40	User Priority for DSCP 0b101_000	0x5

315. PIM6: DSCP Priority Ingress Mapping VI Register (offset: 0x006C)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:27	RW	PRI_DSCP_59	User Priority for DSCP 0b111_011	0x7
26:24	RW	PRI_DSCP_58	User Priority for DSCP 0b111_010	0x7
23:21	RW	PRI_DSCP_57	User Priority for DSCP 0b111_001	0x7

Bits	Type	Name	Description	Initial Value
20:18	RW	PRI_DSCP_56	User Priority for DSCP 0b111_000	0x7
17:15	RW	PRI_DSCP_55	User Priority for DSCP 0b110_111	0x6
14:12	RW	PRI_DSCP_54	User Priority for DSCP 0b110_110	0x6
11:9	RW	PRI_DSCP_53	User Priority for DSCP 0b110_101	0x6
8:6	RW	PRI_DSCP_52	User Priority for DSCP 0b110_100	0x6
5:3	RW	PRI_DSCP_51	User Priority for DSCP 0b110_011	0x6
2:0	RW	PRI_DSCP_50	User Priority for DSCP 0b110_010	0x6

316. PIM7: DSCP Priority Ingress Mapping VII Register (offset: 0x0070)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:9	RW	PRI_DSCP_63	User Priority for DSCP 0b111_111	0x7
8:6	RW	PRI_DSCP_62	User Priority for DSCP 0b111_110	0x7
5:3	RW	PRI_DSCP_61	User Priority for DSCP 0b111_101	0x7
2:0	RW	PRI_DSCP_60	User Priority for DSCP 0b111_100	0x7

317. ATA1: Address Table Access I Register (offset: 0x0074)

Bits	Type	Name	Description	Initial Value
31:24	RW	BYTE_0	MAC Address [47:40] /Destination IP (DIP) Address [31:24]	0x0
23:16	RW	BYTE_1	MAC Address [39:32] /DIP Address [23:16]	0x0
15:8	RW	BYTE_2	MAC Address [31:24] /DIP Address [15:8]	0x0
7:0	RW	BYTE_3	MAC Address [23:16] /DIP Address [7:0] / Source Port [7:0]	0x0

318. ATA2: Address Table Access II Register (offset: 0x0078)

Bits	Type	Name	Description	Initial Value
31:24	RW	BYTE_0	MAC Address [15: 8] /Source IP (SIP) Address [31:24]	0x0
23:16	RW	BYTE_1	MAC Address [7: 0] / SIPAddress [23:16]	0x0
15:8	RW	BYTE_2	SIP Address [15: 8] or bit[15]: IVL bit[14:12]: Filter ID[2:0] bit[11:8]: CVID[11: 8] NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table.	0x0
7:0	RW	BYTE_3	SIP Address[7:0] or CVID[7:0]	0x0

319. ATWD: Address Table Write Data Register (offset: 0x007C)

Table 2-7 Address Table Write Data Register: MAC Address

Bits	Type	Name	Description	Initial Value
31:24	RW	TIMER	Age Timer	0x0
23	RW	MY_MAC	MAC address is reserved for MY_MAC attribute	0x0
22:20	RW	SA_PORT_FW	Source Address Hit Frame Port Forwarding	0x0
19	RW	SA_MIR_EN	Source Address Hit to Mirror Port	0x0
18:16	RW	USER_PRI	User Priority	0x0
15:13	RW	EG_TAG	Egress VLAN Tag Attribute	0x0
12	RW	LEAKY_EN	Leaky VLAN Enable	0x0
11:4	RW	PORT	Destination Port Map	0x0
3:2	RW	STATUS	Address Entry Live Status	0x0
1:0	-	-	Reserved	0x0

Table 2-8 Address Table Write Data Register: DIP Entry

Bits	Type	Name	Description	Initial Value
31:19	-	-	Reserved	0x0
18:16	RW	USER_PRI	User Priority	0x0
15:13	RW	EG_TAG	Egress VLAN Tag Attribute	0x0
12	RW	LEAKY_EN	Leaky VLAN Enable	0x0
11:4	RW	PORT	Destination Port Map	0x0
3:2	RW	STATUS	Address Entry Live Status	0x0
1:0	-	-	Reserved	0x0

Table 2-9 Address Table Write Data Register: SIP Entry

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:4	RW	PORT	Destination Port Map	0x0
3:2	RW	STATUS	Address Entry Live Status	0x0
1:0	-	-	Reserved	0x0

320. ATC: Address Table Control Register (offset: 0x0080)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RO	ADDR	Address Table Access Index The actual address table access index which is calculated from a 48-bit MAC address, a 32-bit DIP, and a SIP address. (for debugging purposes)	0x0

Bits	Type	Name	Description	Initial Value
15	W1C	BUSY	Address Table Is Busy SW can set this bit to 1 only if this bit is reset. After ATWD registers are written and this bit is set, this chip will perform the corresponding function according to AC_CMD, AC_SAT, and AC_MAT included in this register.	0x0
14	RO	SRCH_END	Linear Search End The linear search has reached the index end of the address table.	0x0
13	RO	SRCH_HIT	Linear Search Hit The linear search has find the target based on AC_MAT and return the data on TSRA1,2 and ATRD.	0x0
12	RO	ADDR_INVLD	Address Entry is not Valid The specified entry is not valid for read or removal access. The specified entry can not be modified or added for write access. (hash collision)	0x0
11:8	RW	AC_MAT	Address Table Multiple Access Target Whenever MATC register is written and bit.15 is set, this chip will perform the corresponding function on the Address table based on AC_CMD bits. 4'b0000: All MAC address entries 4'b0001: All DIP/GA address entries 4'b0010: All SIP address entries 4'b0011: All valid address entry 4'b0100: All non-static MAC address entries. 4'b0101: All non-static DIP address entries. 4'b0110: All static MAC address entries 4'b0111: All static DIP address entries 4'b1000: All relative SIP address entries based on the specific DIP from ATA2 register. 4'b1001: All relative SIP address entries based on the specific SIP from ATA2 register. 4'b1010: All MAC Address entries with the customer VID specified in ATA2.CVID[11:0] 4'b1010: All MAC address entries with the Filter ID specified in ATA2.FID[2:0] 4'b1100: All MAC Address entries with the source ports specified in ATA1.PORT[7:0] 4'b1101 to 4'b1111: Reserved	0x0
7:6	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
5:4	RW	AC_SAT	Address Table Single Access Target Whenever MATC register is written and bit.31 is set, this chip will perform the corresponding function on the Address table based on FUNC bits. 2'b00: Specified MAC address entry 2'b01: Specified DIP address entry 2'b10: Specified SIP address entry 2'b11: Specified address entry(read only)	0x0
3	-	-	Reserved	0x0
2:0	RW	AC_CMD	Address Table Access Command 3'b000: Read command (single entry) 3'b001: Write command (single entry) NOTE: Supports modify, add, and remove 3'b010: Clean command (multiple entries) 3'b011: Reserved 3'b100: Start Search command (reset to 1st entry) 3'b101: Next Search command (next entry) 3'b110 to 3'b111: Reserved	0x0

321. TSRA1: Table Search Read Address-I Register (offset: 0x0084)

Bits	Type	Name	Description	Initial Value
31:24	RO	BYTE_0	MAC Address [47:40] /DIP Address [31:24]	0x0
23:16	RO	BYTE_1	MAC Address [39:32] /DIP Address [23:16]	0x0
15:8	RO	BYTE_2	MAC Address [31:24] /DIP Address [15:8]	0x0
7:0	RO	BYTE_3	MAC Address [23:16] /DIP Address [7:0]	0x0

322. TSRA2: Table Search Read Address-II Register (offset: 0x0088)

Bits	Type	Name	Description	Initial Value
31:24	RO	BYTE_0	MAC Address [15:8] /SIP Address [31:24]	0x0
23:16	RO	BYTE_1	MAC Address [7:0] /SIP Address [23:16]	0x0
15:8	RO	BYTE_2	SIP Address [15:8] or Bit[15]: IVL Bit[14:12]: Filter ID[2:0] Bit[11:8]: CVID[11:8]	0x0
7:0	RO	BYTE_3	SIP Address [7:0]	0x0

323. ATRD: Address Table Read Data Register (offset: 0x008C)

Table 2-10 Address Table Read Data Register: MAC Entry

Bits	Type	Name	Description	Initial Value
31:24	RO	TIMER	Age Timer	0x0
23	RO	MY_MAC	MAC address is reserved for MY_MAC attribute	0x0

Bits	Type	Name	Description	Initial Value
22:20	RO	SA_PORT_FW	Source Address Hit Frame Port Forwarding	0x0
19	RO	SA_MIR_EN	Source Address Hit to Mirror Port	0x0
18:16	RO	USER_PRI	User Priority	0x0
15:13	RO	EG_TAG	Egress VLAN Tag Attribute	0x0
12	RO	LEAKY_EN	Leaky VLAN Enable	0x0
11:4	RO	PORT	Destination Port Map	0x0
3:2	RO	STATUS	Address Entry Live Status	0x0
1:0	RO	TYPE	Address Entry Type	0x0

Table 2-11 Address Table Read Data Register: DIP Entry

Bits	Type	Name	Description	Initial Value
31:19	-	-	Reserved	0x0
18:16	RO	USER_PRI	User Priority	0x0
15:13	RO	EG_TAG	Egress VLAN Tag Attribute	0x0
12	RO	LEAKY_EN	Leaky VLAN Enable	0x0
11:4	RO	PORT	Destination Port Map	0x0
3:2	RO	STATUS	Address Entry Live Status	0x0
1:0	RO	TYPE	Address Entry Type	0x0

Table 2-12 Address Table Read Data Register: SIP Entry

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:4	RO	PORT	Destination Port Map	0x0
3:2	RO	STATUS	Address Entry Live Status	0x0
1:0	RO	TYPE	Address Entry Type	0x0

324. VTCR: VLAN Table Control Register (offset: 0x0090)

Bits	Type	Name	Description	Initial Value
31	W1C	BUSY	VLAN Table Is Busy SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.	0x0
30:17	-	-	Reserved	0x0
16	RO	IDX_INVLD	Entry is not Valid This index for the access control is out of the valid index.	0x0

Bits	Type	Name	Description	Initial Value
15:12	RW	FUNC	Access Control Function Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. 4'b0000: Read the specified VID Entry from VAWD# register based on VID bits 4'b0001: Write the specified VID Entry though VAWD# register based on VID bits. 4'b0010: Make the specified VID entry invalid based on VID bits. 4'b0011: Make the specified VID entry valid based on VID bits . 4'b0100: Read the specified ACL Table entry. 4'b0101: Write the specified ACL Table entry. 4'b0110: Read the specified trTCM Meter Table. 4'b0111: Write the specified trTCM Meter Table. 4'b1000: Read the specified ACL Mask entry. 4'b1001: Write the specified ACL Mask entry. 4'b1010: Read the specified ACL Rule Control entry. 4'b1011: Write the specified ACL Rule Control entry. 4'b1100: Read the specified ACL Rate Control entry. 4'b1101: Write the specified ACL Rate Control entry. 4'b1110: Reserved 4'b1111: Reserved	0x0
11:0	RW	VID	1. VLAN ID Number: 0x0 to 0x1F (16) 2. ACL table index: 0x0 to 0x3F (64) 3. ACL mask control: 0x0 to 0x1F (32)	0x0

325. VAWD1: VLAN and ACL Write Data-I Register (offset: 0x0094)

Table 2-13 VLAN and ACL Write Data-I Register: VLAN Entry

Bits	Type	Name	Description	Initial Value
31	RW	PORT_STAG	Port-based Service TAG	0x0
30	RW	IVL_MAC	Independent VLAN Learning	0x0
29	RW	EG_CON	Egress Tag Consistent	0x0
28	RW	VTAG_EN	Per VLAN Egress Tag Control	0x0
27	RW	COPY_PRI	Copy User Priority Value from Customer Priority Tag for Stack VLAN	0x0
26:24	RW	USER_PRI	Service Tag (STAG) User Priority Value from VLAN Table	0x0
23:16	RW	PORT_MEM	VLAN Member Control	0x0

Bits	Type	Name	Description	Initial Value
15:4	RW	S_TAG1	Service Tag I	0x0
3:1	RW	FID	Filtering Database	0x0
0	RW	VALID	VLAN Entry Valid	0x0

Table 2-14 VLAN and ACL Write Data-I Register: ACL Rule Table

Bits	Type	Name	Description	Initial Value
31:16	RW	BIT_MASK	Comparison Pattern Mask 0: No mask 1: Mask	0x0
15:0	RW	CMP_PAT	Comparison Pattern	0x0

Table 2-15 VLAN and ACL Write Data-I Register: ACL Rule Mask

Bits	Type	Name	Description	Initial Value
31:0	RW	ACL_MASK	ACL Mask[31:0] 0: No mask 1: Mask	0x0

Table 2-16 VLAN and ACL Write Data-I Register: ACL Rate Control

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30:16	RW	RATE	Per Flow Ingress Rate Limit Accumulator	0x0
15	RW	RATE_EN	Per Flow Ingress Rate Enable	0x0
14	RW	RATE_BKT	Rate Bucket Selection	0x0
13:0	RW	RATE_ACCU	Per Flow Ingress Rate Limit Control	0x0

NOTE: For more information on this register, see the ACL Rule Control section.

Table 2-17 VLAN and ACL Write Data-I Register: ACL Rule Control

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29	RW	ACL_MANG	Management Frame Attribute	0x0
28	RW	INT_EN	Interrupt Enable	0x0
27	RW	ACL_CNT_EN	Enable ACL Hit Count	0x0
26:24	RW	CNT_IDX	Counter Group Index	0x0
23	RW	VLAN_PORT_EN	Swap VLAN Member	0x0
22	RW	DA_SWAP	Multicast MAC Address Swap	0x0
21	RW	SA_SWAP	Source MAC Address Swap	0x0
20	RW	PPP_RM	PPPoE Header Removal	0x0
19	RW	LKY_VLAN	Leaky VLAN	0x0
18:16	RW	EG_TAG	Egress VLAN Tag Attribute	0x0
15:8	RW	PORT	Destination Port / VLAN Member	0x0
7	RW	PORT_EN	Force Destination port	0x0

Bits	Type	Name	Description	Initial Value
6:4	RW	PRI_USER	User Priority from ACL	0x0
3	RW	MIR_EN	Frame Copy to Mirror Port	0x0
2:0	RW	PORT_FW	Frame TO_CPU Forwarding	0x0

NOTE: For more information on this register, see the ACL Rule Control section.

Table 2-18 VLAN and ACL Write Data-I Register: trTCM Meter Table

Bits	Type	Name	Description	Initial Value
31	RW	CBS	Committed Burst Size	0x0
15:0	RW	PBS	Peak Burst Rate	0x0

326. VAWD2: VLAN and ACL Write Data-II Register (offset: 0x0098)

Table 2-19 VLAN and ACL Write Data-II Register: VLAN Entry

Bits	Type	Name	Description	Initial Value
31:16	RW	S_TAG2	Service Tag II	0x0
15:14	-	-	Reserved	0x0
13:12	RW	P6_TAG	P6 Egress Tag Control	0x0
11:10	RW	P5_TAG	P5 Egress Tag Control	0x0
9:8	RW	P4_TAG	P4 Egress Tag Control	0x0
7:6	RW	P3_TAG	P3 Egress Tag Control	0x0
5:4	RW	P2_TAG	P2 Egress Tag Control	0x0
3:2	RW	P1_TAG	P1 Egress Tag Control	0x0
1:0	RW	P0_TAG	P0 Egress Tag Control	0x0

Table 2-20 VLAN and ACL Write Data-II Register: ACL Rule Table

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RW	EN	ACL Pattern Enable	0x0
18:16	RW	OFST_TP	Offset Range	0x0
15:8	RW	SP	Incoming Source Port Bit-map	0x0
7:1	RW	WORD_OFST	Word Offset	0x0
0	RW	CMP_SEL	Comparison mode selection	0x0

Table 2-21 VLAN and ACL Write Data-II Register: ACL Rule Mask

Bits	Type	Name	Description	Initial Value
31:0	RW	ACL_MASK	ACL Mask[63:32]	0x0

Table 2-22 VLAN and ACL Write Data-II Register: ACL Rate Control

Bits	Type	Name	Description	Initial Value
31:0	-	-	Reserved	0x0

Table 2-23 VLAN and ACL Write Data-II Register: ACL Rule Control

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:19	RW	ACL_CLASS_IDX	ACL Class Index The ACL flow meter allows users to color code IP packet flows based on their rate.	0x0
18	RW	RED_DROP_G	RED Engine Drop Green Sets the RED engine to drop green color packets. 0: False 1: True	0x0
17	RW	ABS_DROP_Y	Yellow Color Packet Dropped Absolutely All yellow packets are dropped.	0x0
16	RW	RED_DROP_Y	RED Engine Drop Yellow Sets the RED engine to drop yellow color packets. 0: False 1: True	0x0
15	RW	ABS_DROP_R	Red Color Packet Dropped Absolutely All red packets are dropped.	0x0
14	RW	RED_DROP_R	RED Engine Drop Red Sets the RED engine to drop red color packets. 0: False 1: True	0x0
13:11	RW	DROP_PCD_R	User Defined Drop Precedence for Green	0x0
10:8	RW	DROP_PCD_R	User Defined Drop Precedence for Yellow	0x0
7:5	RW	DROP_PCD_R	User Defined Drop Precedence for Red	0x0
4:2	RW	PRI_USER	User Defined Class Selector	0x0
1	RW	MIR_EN	Select ACL Defined Class Selector	0x0
0	RW	DROP_PCD_SEL	Select ACL Defined Drop Precedence	0x0

Table 2-24 VLAN and ACL Write Data-II Register: trTCM Meter Table

Bits	Type	Name	Description	Initial Value
31:16	RW	CIR	Committed Information Rate	0x0
15:0	RW	PIR	Peak Information Rate	0x0

327. TRTCM: Two Rate Three Color Mark Register (offset: 0x009C)

Bits	Type	Name	Description	Initial Value
31	RW	TRTCM_EN	Two Rate Three Color Marker (trTCM) Enable When this bit is enabled, the meter table will be updated based on Peak Information Rate (PIR) and Committed Information Rate (CIR). The color marker will also be enabled when ACL is hit. 0: Disable 1: Enable	0x0

Bits	Type	Name	Description	Initial Value
30:26	-	-	Reserved	0x0
25:16	RW	RED_HTH	RED High Threshold The highest threshold for Random Early Detection. Sets a high threshold number of packets in a queue. When the threshold is exceeded, packets entering the queue are dropped.	0x0
15:10	-	-	Reserved	0x0
9:0	RW	RED_LTH	RED Low Threshold The lowest threshold for Random Early Detection. Sets a low threshold number of packets in a queue, below which no packets are dropped. If the number of packets is higher than the low threshold, there is an increasing probability that packets will be dropped.	0x0

328. AAC: Address Age Control Register (offset: 0x00A0)

Bits	Type	Name	Description	Initial Value
31:21	-	-	Reserved	0x0
20	RW	AGE_DIS	Address Table Aging Disable Disable or pause MAC address aging.	0x0
19:12	RW	AGE_CNT	Address Table Age Count This age count is recorded in the age timer field of the MAC address table when a new source address is received and the table entry is ready to refresh the timer. The applied age timer is equal to (AGE_CNT+1) *(AGE_UNIT+1) seconds.	0x95
11:0	RW	AGE_UNIT	Address Table Age Unit The applied aging unit is equal to (AGE_UNIT+1) seconds.	0x1

329. DHCP: DHCPv4 and DHCPv6 Control Register (offset: 0x00A4)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	DHCP6_MANG_FR	DHCPv6 Discover as Management Frame DHCP server treats DHCPv6 Discover packets as management frames. 1'b0: Disable 1'b1: Regarded as management frame	0x1
26	RW	DHCP6_PAE_FR	DHCPv6 Discover as PAE (Port Access Entity) Frame DHCP server treats DHCPv6 Discover packets as PAE frames. 1'b0: Disable 1'b1: Regarded as PAE frame	0x0

Bits	Type	Name	Description	Initial Value
25	RW	DHCP6_BPDU_FR	DHCPv6 Discover as Bridge Protocol Data Unit (BPDU) Frame DHCP server treats DHCPv6 packets as BPDU frames. 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0
24:22	RW	DHCP6_EG_TAG	DHCPv6 Discovery Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
21	RW	DHCP6_LKY_VLAN	DHCPv6 Discovery Leaky VLAN Enable Sends unicast frames to other VLANs or only forwards unicast frames to the originating VLAN. 1'b0: Disable 1'b1: Enable	0x0
20	RW	DHCP6_PRI_HIGH	DHCPv6 Discover Packets Priority High Sets DHCPv6 discover packets to the highest priority. 1'b0: System Default 1'b1: Assigned to the highest priority queue	0x1
19	RW	DHCP6_MIR	DHCPv6 Discovery Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
18:16	RW	DHCP6_PORT_FW	DHCPv6 Discovery TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
15:12	-	-	Reserved	0x0
11	RW	DHCP4_MANG_FR	DHCPv4 as Management Frame 1'b0: Disable 1'b1: Regarded as management frame	0x1
10	RW	DHCP4_PAE_FR	DHCPv4 as PAE Frame 1'b0: Disable 1'b1: Regarded as PAE frame	0x0

Bits	Type	Name	Description	Initial Value
9	RW	DHCP4_BPDU_FR	DHCPv4 as BPDU Frame 1'b0: Non-BPDU Frame 1'b1: Regarded as BPDU frame	0x0
8:6	RW	DHCP4_EG_TAG	DHCPv4 Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
5	RW	DHCP4_LKY_VLAN	DHCPv4 CP Leaky VLAN Enable 1'b0: Disable 1'b1: Enable	0x0
4	RW	DHCP4_PRI_HIGH	DHCPv4 Force the Highest Priority 1'b0: System default 1'b1: Assigned to the highest priority queue	0x1
3	RW	DHCP4_MIR	DHCPv4 Mirror Port 1'b0: Disable 1'b1: Frame copied to Mirror port	0x0
2:0	RW	DHCP4_PORT_FW	DHCPv4 TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0

330. VTIM1: VID to Table Index Map 1 Register (offset: 0x0100)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID1	VLAN Identifier for VLAN Table Index 1	0x002
11:0	RW	VID0	VLAN Identifier for VLAN Table Index 0	0x001

331. VTIM2: VID to Table Index Map 2 Register (offset: 0x0104)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID3	VLAN Identifier for VLAN Table Index 3	0x004
11:0	RW	VID2	VLAN Identifier for VLAN Table Index 2	0x003

332. VTIM3: VID to Table Index Map 3 Register (offset: 0x0108)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
23:12	RW	VID5	VLAN Identifier for VLAN Table Index 5	0x006
11:0	RW	VID4	VLAN Identifier for VLAN Table Index 4	0x005

333. VTIM4: VID to Table Index Map 4 Register (offset: 0x010C)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID7	VLAN Identifier for VLAN Table Index 7	0x008
11:0	RW	VID6	VLAN Identifier for VLAN Table Index 6	0x007

334. VTIM5: VID to Table Index Map 5 Register (offset: 0x0110)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID9	VLAN Identifier for VLAN Table Index 9	0x00A
11:0	RW	VID8	VLAN Identifier for VLAN Table Index 8	0x009

335. VTIM6: VID to Table Index Map 6 Register (offset: 0x0114)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID11	VLAN Identifier for VLAN Table Index 11	0x00C
11:0	RW	VID10	VLAN Identifier for VLAN Table Index 10	0x00B

336. VTIM7: VID to Table Index Map 7 Register (offset: 0x0118)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID13	VLAN Identifier for VLAN Table Index 13	0x00E
11:0	RW	VID12	VLAN Identifier for VLAN Table Index 12	0x00D

337. VTIM8: VID to Table Index Map 8 Register (offset: 0x011C)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID15	VLAN Identifier for VLAN Table Index 15	0x010
11:0	RW	VID14	VLAN Identifier for VLAN Table Index 14	0x00F

338. DBGCR: Debug Control Register (offset: 0x0200)

Bits	Type	Name	Description	Initial Value
31	W1C	DBG_BUSY	Debug Mode Is Busy SW can set this bit to 1 only if this bit is reset. After DBGD1 and DBGD2 registers have been written and this bit is set, this chip will perform debug commands on the corresponding debug control and data which reside in different blocks based on DEBUG_ID.	0x0

Bits	Type	Name	Description	Initial Value
30:26	-	-	Reserved	0x0
25	RW	SIM_AGE	Age Timer Simulation Mode Enables simulation mode on the age timer. 1'b0: Disable 1'b1: Only the first 8 entries are used and fast age-out is performed on the age timer.	0x0
24	RW	PCNT_CHK	Page Count Check Enables page link count check on Tx. 1'b0: Disabled 1'b1: Write page count info on PKT_MEM	0x0
23	RW	DBG_DIR	Debug Read/Write Direction Debug read or write command. DBG_CTRL and DBG_DATA are read from or written to the corresponding latches.	0x0
22:16	RW	DBG_ID	Debug Identification Debug ID for the different functions according to the following table.	0x0
15:0	RW	DBG_CTRL	Debug Control Debug mode control will be explained according to the different Debug ID. DBG_CTRL is used to control the debug data along with the DBG_ID.	0x0

Table 2-25 Debug Control Register: Debug ID and Control

DBG_ID	Module	Bit	DBG_CTRL	Action
0x0	ARL_TBLSRCH	15	TRIG_ON	Enable Frame Trigger Enable this bit to get the table data. This bit is auto-cleared after frame capture is done. 0: Disable 1: Enable
		14	-	Reserved
		13:12	DATA_SEL	Output Data Selection 2'b00: MAC Control+Frame_Type 2'b01: VLAN Control+Frame_Type 2'b10: ACL Control+Frame_Type 2'b11: Reserved
		11	DP Filter	Filter by Destination Port
		10:6	Dest. Port	Indicates Destination Port
		5	SP Filter	Filter by Source Port
		4:0	Source Port	Source Port Indication
0x1	ARL_TBLSRCH	15	TRIG_ON	Enable Frame Trigger Enable this bit to get the table data. This bit is auto-cleared after frame capture is done. 0: Disable 1: Enable

DBG_ID	Module	Bit	DBG_CTRL	Action
		14	-	Reserved
		13:12	DATA_SEL	Output Data Selection 2'b00: TBL_ACL_HIT[63:0] 2'b01: TBL_ACL_FLAG[31:0] 2'b10 to 2'b11: Reserved
		11	DP Filter	Filter by Destination Port
		10:6	Dest. Port	Indicates Destination Port
		5	SP Filter	Filter by Source Port
		4:0	Source Port	Source Port Indication
0x2	ARL_ENQUE	15	TRIG_ON	Enable Frame Trigger to get the table data after this bit is set and cleared after the frame capture is done.
		14	-	Reserved
		13:12	DATA_SEL	Output Data Selection 2'b00: PKT2ENQ_OUT[39:0] 2'b01: TBL_PL_INFO[63:0] 2'b10: TBL_PL_INFO[127:64] 2'b11: Reserved
		11	DP Filter	Filter by Destination Port
		10:6	Dest. Port	Indicates Destination Port
		5	SP Filter	Filter by Source Port
		4:0	Source Port	Source Port Indication
0x3	ARL_PKTQUE	15	CNT_EN	Enables the specified frame count (bit[4:0]).
		14:5	-	Reserved
		4	TCM_DROP	Counts frames dropped by trTCM.
		3	BSD_DROP	Counts frames dropped by Broadcast Storm.
		2	RATE_DROP	Counts frames dropped by Rate Limit.
		1	ARL_DROP	Counts frames dropped by port map or security.

339. DBGD1: Debug Data-I Register (offset: 0x0204)

Bits	Type	Name	Description	Initial Value
31:0	RW	DBG_MSB	Debug Read/Write Data MSB	0x0

340. DBGD2: Debug Data-II Register (offset: 0x0208)

Bits	Type	Name	Description	Initial Value
31:0	RW	DBG_LSB	Debug Read/Write Data LSB	0x0

341. DBG_CNT: Debug Counter Register (offset: 0x020C)

Bits	Type	Name	Description	Initial Value
31:0	RW	DBG_CNT	Debug Trigger Counter Universal event counter used for debugging.	0x0

2.20.8 BMU Registers

2.20.8.1 List of Registers

No.	Offset	Register Name	Description	Page
342	0x1000, 0x1100, 0x1200, 0x1300, 0x1400, 0x1500, 0x1600, 0x1700	MMSCR0_Q0Pn	Max-Min Scheduler Control Register 0 of Queue 0/Port n	293
343	0x1004, 0x1104, 0x1204, 0x1304, 0x1404, 0x1504, 0x1604, 0x1704	MMSCR1_Q0Pn	Max-Min Scheduler Control Register 1 of Queue 0/Port n	293
344	0x1008, 0x1108, 0x1208, 0x1308, 0x1408, 0x1508, 0x1608, 0x1708	MMSCR0_Q1Pn	Max-Min Scheduler Control Register 0 of Queue 1/Port n	294
345	0x100C, 0x110C, 0x120C, 0x130C, 0x140C, 0x150C, 0x160C, 0x170C	MMSCR1_Q1Pn	Max-Min Scheduler Control Register 1 of Queue 1/Port n	295
346	0x1010, 0x1110, 0x1210, 0x1310, 0x1410, 0x1510, 0x1610, 0x1710	MMSCR0_Q2Pn	Max-Min Scheduler Control Register 0 of Queue 2/Port n	295
347	0x1014, 0x1114, 0x1214, 0x1314, 0x1414, 0x1514, 0x1614, 0x1714	MMSCR1_Q2Pn	Max-Min Scheduler Control Register 1 of Queue 2/Port n	296
348	0x1018, 0x1118, 0x1218, 0x1318, 0x1418, 0x1518, 0x1618, 0x1718	MMSCR0_Q3Pn	Max-Min Scheduler Control Register 0 of Queue 3/Port n	296
349	0x101C, 0x111C, 0x121C, 0x131C, 0x141C, 0x151C, 0x161C, 0x171C	MMSCR1_Q3Pn	Max-Min Scheduler Control Register 1 of Queue 3/Port n	297
350	0x1020, 0x1120, 0x1220, 0x1320, 0x1420, 0x1520, 0x1620, 0x1720	MMSCR0_Q4Pn	Max-Min Scheduler Control Register 0 of Queue 4/Port n	297
351	0x1024, 0x1124, 0x1224, 0x1324, 0x1424, 0x1524, 0x1624, 0x1724	MMSCR1_Q4Pn	Max-Min Scheduler Control Register 1 of Queue 4/Port n	298
352	0x1028, 0x1128, 0x1228, 0x1328, 0x1428, 0x1528, 0x1628, 0x1728	MMSCR0_Q5Pn	Max-Min Scheduler Control Register 0 of Queue 5/Port n	298
353	0x102C, 0x112C, 0x122C, 0x132C, 0x142C, 0x152C, 0x162C, 0x172C	MMSCR1_Q5Pn	Max-Min Scheduler Control Register 1 of Queue 5/Port n	299
354	0x1030, 0x1130, 0x1230, 0x1330, 0x1430, 0x1530, 0x1630, 0x1730	MMSCR0_Q6Pn	Max-Min Scheduler Control Register 0 of Queue 6/Port n	299
355	0x1034, 0x1134, 0x1234, 0x1334, 0x1434, 0x1534, 0x1634, 0x1734	MMSCR1_Q6Pn	Max-Min Scheduler Control Register 1 of Queue 6/Port n	300

356	0x1038, 0x1138, 0x1238, 0x1338, 0x1438, 0x1538, 0x1638, 0x1738	MMSCR0_Q7Pn	Max-Min Scheduler Control Register 0 of Queue 7/Port n	301
357	0x103C, 0x113C, 0x123C, 0x133C, 0x143C, 0x153C, 0x163C, 0x173C	MMSCR1_Q7Pn	Max-Min Scheduler Control Register 1 of Queue 7/Port n	301
358	0x1040, 0x1140, 0x1240, 0x1340, 0x1440, 0x1540, 0x1640, 0x1740	ERLCR_Pn	Egress Rate Limit Control Register of Port n	302
359	0x1080, 0x1180, 0x1280, 0x1380, 0x1480, 0x1580, 0x1680, 0x1780	IRLCR_Pn	Ingress Rate Limit Control Register of Port n	302
360	0x1084, 0x1184, 0x1284, 0x1384, 0x1484, 0x1584, 0x1684, 0x1784	FPC_RXCTRL_Pn	Free Page Count at RX_CTRL of Port n	303
361	0x1090, 0x1190, 0x1290, 0x1390, 0x1490, 0x1590, 0x1690, 0x1790	EPC_QUE01_Pn	Egress Page Count at Queue 0/1 of Port n	303
362	0x1094, 0x1194, 0x1294, 0x1394, 0x1494, 0x1594, 0x1694, 0x1794	EPC_QUE23_Pn	Egress Page Count at Queue 2/3 of Port n	303
363	0x1098, 0x1198, 0x1298, 0x1398, 0x1498, 0x1598, 0x1698, 0x1798	EPC_QUE45_Pn	Egress Page Count at Queue 4/5 of Port n	303
364	0x109C, 0x119C, 0x129C, 0x139C, 0x149C, 0x159C, 0x169C, 0x179C	EPC_QUE67_Pn	Egress Page Count at Queue 6/7 of Port n	304
365	0x1F80	GERLCR	Global Egress Rate Limit Control Register	304
366	0x1FC0	FPLC	Free Page Link Count Register	304
367	0x1FE0	GFCCR0	Global Flow_Control Control Register 0	305
368	0x1FE4	GFCCR1	Global Flow_Control Control Register 1	305
369	0x1FE8	FCBR0	Flow Control Block Reservation Control Register for group 0	306
370	0x1FEC	FCBR1	Flow Control Block Reservation Control Register for group 1	306
371	0x1FF0	GIRLCR	Global Ingress Rate Limit Control Register	306
372	0x1FF4	GFCCR2	Global Flow_Control Control Register 2	307

2.20.8.2 Register Descriptions

342. MMSCR0_Q0Pn: Max-Min Scheduler Control Register 0 of Queue 0/Port n (offset: 0x1000, 0x1100, 0x1200, 0x1300, 0x1400, 0x1500, 0x1600, 0x1700)

Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x Minimum Traffic Arbitration Scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x Minimum Rate Control Enable 1'b0: Disable queue 0 min. rate limit control. When disabled, the shaper always lets packets pass. (infinite rate) 1'b1: Enable queue 0 min. rate limit control. Final Rate Limit = $MAN \cdot 10^{(EXP)} \cdot 1 \text{ Kbps}$ where, EXP: Rate Limit Exponent (defined in bit[11:8] of this register) MAN: Rate Limit Mantissa (defined in bit[6:0] of this register)	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4 'd0: 1 Kbps 'd1: 10 Kbps 'd2: 100 Kbps 'd3: 1 Mbps 'd4: 10 Mbps	0x0
7	-	-	Reserved	0x0
6:0	RW	MIN_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 1 to 100	0x0

343. MMSCR1_Q0Pn: Max-Min Scheduler Control Register 1 of Queue 0/Port n (offset: 0x1004, 0x1104, 0x1204, 0x1304, 0x1404, 0x1504, 0x1604, 0x1704)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x Maximum Traffic Arbitration Scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Maximum WFQ Weighted value = MAX_WEIGHT_Qx_Pn + 1	0x0

Bits	Type	Name	Description	Initial Value
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Maximum Rate Control Enable 1'b0: Disable queue 0 max. rate limit control. When disabled, the shaper always lets packets pass. (infinite rate) 1'b1: Enable queue 0 max. rate limit control. Final Rate Limit = $MAN \cdot 10^{(EXP)} \cdot 1$ kbps where, EXP: Rate Limit Exponent (defined in bit[11:8] of this register) MAN: Rate Limit Mantissa (defined in bit[6:0] of this register)	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x max. shaper rate limit control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x0

344. MMSCRO_Q1Pn: Max-Min Scheduler Control Register 0 of Queue 1/Port n (offset: 0x1008, 0x1108, 0x1208, 0x1308, 0x1408, 0x1508, 0x1608, 0x1708)

Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x Min. Traffic Arbitration Scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x Min. Rate Control Enable 1'b0: Disables queue 1 minimum rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 1 minimum rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MIN_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 100	0x00

345. MMSCR1_Q1Pn: Max-Min Scheduler Control Register 1 of Queue 1/Port n (offset: 0x100C, 0x110C, 0x120C, 0x130C, 0x140C, 0x150C, 0x160C, 0x170C)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x Max. Traffic Arbitration Scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Max. WFQ Weighted value= MAX_WEIGHT_Qx_Pn + 1	0x0
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Max. Rate Control Enable 1'b0: Disable queue 1 max. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 1 max. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x00

346. MMSCR0_Q2Pn: Max-Min Scheduler Control Register 0 of Queue 2/Port n (offset: 0x1010, 0x1110, 0x1210, 0x1310, 0x1410, 0x1510, 0x1610, 0x1710)

Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x Min. Traffic Arbitration Scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x Min. Rate Control Enable 1'b0: Disable queue 2 min. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 2 min. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MIN_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 100	0x00

347. MMSCR1_Q2Pn: Max-Min Scheduler Control Register 1 of Queue 2/Port n (offset: 0x1014, 0x1114, 0x1214, 0x1314, 0x1414, 0x1514, 0x1614, 0x1714)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x Max. Traffic Arbitration Scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Max. WFQ Weighted value = MAX_WEIGHT_Qx_Pn + 1	0x0
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Max. Rate Control Enable 1'b0: Disable queue 2 max. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 2 max. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x00

348. MMSCR0_Q3Pn: Max-Min Scheduler Control Register 0 of Queue 3/Port n (offset: 0x1018, 0x1118, 0x1218, 0x1318, 0x1418, 0x1518, 0x1618, 0x1718)

Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x Min. Traffic Arbitration Scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x Min. Rate Control Enable 1'b0: Disable queue 3 min. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 3 min. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
6:0	RW	MIN_RATE_CTRL _MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 100	0x00

349. MMSCR1_Q3Pn: Max-Min Scheduler Control Register 1 of Queue 3/Port n (offset: 0x101C, 0x111C, 0x121C, 0x131C, 0x141C, 0x151C, 0x161C, 0x171C)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x Max. Traffic Arbitration Scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Max. WFQ Weighted value = MAX_WEIGHT_Qx_Pn + 1	0x0
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Max. Rate Control Enable 1'b0: Disable queue 3 max. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 3 max. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL _EXP_Qx_Pn	Exponent part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL _MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x00

350. MMSCR0_Q4Pn: Max-Min Scheduler Control Register 0 of Queue 4/Port n (offset: 0x1020, 0x1120, 0x1220, 0x1320, 0x1420, 0x1520, 0x1620, 0x1720)

Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x min. traffic arbitration scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x Min. Rate Control Enable 1'b0: Disable queue 4 min. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 4 min. rate limit control.	0x0
14:12	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MIN_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 100	0x00

351. MMSCR1_Q4Pn: Max-Min Scheduler Control Register 1 of Queue 4/Port n (offset: 0x1024, 0x1124, 0x1224, 0x1324, 0x1424, 0x1524, 0x1624, 0x1724)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x Max. Traffic Arbitration Scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Max. WFQ Weighted value = MAX_WEIGHT_Qx_Pn + 1	0x0
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Max. Rate Control Enable 1'b0: Disable queue 4 max. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 4 max. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x00

352. MMSCR0_Q5Pn: Max-Min Scheduler Control Register 0 of Queue 5/Port n (offset: 0x1028, 0x1128, 0x1228, 0x1328, 0x1428, 0x1528, 0x1628, 0x1728)

Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x Min. Traffic Arbitration Scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x Min. Rate Control Enable 1'b0: Disable queue 5 min. rate limit control. When disabled, shaper always lets the packet pass.(infinite rate) 1'b1: Enable queue 0 min. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MIN_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 100	0x00

353. MMSCR1_Q5Pn: Max-Min Scheduler Control Register 1 of Queue 5/Port n (offset: 0x102C, 0x112C, 0x122C, 0x132C, 0x142C, 0x152C, 0x162C, 0x172C)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x max. traffic arbitration scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Max. WFQ Weighted value = (MAX_WEIGHT_Qx_Pn + 1)	0x0
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Max. Rate Control Enable 1'b0: Disable queue 5 max. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 5 max. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x00

354. MMSCR0_Q6Pn: Max-Min Scheduler Control Register 0 of Queue 6/Port n (offset: 0x1030, 0x1130, 0x1230, 0x1330, 0x1430, 0x1530, 0x1630, 0x1730)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x min. traffic arbitration scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x min. rate control enable 1'b0: Disable queue 6 min. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 6 min. rate limit control	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MIN_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 100	0x00

355. MMSCR1_Q6Pn: Max-Min Scheduler Control Register 1 of Queue 6/Port n (offset: 0x1034, 0x1134, 0x1234, 0x1334, 0x1434, 0x1534, 0x1634, 0x1734)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x Max. Traffic Arbitration Scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Max. WFQ Weighted value = MAX_WEIGHT_Qx_Pn + 1	0x0
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Max. Rate Control Enable 1'b0: Disable queue 6 max. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 6 max. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x00

356. MMSCRO_Q7Pn: Max-Min Scheduler Control Register 0 of Queue 7/Port n (offset: 0x1038, 0x1138, 0x1238, 0x1338, 0x1438, 0x1538, 0x1638, 0x1738)

Bits	Type	Name	Description	Initial Value
31	RW	MIN_SP_WRR_Qx_Pn	Port n Queue x Min. Traffic Arbitration Scheme 1'b0: Round-Robin (RR) 1'b1: Strict Priority (SP)	0x0
30:16	-	-	Reserved	0x0
15	RW	MIN_RATE_EN_Qx_Pn	Port n Queue x Min. Rate Control Enable 1'b0: Disable queue 7 min. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 7 min. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MIN_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MIN_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Min. Shaper Rate Limit Control Value range: 0 to 100	0x00

357. MMSCR1_Q7Pn: Max-Min Scheduler Control Register 1 of Queue 7/Port n (offset: 0x103C, 0x113C, 0x123C, 0x133C, 0x143C, 0x153C, 0x163C, 0x173C)

Bits	Type	Name	Description	Initial Value
31	RW	MAX_SP_WFQ_Qx_Pn	Port n Queue x Max. Traffic Arbitration Scheme 1'b0: Weighted Fair Queuing (WFQ) 1'b1: Strict Priority (SP)	0x0
30:28	-	-	Reserved	0x0
27:24	RW	MAX_WEIGHT_Qx_Pn	Port n Queue x Weighted Value For Max. WFQ Weighted value is = MAX_WEIGHT_Qx_Pn + 1	0x0
23:16	-	-	Reserved	0x0
15	RW	MAX_RATE_EN_Qx_Pn	Port n Queue x Max. Rate Control Enable 1'b0: Disable queue 7 max. rate limit control. When disabled, shaper always lets the packet pass. (infinite rate) 1'b1: Enable queue 7 max. rate limit control.	0x0
14:12	-	-	Reserved	0x0
11:8	RW	MAX_RATE_CTRL_EXP_Qx_Pn	Exponent part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 4	0x0
7	-	-	Reserved	0x0
6:0	RW	MAX_RATE_CTRL_MAN_Qx_Pn	Mantissa part of Port n Queue x Max. Shaper Rate Limit Control Value range: 0 to 100	0x00

358. ERLCR_Pn: Egress Rate Limit Control Register of Port n (offset: 0x1040, 0x1140, 0x1240, 0x1340, 0x1440, 0x1540, 0x1640, 0x1740)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15	RW	EG_RATE_LIMIT_EN_Pn	Port n Egress Rate Limit Control Enable 1'b0: Disable 1'b1: Enable egress rate limit control Egress port rate limitation = $MAN * 10^{(EXP)} * 1$ kbps where, EXP: EGRESS_RATE_LIMIT_EXP (defined in bit[11:8] of this register) MAN: EGRESS_RATE_LIMIT_MAN (defined in bit[6:0] of this register)	0x0
14:12	-	-	Reserved	-
11:8	RW	EG_RATE_LIMIT_EXP_Pn	Exponent part of Port n Egress Rate Limit Control Value range: 0 to 4 'd0: 1 kbps 'd1: 10 kbps 'd2: 100 kbps 'd3: 1 Mbps 'd4: 10 Mbps	0x0
7	-	-	Reserved	-
6:0	RW	EG_RATE_LIMIT_MAN_Pn	Mantissa part of port n Egress Rate Limit Control Value range: 1 to 100 (7-bit)	0x00

359. IRLCR_Pn: Ingress Rate Limit Control Register of Port n (offset: 0x1080, 0x1180, 0x1280, 0x1380, 0x1480, 0x1580, 0x1680, 0x1780)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	-
15	RW	IGC_RATE_EN_Pn	Port n Ingress Rate Limit Control Enable The rate of tokens to be filled into token bucket used for ingress rate control. 1'b0: Disable 1'b1: Ingress rate limit control enable Ingress Rate Limit Control = $(MAN * 10^{(EXP)})$ kbps where, EXP: INGRESS_RATE_LIMIT_EXP (defined in bit[11:8] of this register) MAN: INGRESS_RATE_LIMIT_MAN (defined in bit[6:0] of this register)\	0x0
14:12	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
11:8	RW	IGC_RATE_EXP_Pn	Exponent part of Port n Ingress Rate Limit Control Value range: 0 to 4 'd0: 1 kbps 'd1: 10 kbps 'd2: 100 kbps 'd3: 1 Mbps 'd4: 10 Mbps	0x0
7	-	-	Reserved	-
6:0	RW	IGC_RATE_MAN_Pn	Mantissa part of Port n Ingress Rate Limit Control Value range: 0 to 100	0x0

360. FPC_RXCTRL_Pn: Free Page Count at RX_CTRL of Port n (offset: 0x1084, 0x1184, 0x1284, 0x1384, 0x1484, 0x1584, 0x1684, 0x1784)

Bits	Type	Name	Description	Initial Value
31:3	-	-	Reserved	0x0
2:0	RO	FPC_RXCTRL	Free Page Count at RX_CTRL Indicates the free page count at RX_CTRL module.	0x3

361. EPC_QUE01_Pn: Egress Page Count at Queue 0/1 of Port n (offset: 0x1090, 0x1190, 0x1290, 0x1390, 0x1490, 0x1590, 0x1690, 0x1790)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24:16	RO	EPC_QUE1	Egress Page Count at Queue 1 Indicates the page count at egress queue 1.	0x0
15:9	-	-	Reserved	0x0
8:0	RO	EPC_QUE0	Egress Page Count at Queue 0 Indicates the page count at egress queue 0.	0x0

362. EPC_QUE23_Pn: Egress Page Count at Queue 2/3 of Port n (offset: 0x1094, 0x1194, 0x1294, 0x1394, 0x1494, 0x1594, 0x1694, 0x1794)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24:16	RO	EPC_QUE3	Egress Page Count at Queue 3 Indicates the page count at egress queue 3.	0x0
15:9	-	-	Reserved	0x0
8:0	RO	EPC_QUE2	Egress Page Count at Queue 2 Indicates the page count at egress queue 2.	0x0

363. EPC_QUE45_Pn: Egress Page Count at Queue 4/5 of Port n (offset: 0x1098, 0x1198, 0x1298, 0x1398, 0x1498, 0x1598, 0x1698, 0x1798)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24:16	RO	EPC_QUEUE5	Egress Page Count at Queue 5 Indicates the page count at egress queue 5. NOTE: Only the CPU port is supported.	0x0
15:9	-	-	Reserved	0x0
8:0	RO	EPC_QUEUE4	Egress Page Count at Queue 4 Indicates the page count at egress queue 4. NOTE: Only the CPU port is supported.	0x0

364. EPC_QUEUE67_Pn: Egress Page Count at Queue 6/7 of Port n (offset: 0x109C, 0x119C, 0x129C, 0x139C, 0x149C, 0x159C, 0x169C, 0x179C)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24:16	RO	EPC_QUEUE7	Egress Page Count at Queue 7 Indicates the page count at egress queue 7. NOTE: Only the CPU port is supported.	0x0
15:9	-	-	Reserved	0x0
8:0	RO	EPC_QUEUE6	Egress Page Count at Queue 6 Indicates the page count at egress queue 6. NOTE: Only the CPU port is supported.	0x0

365. GERLCR: Global Egress Rate Limit Control Register (offset: 0x1F80)

Bits	Type	Name	Description	Initial Value
31:10	-	-	Reserved	0x0
9	RW	EGC_MFRM_EX	Egress Rate Excludes Management Frames Management frames will be ignored by the rate limit. (Management frame type is set by ARL registers.)	0x0
8	RW	EGC_IPG_OP	Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation. 0'b0: IPG byte is excluded 1'b1: IPG byte is included	0x0
7:0	RW	EGC_IPG_BYTE	Egress Rate IPG Byte Count Byte count should be added while calculating the rate limit. 0x04: 4 byte CRC (default) 0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble	0x0

366. FPLC: Free Page Link Count Register (offset: 0x1FC0)

Bits	Type	Name	Description	Initial Value
31:26	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
25:16	RO	MIN_FREE_PL_CNT	Minimal Free Page Link Count in LMU from last read access	0x1E8
15:10	-	-	Reserved	0x0
9:0	RO	FREE_PL_CNT	Free Page Link Count in LMU.	0x1E8

367. GFCCR0: Global Flow Control Control Register 0 (offset: 0x1FE0)

Bits	Type	Name	Description	Initial Value
31	RW	FC_EN	Flow Control Enable 1'b1: Enable	0x1
30	-	-	Reserved	0x0
29	RW	FC_OFF2ON_OPT	Flow Control Assertion Option Enables aggressive frame discard option in flow control transition from OFF to ON. 0: Disable 1: Enable	0x1
28	RW	FC_ON2OFF_OPT	Flow Control De-Assertion Option Enable aggressive frame discard option in flow control transition from ON to OFF. 0: Disable 1: Enable	0x0
27:24	-	-	Reserved	0x0
23:16	RW	FC_PORT_BLK_THD	Flow Control Block Threshold Per port memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (reserve block not included)	0x08
15:8	RW	FC_FREE_BLK_HITHD	Flow Control Free Block High Threshold High water mark of memory buffer (in units of 2 blocks) associated with flow control and packet discard mechanism. (reserve block not included)	0x78
7:0	RW	FC_FREE_BLK_LOTHD	Flow Control Free Block Low Threshold Low water mark of memory buffer (in units of 2 blocks) associated with flow control and packet discard mechanism. (reserve block not included)	0x64

368. GFCCR1: Global Flow Control Control Register 1 (offset: 0x1FE4)

Bits	Type	Name	Description	Initial Value
31:28	RW	FC_BLK_THD_Q7	Tx Queue 7 Block Threshold For Flow Control	0x4
27:24	RW	FC_BLK_THD_Q6	Tx Queue 6 Block Threshold For Flow Control	0x4
23:20	RW	FC_BLK_THD_Q5	Tx Queue 5 Block Threshold For Flow Control	0x4
19:16	RW	FC_BLK_THD_Q4	Tx Queue 4 Block Threshold For Flow Control	0x4
15:12	RW	FC_BLK_THD_Q3	Tx Queue 3 Block Threshold For Flow Control	0x4
11:8	RW	FC_BLK_THD_Q2	Tx Queue 2 Block Threshold For Flow Control	0x4

Bits	Type	Name	Description	Initial Value
7:4	RW	FC_BLK_THD_Q1	Tx Queue 1 Block Threshold For Flow Control	0x4
3:0	RW	FC_BLK_THD_Q0	Tx Queue 0 Block Threshold For Flow Control	0x4

NOTE:

Current associated port will start the flow control mechanism (or discard when flow control scheme is disabled) if the following conditions (a) && (b) && (c) are satisfied, and flow control is stopped if following conditions !(a) && !(b) && (d) are satisfied.

(a) Num(MEMORY_BLOCK_ALREADY_IN_QUEUE_0) > CSR_FC_Q0_BLK_THD.

(b) Num(MEMORY_BLOCK_ALREADY_IN_PORT) > CSR_FC_PORT_BLK_THD.

(c) Num(FREE_MEMORY_BLOCK) < SR_FC_LOW_THD.

(d) Num(FREE_MEMORY_BLOCK) > CSR_FC_HIGH_THD

369. FCBRCR0: Flow Control Block Reservation Control Register for group 0 (offset: 0x1FE8)

Bits	Type	Name	Description	Initial Value
31	RW	FC_RSV_GRP0_EN	Queue Block Reservation Group 0 Enable 1'b1: Enable	0x0
30:24	-	-	Reserved	0x0
23:16	RW	FC_RSV_GRP0_PMAP	Flow Control Reservation Group 0 Port Map When b31=1, Port map for queue block reservation group 0 NOTE: Assume 8 ports	0x00
15:12	-	-	Reserved	0x0
11:8	RW	FC_RSV_GRP0_BLK_NUM	Flow Control Reservation Group 0 Block Number When b31=1, Block size for queue block reservation group 0	0x0
7:0	RW	FC_RSV_GRP0_QMAP	Flow Control Reservation Block Group 0 Queue Map When b31=1, Queue map for queue block reservation group 0	0x00

370. FCBRCR1: Flow Control Block Reservation Control Register for group 1 (offset: 0x1FEC)

Bits	Type	Name	Description	Initial Value
31	RW	FC_RSV_GRP1_EN	Reserved. (Not implemented)	0x0
30:24	-	-	Reserved	0x0
23:16	RW	FC_RSV_GRP1_PMAP	Reserved. (Not implemented)	0x00
15:12	-	-	Reserved	0x0
11:8	RW	FC_RSV_GRP1_BLK_NUM	Reserved. (Not implemented)	0x0
7:0	RW	FC_RSV_GRP1_QMAP	Reserved. (Not implemented)	0x00

371. GIRLCR: Global Ingress Rate Limit Control Register (offset: 0x1FF0)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:10	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
9	RW	IGC_MFRM_EX	Ingress Rate Excludes Management Frames Management frames will be ignored by rate limit. 1'b0: Management frame included 1'b1: Management frame excluded NOTE: Management frame type is set by ARL registers.	0x0
8	RW	IGC_IPG_OP	Ingress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation. 0'b0: IPG byte is excluded 1'b1: IPG byte is included	0x1
7:0	RW	IGC_IPG_BYTE	Ingress Rate IPG Byte Count Byte count should be added while calculating the rate limit. 0x04: Add 4 byte CRC (byte rate calculation). 0x18: Add 4 byte CRC + 8 byte Preamble + 12 byte IPG (line rate calculation).	0x04

372. GFCCR2: Global Flow_Control Control Register 2 (offset: 0x1FF4)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x00
15:8	RW	FC_PORT_BLK_HI_THD	Flow Control Port Block High Threshold Number of port block high thresholds associated with packet discard mechanism. (unit: 2 blocks)	0x12
7:0	RW	FC_QUE_BLK_HI_THD	Flow Control Queue Block High Threshold Number of queue block high thresholds associated with packet discard mechanism. (unit: 2 blocks)	0x0c

2.20.9 PORT Registers

2.20.9.1 List of Registers

No.	Offset	Name	Description	Page
373	0x2000, 0x2100, 0x2200, 0x2300, 0x2400, 0x2500, 0x2600, 0x2700	SSC	STP State Control Register	309
374	0x2004, 0x2104, 0x2204, 0x2304, 0x2404, 0x2504, 0x2604, 0x2704	PCR	Port Control Register	309
375	0x2008, 0x2108, 0x2208, 0x2308, 0x2408, 0x2508, 0x2608, 0x2708	PIC	Port IGMP Control Register	311
376	0x200C, 0x210C, 0x220C, 0x230C, 0x240C, 0x250C, 0x260C, 0x270C	PSC	Port Security Control Register	314
377	0x2010, 0x2110, 0x2210, 0x2310, 0x2410, 0x2510, 0x2610, 0x2710	PVC	Port VLAN Control Register	315
378	0x2014, 0x2114, 0x2214, 0x2314, 0x2414, 0x2514, 0x2614, 0x2714	PPBV1	Port-and-Protocol Based VLAN-I Register	316
379	0x2018, 0x2118, 0x2218, 0x2318, 0x2418, 0x2518, 0x2618, 0x2718	PPBV2	Port-and-Protocol Based VLAN-II Register	316
380	0x201C, 0x211C, 0x221C, 0x231C, 0x241C, 0x251C, 0x261C, 0x271C	BSR	Broadcast Storm Rate Control Register	317
381	0x2020, 0x2120, 0x2220, 0x2320, 0x2420, 0x2520, 0x2620, 0x2720	STAG01	STAG Index 0/1 Register	318
382	0x2024, 0x2124, 0x2224, 0x2324, 0x2424, 0x2524, 0x2624, 0x2724	STAG23	STAG Index 2/3 Register	318
383	0x2028, 0x2128, 0x2228, 0x2328, 0x2428, 0x2528, 0x2628, 0x2728	STAG45	STAG Index 4/5 Register	318
384	0x202C, 0x212C, 0x222C, 0x232C, 0x242C, 0x252C, 0x262C, 0x272C	STAG67	STAG Index 6/7 Register	318
385	0x2030, 0x2130, 0x2230, 0x2330, 0x2430, 0x2530, 0x2630, 0x2730	TPF	TO_PPE Forwarding Register	318

2.20.9.2 Register Descriptions

373. SSC: STP State Control Register (offset: 0x2000, 0x2100, 0x2200, 0x2300, 0x2400, 0x2500, 0x2600, 0x2700)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:14	RW	FID7_PST	(Rapid) Spanning Tree Protocol Port State	0x3
13:12	RW	FID6_PST	(Rapid) Spanning Tree Protocol Port State	0x3
11:10	RW	FID5_PST	(Rapid) Spanning Tree Protocol Port State	0x3
9:8	RW	FID4_PST	(Rapid) Spanning Tree Protocol Port State	0x3
7:6	RW	FID3_PST	(Rapid) Spanning Tree Protocol Port State	0x3
5:4	RW	FID2_PST	(Rapid) Spanning Tree Protocol Port State	0x3
3:2	RW	FID1_PST	(Rapid) Spanning Tree Protocol Port State	0x3
1:0	RW	FID0_PST	(Rapid) Spanning Tree Protocol Port State	0x3

NOTE: Where applicable,
 2'b00: Disable/Discarding
 2'b01: Blocking /Listening/Discarding
 2'b10: Learning
 2'b11: Forwarding

374. PCR: Port Control Register (offset: 0x2004, 0x2104, 0x2204, 0x2304, 0x2404, 0x2504, 0x2604, 0x2704)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29:28	RW	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack	0x0
27	-	-	Reserved	0x0
26:24	RW	PORT_PRI	Port-based User Priority User priority for the ingress port. 0x0: 0 ... 0x7: 7	0x0
23:16	RW	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work without 802.1Q function or an optional forwarding port map if the ingress membership violates or VID is missed on the VLAN table within 802.1Q function. NOTE: The final and effective port member should exclude the received port.	0xFF
15:13	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
12	RW	UP2DSCP_EN	User Priority To DSCP Enable Replaces DSCP according to user priority. 0: Disable 1: Enable	0x0
11	RW	UP2TAG_EN	User Priority To Tag Enable Replace 802.Q priority by user priority 0: Disable 1: Enable	0x0
10	RW	ACL_EN	Port-based ACL Enable 1'b0: Bypass the ACL Table 1'b1: Lookup the ACL Table and take the corresponding actions.	0x0
9	RW	PORT_TX_MIR	Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. 1'b0: Disable 1'b1: Enable NOTE: Multi-port support is possible	0x0
8	RW	PORT_RX_MIR	Port Rx Mirror Enable All frames received from this port are copied to the mirror port. 1'b0: Disable 1'b1: Enable NOTE: Multi-port support is possible.	0x0
7	RW	ACL_MIR	ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 1'b0: Disable 1'b1: Enable	0x0
6:4	RW	MIS_PORT_FW	ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatch 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded. 3'b101: System default and CPU port included. 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped	0x0
3	-	-	Reserved	0x0
2	RW	VLAN_MIS	VLAN Mismatch to Mirror Port 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.	0x0

Bits	Type	Name	Description	Initial Value
1:0	RW	PORT_VLAN	Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode Forward received frames with ingress ports that do not belong to the VLAN member. Per frames whose VID is not listed on the VLAN table are forwarded based on the Port Matrix member. 2'b10: Check Mode Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames once if VID is missed on the VLAN table. 2'b11: Security Mode Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.	0x0

375. PIC: Port IGMP Control Register (offset: 0x2008, 0x2108, 0x2208, 0x2308, 0x2408, 0x2508, 0x2608, 0x2708)

Bits	Type	Name	Description	Initial Value
31:19	-	-	Reserved	0x0
19	RW	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copies IP multicast frames with an IGMP table mismatch to the mirror port. 1'b0: Disable 1'b1: Frame copied to Mirror port NOTE: This control register is valid only if PSR.IGMP_EN or MLD_EN is set on per port basis.	0x0
18:16	RW	IGMP_MIS	IP Multicast IGMP Table Mismatch TO_CPU Forwarding Selects how to forward IP multicast frames with an IGMP table mismatch. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded. 3'b101: System default and CPU port included. 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped NOTE: This control register is valid only if PSR.IGMP_EN or MLD_EN is set on per port basis.	0x0

Bits	Type	Name	Description	Initial Value
15:14	RW	ROBUST_VAR	Robustness Variable Defines the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times	0x2
13	RW	MLD_HW_LEAVE	MLD HW Leave Enable Enables HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without group-specific query. 1'b0: Disable 1'b1: Enable	0x0
12	RW	IGMP_HW_LEAVE	IGMP HW Leave Enable Enables HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without group-specific query. 1'b0: Disable 1'b1: Enable	0x0
11	-	-	Reserved	0x0
10	RW	IPM_224	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 1'b0: This frame is regarded as a normal multicast and search ADDR Table. 1'b1: This frame is regarded as an IP multicast frame and search IGMP table.	0x0
9	RW	IPM_33	IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 1'b0: This frame is regarded as normal multicast and search ADDR table. 1'b1: This frame is regarded as IP multicast frame and search IGMP table.	0x0
8	RW	IPM_01	IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 1'b0: This frame is regarded as normal multicast and search ADDR Table. 1'b1: This frame is regarded as IP multicast frame and search IGMP table.	0x0
7	RW	MLD2_JOIN_EN	MLD v2 HW Join Enable Enables HW IGMP snooping. Group Address will be learned and filled in the ADDR Table automatically for the specific Record Type – IS_EX(), TO_EX(). 1'b0: Disable 1'b1: Enable	0x0

Bits	Type	Name	Description	Initial Value
6	RW	IGMP3_JOIN_EN	IGMP v3 HW Join Enable Enables HW IGMP snooping. Group Address will be learned and filled in the ADDR Table automatically for the specific Record Type – IS_EX(), TO_EX(). 1'b0: Disable 1'b1: Enable	0x0
5	RW	MLD_JOIN_EN	MLD Snooping HW Join Enable 1'b0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1'b1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).	0x0
4	RW	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enables HW IGMP snooping. Group Address will be learned and filled in the ADDR Table automatically. 1'b0: Disable 1'b1: Enable	0x0
3	RW	MLD_SQRY_EN	MLD HW Specific Query Enable 1'b0: MLD specific query message will not refresh the IP multicast table. 1'b1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.	0x0
2	RW	IGMP_SQRY_EN	IGMP HW Specific Query Enable 1'b0: IGMP specific query message will not refresh the IP multicast table. 1'b1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.	0x0
1	RW	MLD_GQRY_EN	MLD HW General Query Enable 1'b0: MLD general query message will not refresh the IP multicast table. 1'b1: This port is capable of recognizing the MLD general query message to refresh the multicast member.	0x0
0	RW	IGMP_GQRY_EN	IGMP HW General Query Enable 1'b0: IGMP general Query message will not refresh the IP multicast table. 1'b1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.	0x0

376. PSC: Port Security Control Register (offset: 0x200C, 0x210C, 0x220C, 0x230C, 0x240C, 0x250C, 0x260C, 0x270C)

Bits	Type	Name	Description	Initial Value
31:20	RO	SA_LRN_CNT	Learned Source Address Number	0x0
19:8	RW	MAX_SA_LRN	Rx SA Allowable Learning Number Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1 to 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation	0xFFFF
7:6	-	-	Reserved	0x0
5	RW	SA_CNT_EN	SA Counter Enable Enables the learned source MAC Address counter. 0: Disable 1: Enable	0x0
4	RW	SA_DIS	SA Disable Disables source MAC address learning. 0: Enable 1: Disable	0x0
3:2	RW	SA_LOCK	SA Lock Select 2'b00: Receive without SA authorization. 2'b01: All received frame whose SA look-up is missing or not a port member in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or not a port member in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or not a port member in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM) NOTE: PAE frames should be passed and not affected by SA Lock.	0x0
1	RW	TX_PORT_LOCK	Tx Port Lock Enable 1'b0: Transmit authorized. 1'b1: Disable frame transmission. NOTE: PAE Frames should be passed and not affected by Port Lock.	0x0
0	RW	RX_PORT_LOCK	Rx Port Lock Enable NOTE: PAE frames should be passed and not affected by Port Lock. 1'b0: Receive authorized. 1'b1: Disable frame receiving.	0x0

377. PVC: Port VLAN Control Register (offset: 0x2010, 0x2110, 0x2210, 0x2310, 0x2410, 0x2510, 0x2610, 0x2710)

Bits	Type	Name	Description	Initial Value
31:16	RW	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.	0x8100
15	RW	DIS_PVID	PVID Disable Disables PVID insertion in priority-tagged frames. 1'b0: Use PVID for priority-tagged frames. 1'b1: Keep VID=0 for priority-tagged frames.	0x0
14	RW	FORCE_PVID	Forces PVID on VLAN-tagged frames 1'b0: Use VID in VLAN-tagged frame. 1'b1: Force-replaces VID with PVID .	0x0
13:11	-	-	Reserved	0x0
10:8	RW	EG_TAG	Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack	0x0
7:6	RW	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port	0x3
5	RW	PORT_SPEC_TAG	Special Tag Enable Enables a proprietary VLAN tag format to carry additional information to the remote port. 1'b0: No specific tag format for Tx/Rx 1'b1: Enable	0x0
4	RW	BC_LKYV_EN	Broadcast Leaky VLAN Enable 1'b0: Broadcast frames received by this port will be blocked by VLAN. 1'b1: Broadcast frames received by this port can pass through VLAN.	0x0

Bits	Type	Name	Description	Initial Value
3	RW	MC_LKYV_EN	Multicast Leaky VLAN Enable 1'b0: Multicast frames received by this port will be blocked by VLAN. 1'b1: Multicast frames received by this port can pass through VLAN. NOTE: Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.)	0x0
2	RW	UC_LKYV_EN	Unicast Leaky VLAN Enable 1'b0: Unicast frame received by this port will be blocked by VLAN. 1'b1: Unicast frame received by this port can pass through VLAN. NOTE: Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.)	0x0
1:0	RW	ACC_FRM	Acceptable Frame Type 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved	0x0

378. PPBV1: Port-and-Protocol Based VLAN-I Register (offset: 0x2014, 0x2114, 0x2214, 0x2314, 0x2414, 0x2514, 0x2614, 0x2714)

Bits	Type	Name	Description	Initial Value
31:29	RW	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for per port according to IEEE 802.1Q definition.	0x0
28	-	-	Reserved	0x0
27:16	RW	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for per port according to IEEE 802.1Q definition.	0x1
15:13	RW	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for per port according to IEEE 802.1Q definition.	0x0
12	-	-	Reserved	0x0
11:0	RW	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for per port according to IEEE 802.1Q definition.	0x1

379. PPBV2: Port-and-Protocol Based VLAN-II Register (offset: 0x2018, 0x2118, 0x2218, 0x2318, 0x2418, 0x2518, 0x2618, 0x2718)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:29	RW	G3_PORT_PRI	Group 3 Port Priority (optional) The Group 3 Priority for per port according to IEEE 802.1Q definition.	0x0
28	-	-	Reserved	0x0
27:16	RW	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for per port according to IEEE 802.1Q definition.	0x1
15:13	RW	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 and default priority for per port according to IEEE 802.1Q definition.	0x0
12	-	-	Reserved	0x0
11:0	RW	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 and default VID for per port according to IEEE 802.1Q definition.	0x1

380. BSR: Broadcast Storm Rate Control Register (offset: 0x201C, 0x211C, 0x221C, 0x231C, 0x241C, 0x251C, 0x261C, 0x271C)

Bits	Type	Name	Description	Initial Value
31	RW	STRM_MODE	Broadcast Storm Suppression 1'b0: Packet-based (1 second period) 1'b1: Rate-based	0x0
30	RW	STRM_BC_INC	Broadcast Storm Included 1'b0: Exclude BC frame 1'b1: Include BC frame	0x0
29	RW	STRM_MC_INC	Unknown Multicast Storm Included	0x0
28	RW	STRM_UC_INC	Unknown Unicast Storm Included	0x0
27:26	-	-	Reserved	0x0
25:24	RW	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps	0x0
23:16	RW	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed. 8'h0: (0 * STORM_UNIT) packets or bps 8'h1: (1 * STORM_UNIT) packets or bps ...	0x0
15:8	RW	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed. 8'h0: (0 * STORM_UNIT) packets or bps 8'h1: (1 * STORM_UNIT) packets or bps ...	0x0

Bits	Type	Name	Description	Initial Value
7:0	RW	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed. 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1 * STORM_UNIT) packets or bps ...	0x0

381. STAG01: STAG Index 0/1 Register (offset: 0x2020, 0x2120, 0x2220, 0x2320, 0x2420, 0x2520, 0x2620, 0x2720)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID1	VLAN Identifier for STAG Index 1	0x0
11:0	RW	VID0	VLAN Identifier for STAG Index 0	0x0

382. STAG23: STAG Index 2/3 Register (offset: 0x2024, 0x2124, 0x2224, 0x2324, 0x2424, 0x2524, 0x2624, 0x2724)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID3	VLAN Identifier for STAG Index 3	0x0
11:0	RW	VID2	VLAN Identifier for STAG Index 2	0x0

383. STAG45: STAG Index 4/5 Register (offset: 0x2028, 0x2128, 0x2228, 0x2328, 0x2428, 0x2528, 0x2628, 0x2728)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID5	VLAN Identifier for STAG Index 5	0x0
11:0	RW	VID4	VLAN Identifier for STAG Index 4	0x0

384. STAG67: STAG Index 6/7 Register (offset: 0x202C, 0x212C, 0x222C, 0x232C, 0x242C, 0x252C, 0x262C, 0x272C)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:12	RW	VID7	VLAN Identifier for STAG Index 7	0x0
11:0	RW	VID6	VLAN Identifier for STAG Index 6	0x0

385. TPF: TO_PPE Forwarding Register (offset: 0x2030, 0x2130, 0x2230, 0x2330, 0x2430, 0x2530, 0x2630, 0x2730)

Bits	Type	Name	Description	Initial Value
31:14	-	-	Reserved	0x0
13	RW	IP6_PPE_UN	IPv6 Unknown UC packet to PPE Forwarding Forwards unknown UC packets to the PPE port instead of the CPU port.	0x0

Bits	Type	Name	Description	Initial Value
12	RW	IP6_PPE_UC	IPv6 Learned UC Frame to PPE Forwarding Forwards IPv6 learned UC frames to the PPE port instead of the CPU port.	0x0
11	RW	IP6_PPE_BC	IPv6 Broadcast Frame to PPE Forwarding Forwards IPv6 broadcast frames to the PPE port instead of the CPU port.	0x0
10	RW	IP6_PPE_IPM	IPv6 IP_MULTI packet to PPE Forwarding Forwards IPv6 IP_MULTI packets to the PPE port instead of the CPU port. NOTE: This bit is only valid when PIC.IPM_*[10:8] is enabled.	0x0
9	RW	IP6_PPE_MC	IPv6 Multicast Frame to PPE Forwarding Forwards IP multicast frames to the PPE port instead of the CPU port.	0x0
8	RW	IP6_PPE_UC	IPv6 MY_MAC Frame to PPE Forwarding Forwards MY_MAC frames to the PPE port instead of the CPU port.	0x0
7:6	-	-	Reserved	0x0
5	RW	IP4_PPE_UN	IPv4 Unknown UC packet to PPE Forwarding Forwards IPv4 unknown UC packets to the PPE port instead of the CPU port.	0x0
4	RW	IP4_PPE_UC	IPv4 Learned UC Frame to PPE Forwarding Forwards IPv4 learned UC frames to the PPE port instead of the CPU port.	0x0
3	RW	IP4_PPE_BC	IPv4 Broadcast Frame to PPE Forwarding Forwards IPv4 broadcast frames to the PPE port instead of the CPU port.	0x0
2	RW	IP4_PPE_IPM	IPv4 IP_MULTI packet to PPE Forwarding NOTE: This bit is only valid when IPIC.IPM_*[10:8] is enabled. Forwards IPv4 packets to the PPE port instead of the CPU port.	0x0
1	RW	IP4_PPE_MC	IPv4 Multicast Frame to PPE Forwarding Forwards IPv4 packets to PPE port instead of the CPU port.	0x0
0	RW	IP4_PPE_UC	IPv4 MY_MAC Frame to PPE Forwarding Forwards IPv4 MY_MAC frames to the PPE port instead of the CPU port.	0x0

NOTE:

1'b0: Disable

1'b1: Enable

2.20.10 MAC Registers

2.20.10.1 List of Registers

No.	Offset	Name	Description	Page
386	0x3000, 0x3100, 0x3200, 0x3300, 0x3400, 0x3500, 0x3600, 0x3700	PMCR_Pn	Port n MAC Control Register	321
387	0x3004, 0x3104, 0x3204, 0x3304, 0x3404, 0x3504, 0x3604, 0x3704	PMEEECR_Pn	Port n MAC EEE Control Register	323
388	0x3008, 0x3108, 0x3208, 0x3308, 0x3408, 0x3508, 0x3608, 0x3708	PMSR_Pn	Port n MAC Status Register	323
389	0x3010, 0x3110, 0x3210, 0x3310, 0x3410, 0x3510, 0x3610, 0x3710	PINT_EN_Pn	Port n Interrupt Enable Register	324
390	0x3014, 0x3114, 0x3214, 0x3314, 0x3414, 0x3514, 0x3614, 0x3714	PINT_STS_Pn	Port n Interrupt Status Register	325
391	0x3FE0	GMACCR	Global MAC Control Register	326
392	0x3FE4	SMACCR0	System MAC Control Register 0	326
393	0x3FE8	SMACCR1	System MAC Control Register 1	326
394	0x3FF0	CKGCR	Clock Gating Control Register	327
395	0x3FF4	GPINT_EN	Global Port Interrupt Enable Register	327
396	0x3FF8	GPINT_STS	Global Port Interrupt Status Register	328

2.20.10.2 Register Descriptions

386. PMCR_Pn: Port n MAC Control Register (offset: 0x3000, 0x3100, 0x3200, 0x3300, 0x3400, 0x3500, 0x3600, 0x3700)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19:18	RW	IPG_CFG_Pn	Port n Inter-Frame Gap (IFG) Shrink <i>For CPU Port:</i> 2'b00: Normal 96-bit IFG 2'b01: Transmit 96-bit IFG with short IFG in random behavior. 2'b10: Shrink 64-bit IFG 2'b11: When any output queue inside the port is congested, shrink 64-bit IFG is enabled; otherwise, normal 96-bit IFG is the default. <i>For Non-CPU Ports:</i> 2'b00: Normal 96-bit IFG 2'b01: Transmit 96-bit IFG with short IFG in random behavior. 2'b1x: Disable	0x1
17:16	-	-	Reserved	0x0
15	RW	FORCE_MODE_Pn	Port n Force Mode Port n operates in force mode. It is used to control port n status for link, speed, duplex, RX_FC, TX_FC, eee100, and eee1g. 0: Force mode off. (MAC status is determined by the PHY auto-polling module). 1: Force mode on. (MAC status is determined by the FORCE_XXX_PN register).	0x0
14	RW	MAC_TX_EN_Pn	Port n Tx MAC Enable 1'b0: Disable 1'b1: Enable NOTE: This bit only impact on MAC function, there is no impact on the link status or queue manager.	0x1
13	RW	MAC_RX_EN_Pn	Port n Rx MAC Enable 1'b0: Disable 1'b1: Enable NOTE: This bit only impact on MAC function, there is no impact on the link status or queue manager.	0x1
12:10	-	-	Reserved	0x0
9	RW	BKOFF_EN_Pn	Port n Backoff Enable Sets the port n MAC to follow the back-off mechanism when a collision happens. 1'b0: Disable 1'b1: Enable	0x1

Bits	Type	Name	Description	Initial Value
8	RW	BACKPR_EN_Pn	Port n Back Pressure Enable Enables the back pressure mechanism when operating in half-duplex mode and internal resources are low. 1'b0: Disable 1'b1: Enable	0x1
7	RW	FORCE_EEE1G_Pn	Port n Force LPI Mode For 1000 Mbps When (FORCE_MODE_PN = 1), this bit is used to control port n's 1000Base-T EEE capability. 1'b0: Not capable of entering EEE Low Power Idle mode for 1000 Mbps link speed. 1'b1: Is capable of entering EEE Low Power Idle mode for 1000 Mbps link speed.	0x0
6	RW	FORCE_EEE100_Pn	Port n Force LPI Mode For 100 Mbps When (FORCE_MODE_PN = 1), this bit is used to control port n's 100Base-TX EEE capability. 1'b0: Not capable of entering EEE Low Power Idle mode for 100 Mbps link speed. 1'b1: Is capable of entering EEE Low Power Idle mode for 100 Mbps link speed.	0x0
5	RW	FORCE_RX_FC_Pn	Port n Force Rx FC When (FORCE_MODE_PN = 1), this bit is used to control port n's Rx FC capability. 1'b0: Disable 1'b1: Force port n MAC to accept a pause frame when operating in full-duplex mode.	0x1
4	RW	FORCE_TX_FC_Pn	Port n Force Tx FC When (FORCE_MODE_PN = 1), this bit is used to control the port n's Tx FC capability. 1'b0: Disable 1'b1: Force MAC of port n to transmit a pause frame when operates in full-duplex mode and internal resources are low.	0x1
3:2	RW	FORCE_SPD_Pn	Port n Force Speed When (FORCE_MODE_PN = 1), these bits are used to control the MAC speed of port n. 2'b00: 10 Mbps 2'b01: 100 Mbps 2'b10: 1000 Mbps 2'b11: Invalid	0x0
1	RW	FORCE_DPX_Pn	Port n Force duplex When (FORCE_MODE_PN = 1), this bit is used to control MAC duplex of port n. 1'b0: Half Duplex 1'b1: Full Duplex	0x0

Bits	Type	Name	Description	Initial Value
0	RW	FORCE_LNK_Pn	Port n Force MAC Link Up When (FORCE_MODE_PN = 1), this bit is used to control link status of port n. 1'b0: Link down 1'b1: Link up	0x0

387. PMEEECR_Pn: Port n MAC EEE Control Register (offset: 0x3004, 0x3104, 0x3204, 0x3304, 0x3404, 0x3504, 0x3604, 0x3704)

Bits	Type	Name	Description	Initial Value
31:24	RW	WAKEUP_TIME_1000_Pn	Port n Wake Up Time for 1000 Mbps Low Power Idle (LPI) Mode The minimum allowed time needed for PHY to become fully functional and for TXMAC to transmit a packet after wakeup. (unit: μ s)	0x11
23:16	RW	WAKEUP_TIME_100_Pn	Port n Wake Up Time for 100 Mbps LPI Mode The minimum allowed time needed to wait for PHY to become fully functional and for TXMAC to transmit packet after wakeup. (unit: μ s)	0x1e
15:4	RW	LPI_THRESH_Pn	Port n LPI Threshold When there is no packet to be transmitted and the time period specified by Pn_LPI_THRESHOLD is exceeded, the TXMAC will automatically enter LPI (Low Power Idle) mode and send an EEE LPI frame to link partners.	0x01e
3:1	-	-	Reserved	0x0
0	RW	LPI_MODE_EN_Pn	Port n Enter LPI Mode 1'b0: LPI mode is depend on the Pn_LPI_THRESHOLD. 1'b1: Set the system to enter LPI mode immediately and send an EEE LPI frame to link partners.	0x0

388. PMSR_Pn: Port n MAC Status Register (offset: 0x3008, 0x3108, 0x3208, 0x3308, 0x3408, 0x3508, 0x3608, 0x3708)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RO	EEE1G_STS_Pn	Port n LPI Mode Status For 1000 Mbps Indicates if capable of of entering EEE Low Power Idle mode for 1000 Mbps link speed. 1'b0: Not capable 1'b1: Capable	0x0

Bits	Type	Name	Description	Initial Value
6	RO	EEE100_STS_Pn	Port n LPI Status Mode For 100 Mbps Indicates if capable of entering EEE Low Power Idle mode for 100 Mbps link speed. 1'b0: Not capable 1'b1: Capable	0x0
5	RO	RX_FC_STS_Pn	Port n Rx XFC Status Port n Rx flow control status. 1'b0: Disable. 1'b1: Let MAC of port n to accept a pause frame when operates in full-duplex mode.	0x0
4	RO	TX_FC_STS_Pn	Port n Tx XFC Status Port n Tx flow control status. 1'b0: Disable. 1'b1: Let MAC of port n to transmit a pause frame when operates in full-duplex mode and internal resource is low.	0x0
3:2	RO	MAC_SPD_STS_Pn	Port n Speed [1:0] Status Current speed of port n after PHY links up. 2'b00: 10 Mbps 2'b01: 100 Mbps 2'b10: 1000 Mbps 2'b11: Invalid	0x0
1	RO	MAC_DPX_STS_Pn	Port n duplex Status Current duplex mode of port n after PHY links up. 1'b0: Half Duplex. 1'b1: Full Duplex.	0x0
0	RO	MAC_LNK_STS_Pn	Port n Link Up Status Link up status of port n. 1'b0: Link Down. 1'b1: Link up.	0x0

389. PINT_EN_Pn: Port n Interrupt Enable Register (offset: 0x3010, 0x3110, 0x3210, 0x3310, 0x3410, 0x3510, 0x3610, 0x3710)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15	RW	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Underrun Interrupt Enable	0x0
14	RW	TX_MISVLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable	0x0
13	RW	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable	0x0
12	RW	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable	0x0
11	RW	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable	0x0

Bits	Type	Name	Description	Initial Value
10	RW	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable	0x0
9	RW	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable	0x0
8	RW	TX_DEQ_TOUT_INT_EN	TX_CTRL DEQ Timeout Interrupt Enable	0x0
7:4	-	-	Reserved	0x0
3	RW	RX_AFF_FULL_INT_EN	RX_CTRL Agent FIFO Full Interrupt Enable	0x0
2	RW	RX_ARL_TOUT_INT_EN	RX_CTRL ARL Timeout Interrupt Enable	0x0
1	RW	RX_WRPB_TOUT_INT_EN	RX_CTRL WR_PB Timeout Interrupt Enable	0x0
0	RW	RX_GPAGE_TOUT_INT_EN	RX_CTRL Get Page Timeout Interrupt Enable	0x0

NOTE:

0: Disable

1: Enable

390. PINT_STS_Pn: Port n Interrupt Status Register (offset: 0x3014, 0x3114, 0x3214, 0x3314, 0x3414, 0x3514, 0x3614, 0x3714)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15	RC	TX_TFF_UNDR_INT	TXMAC TXFIFO Underrun Interrupt	0x0
14	RC	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt	0x0
13	RC	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt	0x0
12	RC	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt	0x0
11	RC	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt	0x0
10	RC	TX_GPAGE_TOUT_INT	TX_CTRL Get Page Timeout Interrupt	0x0
9	RC	TX_RDPB_TOUT_INT	TX_CTRL RD_PB Timeout Interrupt	0x0
8	RC	TX_DEQ_TOUT_INT	TX_CTRL DEQ Timeout Interrupt	0x0
7:4	-	-	Reserved	0x0
3	RC	RX_AFF_FULL_INT	RX_CTRL Agent FIFO Full Interrupt	0x0
2	RC	RX_ARL_TOUT_INT	RX_CTRL ARL Timeout Interrupt	0x0
1	RC	RX_WRPB_TOUT_INT	RX_CTRL WR_PB Timeout Interrupt	0x0
0	RC	RX_GPAGE_TOUT_INT	RX_CTRL Get Page Timeout Interrupt	0x0

NOTE:

Read

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

391. GMACCR: Global MAC Control Register (offset: 0x3FE0)

Bits	Type	Name	Description	Initial Value
31:18	-	-	Reserved	0x0
17	RW	PRMBL_LMT_EN	Preamble Limit Enable 1'b0: RXMAC can recognize the Start Frame Delimiter (SFD), without needing to receive a byte with the value of 55 in the preamble. 1'b1: RXMAC will recognize the SFD before the next new frame when it receives the 7 consecutive bytes with the value of 55 within the 8-byte Preamble. If SFD (8'hd5) shows up after the 8-byte Preamble, RXMAC will not recognize it and treat it as if there were no SFD.	0x0
16:13	-	-	Reserved	0x0
12:9	RW	MTCC_LMT	Maximum Transmit Collision Count Limitation. 4'h0: Disable the Tx collision abort function. Attempts to send the packet continue until the packet is successfully sent. Others: Maximum transmit collision count is up to 4'h15.	0xf
8:6	-	-	Reserved	0x0
5:2	RW	MAX_RX_JUMBO	Maximum length of ingress jumbo frames 4'h0, 4'h1: Reserved 4'h2: 2 KBytes 4'h3: 3 KBytes ... 4'hF: 15 KBytes	0x9
1:0	RW	MAX_RX_PKT_LEN	Maximum Receive Packet Length Sets the maximum length of ingress packets including CRC that can be received by MAC. 2'b00: 1518 bytes for untagged frames 1522 bytes for tagged frames 2'b01: 1536 bytes 2'b10: 1552 bytes 2'b11: MAX_RX_JUMBO	0x1

392. SMACCR0: System MAC Control Register 0 (offset: 0x3FE4)

Bits	Type	Name	Description	Initial Value
31:0	RW	SYS_MACADDR0	System MAC Address, SYS_MAC [31:0] The first 32-bit of system MAC address. It is unique and specified for pause frame.	0x0017_A50 1

393. SMACCR1: System MAC Control Register 1 (offset: 0x3FE8)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
15:0	RW	SYS_MAC_ADDR1	System MAC Address, SYS_MAC [47:32] The second 16-bit of system MAC address. It is unique and specified for pause frame.	0x0000

394. CKGCR: Clock Gating Control Register (offset: 0x3FF0)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	RW	LPI_TXIDLE_THD	Low Power Idle (LPI) Tx Idle Threshold When there is no packet to be transmitted and exceeds time period specified by LPI_TXIDLE_THD, the TXMAC will automatically enter LPI mode and send EEE LPI frame to link partner. Default: 30 ms (unit: 1 ms)	0x1e
7:6	-	-	Reserved.	0x0
5	RW	CKG_TXIDLE	Tx Global Clock Idle Stop 0: Keep Tx port clock ticking. 1: Stop Tx port clock ticking when the corresponding port has no traffic to send and Rx port blocks have been idle for <LPI_TXIDLE_THD> ms.	0x0
4	RW	CKG_RXLPI	Rx Global Clock Idle 0: Keep Rx port clock ticking 1: Stop Rx port clock ticking when the corresponding port enters LPI mode and Rx port blocks are idle.	0x0
3:2	-	-	Reserved.	0x0
1	RW	CKG_LNKDN_PORT	Global Clock Link-Down Port Stop Port clock: clocks for GMAC, PORT_CTRL, and SCH blocks 0: Keep Rx and Tx port clock ticking 1: Stop both Rx and Tx port clock ticking when the corresponding port enters link-down status for 7 seconds.	0x1
0	RW	CKG_LNKDN_GLB	Global Clock Link-Down Stop Global clock: Clock for BMU, PB_CTRL, and ARL blocks 0: Keep the global clock ticking. 1: Stop the global clock ticking when all ports enter link-down status for 7 seconds.	0x1

395. GPINT_EN: Global Port Interrupt Enable Register (offset: 0x3FF4)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RW	PC7_INT_EN	Port Controller 7 Interrupt Enable	0x0

Bits	Type	Name	Description	Initial Value
6	RW	PC6_INT_EN	Port Controller 6 Interrupt Enable	0x0
5	RW	PC5_INT_EN	Port Controller 5 Interrupt Enable	0x0
4	RW	PC4_INT_EN	Port Controller 4 Interrupt Enable	0x0
3	RW	PC3_INT_EN	Port Controller 3 Interrupt Enable	0x0
2	RW	PC2_INT_EN	Port Controller 2 Interrupt Enable	0x0
1	RW	PC1_INT_EN	Port Controller 1 Interrupt Enable	0x0
0	RW	PC0_INT_EN	Port Controller 0 Interrupt Enable	0x0

NOTE:

0: Disable

1: Enable

396. GPINT_STS: Global Port Interrupt Status Register (offset: 0x3FF8)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RC	PC5_INT	Port Controller 7 Interrupt	0x0
6	RC	PC5_INT	Port Controller 6 Interrupt	0x0
5	RC	PC5_INT	Port Controller 5 Interrupt	0x0
4	RC	PC4_INT	Port Controller 4 Interrupt	0x0
3	RC	PC3_INT	Port Controller 3 Interrupt	0x0
2	RC	PC2_INT	Port Controller 2 Interrupt	0x0
1	RC	PC1_INT	Port Controller 1 Interrupt	0x0
0	RC	PC0_INT	Port Controller 0 Interrupt	0x0

NOTE:

Per port interrupt is raised whenever any bit status is set in PINT_STS_Pn and its corresponding enable signal PINT_EN_Pn. User should read-clear the PINT_STS_Pn first and then read-clear GPINT_STS.

2.20.11 MIB Registers

2.20.11.1 List of Registers

No.	Offset	Name	Description	Page
397	0x4000, 0x4100, 0x4200, 0x4300, 0x4400, 0x4500, 0x4600, 0x4700	ESRn	Event Status Register of Port n	330
398	0x4004, 0x4104, 0x4204, 0x4304, 0x4404, 0x4504, 0x4604, 0x4704	IntSn	Interrupt Status Register of Port n	332
399	0x4008, 0x4108, 0x4208, 0x4308, 0x4408, 0x4508, 0x4608, 0x4708	IntMn	Interrupt Mask Register of Port n	333
400	0x4010, 0x4110, 0x4210, 0x4310, 0x4410, 0x4510, 0x4610, 0x4710	TGPCn	Tx Packet Counter of Port n	334
401	0x4014, 0x4114, 0x4214, 0x4314, 0x4414, 0x4514, 0x4614, 0x4714	TBOCn	Tx Bad Octet Counter of Port n	334
402	0x4018, 0x4118, 0x4218, 0x4318, 0x4418, 0x4518, 0x4618, 0x4718	TGOCn	Tx Good Octet Counter of Port n	334
403	0x401C, 0x411C, 0x421C, 0x431C, 0x441C, 0x451C, 0x461C, 0x471C	TEPCn	Tx Event Packet Counter of Port n	334
404	0x4020, 0x4120, 0x4220, 0x4320, 0x4420, 0x4520, 0x4620, 0x4720	RGPCn	Rx Packet Counter of Port n	334
405	0x4024, 0x4124, 0x4224, 0x4324, 0x4424, 0x4524, 0x4624, 0x4724	RBOCn	Rx Bad Octet Counter of Port n	335
406	0x4028, 0x4128, 0x4228, 0x4328, 0x4428, 0x4528, 0x4628, 0x4728	RGOCn	Rx Good Octet Counter of Port n	335
407	0x402C, 0x412C, 0x422C, 0x432C, 0x442C, 0x452C, 0x462C, 0x472C	REPC1n	Rx Event Packet Counter of Port n	335
408	0x4030, 0x4130, 0x4230, 0x4330, 0x4430, 0x4530, 0x4630, 0x4730	REPC2n	Rx Event Packet Counter of Port n	335
409	0x4800	MIBCNTEN	MIB Counter Enable	335
410	0x4804	AECNT1	ACL Event-I Counter	336
411	0x4808	AECNT2	ACL Event-II Counter	336
412	0x480C	AEISR	ACL Event Interrupt Status Register	336

2.20.11.2 Register Descriptions

397. ESRn: Event Status Register of Port n (offset: 0x4000, 0x4100, 0x4200, 0x4300, 0x4400, 0x4500, 0x4600, 0x4700)

Bits	Type	Name	Description	Initial Value
31:26	-	-	Reserved	0x0
25	RC	TX_PAUSE_EVENT	Tx Pause Event Indicates a pause frame transmitted without any error.	0x0
24	RC	TX_XCOL_EVENT	T x Excessive Collisions Event Indicates a frame experienced over the number of MTCC_LIMIT (default 16) consecutive collisions or more, not including late collisions.	0x0
23	RC	TX_LCOL_EVENT	Tx Late Collision Event Indicates a transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet.	0x0
22	RC	TX_DEFER_EVENT	Tx Deferred Event Indicates a frame deferred at the first transmission attempt due to a busy line in half duplex mode. Frame involved in collision is not counted.	0x0
21	RC	TX_MCOL_EVENT	Tx Multiple Collisions Event Indicates a frame successful transmitted with multiple collision.	0x0
20	RC	TX_SCOL_EVENT	Tx Single Collision Event Indicates a frame successful transmitted with only single collision.	0x0
19	RC	TX_COL_EVENT	Tx Collision Event Indicates a collision occurrence during frame transmission.	0x0
18	RC	TX_BCAST_EVENT	Tx Broadcast Frame Event Indicates a broadcast frame transmitted without any error.	0x0
17	RC	TX_MCAST_EVENT	Tx Multicast Frame Event Indicates a multicast frames transmitted without any error.	0x0
16	RC	TX_DROP_EVENT	Tx Frame Dropped Event Indicates a frame dropped for the resource shortage.	0x0
15:12	-	-	Reserved	0x0
11	RC	RX_PAUSE_CNT	Rx FC Frame Count Counts correctly received paused frames.	0x0

Bits	Type	Name	Description	Initial Value
10	RC	RX_JABB_ERR_CNT	Rx Jumbo Frame Error Count Counts frame received that were longer than MAX_RX_PKT_LEN (default 1518) octets (excluding framing bits, but including FCS octets), and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).	0x0
9	RC	RX_OVERSIZE_CNT	Rx Oversized Frame Count Counts the number of frames with length larger than the maximum frame size, received without any error.	0x0
8	RC	RX_FRAG_ERR_CNT	Rx Fragmented Frame Error Count Counts the frame received that were less than 64 octets in length (excluding framing bits but including FCS octets) and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).	0x0
7	RC	RX_UNDERSIZE_CNT	Rx Undersized Frame Count Counts the frame received that were less than 64 octets long (excluding framing bits, but including FCS octets) and were otherwise well formed.	0x0
6	RC	RX_FCS_ERR_CNT	Rx Frame Error Count Counts the frame with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER.	0x0
5	RC	RX_ALIGN_ERR_CNT	Rx Frame Error Count Counts the frame with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER.	0x0
4	RC	RX_BCAST_CNT	Rx Broadcast Frame Count Counts the broadcast frame with length between 64 bytes and the maximum frame size, received without any error. Includes MAC control frames.	0x0
3	RC	RX_MCAST_CNT	Rx Multicast Frame Count Counts the multicast frame with length between 64 bytes and the maximum frame size, received without any error. Includes MAC control frames.	0x0

Bits	Type	Name	Description	Initial Value
2	RC	RX_UCAST_CNT	Rx Unicast Frame Counts the unicast frame with length between 64 bytes and the maximum frame size, received without any error. Includes MAC control frames.	0x0
1	RC	RX_FILTER_CNT	Rx Filtered Frame Count Counts the frame dropped due to security, length error, control frame or no destination port by ARL.	0x0
0	RC	RX_DROP_CNT	Rx Dropped Frame Count Counts the frames dropped due to – 1. an internal buffer shortage by RX_CTR 2. ingress rate limit by Ingress rate limiter 3. broadcast storm Control, trTCM or ACL Rate Limit by ARL.	0x0

NOTE: Where applicable,
0: False
1: True

398. IntSn: Interrupt Status Register of Port n (offset: 0x4004, 0x4104, 0x4204, 0x4304, 0x4404, 0x4504, 0x4604, 0x4704)

Bits	Type	Name	Description	Initial Value
31:21	-	-	Reserved	0x0
20	W1C	INT_TX_BAD_CNT	Tx Bad Frames Count Interrupt Asserts when TX_BAD_CNT reaches the total threshold level.	0x0
19	W1C	INT_TX_GOOD_CNT	Tx Good Frames Count Interrupt Asserts when TX_GOOD_CNT reaches the total threshold level.	0x0
18	W1C	INT_TX_BOCT_CNT	Tx Bad Octets Collision Count Interrupt Asserts when TX_BOCT_CNT reaches the total threshold level.	0x0
17	W1C	INT_TX_GOCT_CNT	Tx Good Octets Collision Count Interrupt Asserts when TX_GOCT_CNT reaches the total threshold level.	0x0
16	W1C	INT_TX_DROP_CNT	Tx Dropped Frames Count Interrupt TX_DROP_CNT reaches the total threshold level.	0x0
15:8	-	-	Reserved	0x0
7	W1C	INT_RX_BAD_CNT	Rx Bad Frames Count Interrupt Asserts when RX_BAD_CNT reaches the total threshold level.	0x0
6	W1C	INT_RX_GOOD_CNT	Rx Good Frames Count Interrupt Asserts when RX_GOOD_CNT reaches the total threshold level.	0x0

Bits	Type	Name	Description	Initial Value
5	W1C	INT_RX_BOCT_CNT	Rx Bad Octets Collision Count Interrupt Asserts when RX_BOCT_CNT reaches the total threshold level.	0x0
4	W1C	INT_RX_GOCT_CNT	Rx Good Octets Collision Count Interrupt Asserts when RX_GOCT_CNT reaches the total threshold level.	0x0
3	W1C	INT_RX_CTRL_DROP_CNT	Rx Control Drops Frame Count Interrupt Asserts when RX_CTRL_DROP_CNT reaches the total threshold level.	0x0
2	W1C	INT_RX_ING_DROP_CNT	Rx Ingress Limit Drop Frame Count Interrupt Asserts when RX_ING_DROP_CNT reaches the total threshold level.	0x0
1	W1C	INT_RX_ARL_DROP_CNT	ARL Drops Frame Count Interrupt Asserts when RX_ARL_DROP_CNT reaches the total threshold level.	0x0
0	W1C	INT_RX_FILTER_CNT	Rx Filtered Frames Count Interrupt Asserts when RX_FILTER_CNT reaches the total threshold level.	0x0

NOTE:

Read

Write

0: Interrupt not asserted.

1: Clear the interrupt

1: Interrupt asserted

399. IntMn: Interrupt Mask Register of Port n (offset: 0x4008, 0x4108, 0x4208, 0x4308, 0x4408, 0x4508, 0x4608, 0x4708)

Bits	Type	Name	Description	Initial Value
31:21	-	-	Reserved	0x7FFF
20	RW	MSK_TX_BAD_CNT	Tx Bad Frames Count Interrupt	0x1
19	RW	MSK_TX_GOOD_CNT	Tx Good Frames Count Interrupt	0x1
18	RW	MSK_TX_BOCT_CNT	Tx Bad Octets Collision Count Interrupt	0x1
17	RW	MSK_TX_GOCT_CNT	Tx Good Octets Collision Count Interrupt	0x1
16	RW	MSK_TX_DROP_CNT	Tx Dropped Frames Count Interrupt	0x1
15:8	-	-	Reserved	0xFF
7	RW	MSK_RX_BAD_CNT	Rx Bad Frames Count Interrupt	0x1
6	RW	MSK_RX_GOOD_CNT	Rx Good Frames Count Interrupt	0x1
5	RW	MSK_RX_BOCT_CNT	Rx Bad Octets Collision Count Interrupt	0x1
4	RW	MSK_RX_GOCT_CNT	Rx Good Octets Collision Count Interrupt	0x1
3	RW	MSK_RX_CTRL_DROP_CNT	Rx Control Drops Frame Count Interrupt	0x1
2	RW	MSK_RX_ING_DROP_CNT	Rx Ingress Limit Drop Frame Count Interrupt	0x1
1	RW	MSK_RX_ARL_DROP_CNT	ARL Drops Frame Count Interrupt	0x1
0	RW	MSK_RX_FILTER_CNT	Rx Filtered Frames Count Interrupt	0x1

400. TGPCn: Tx Packet Counter of Port n (offset: 0x4010, 0x4110, 0x4210, 0x4310, 0x4410, 0x4510, 0x4610, 0x4710)

Bits	Type	Name	Description	Initial Value
31:16	RO	TX_BAD_CNT	Tx Bad Frames Count Counts the number of frames transmitted with collision.	0x0000
15:0	RO	TX_GOOD_CNT	Tx Good Frames Count Counts the number of frames transmitted without any error (excluding Pause frames but including MAC control and Successful retransmission frames).	0x0000

401. TBOCn: Tx Bad Octet Counter of Port n (offset: 0x4014, 0x4114, 0x4214, 0x4314, 0x4414, 0x4514, 0x4614, 0x4714)

Bits	Type	Name	Description	Initial Value
31:0	RO	TX_BOCT_CNT	Tx Bad Frame Collision Octets Count Counts the number of bad bytes of data transmitted with collisions.	0x0000_0000

402. TGOcN: Tx Good Octet Counter of Port n (offset: 0x4018, 0x4118, 0x4218, 0x4318, 0x4418, 0x4518, 0x4618, 0x4718)

Bits	Type	Name	Description	Initial Value
31:0	RO	TX_GOCT_CNT	Tx Good Frame Collision Octets Count Counts the number of good bytes of data transmitted without any error (excluding preamble bits but including FCS octets).	0x0000_0000

403. TEPcN: Tx Event Packet Counter of Port n (offset: 0x401C, 0x411C, 0x421C, 0x431C, 0x441C, 0x451C, 0x461C, 0x471C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:0	RO	TX_DROP_CNT	Tx Dropped Frames Count Counts the number of frames dropped when FIFO is underrun.	0x0000

404. RGPCn: Rx Packet Counter of Port n (offset: 0x4020, 0x4120, 0x4220, 0x4320, 0x4420, 0x4520, 0x4620, 0x4720)

Bits	Type	Name	Description	Initial Value
31:16	RO	RX_BAD_CNT	Rx Bad Frames Error Count Counts the number of frames received with errors.	0x0000
15:0	RO	RX_GOOD_CNT	Rx Good Frames Count Counts the number of frames received without any error.	0x0000

405. RBOCn: Rx Bad Octet Counter of Port n (offset: 0x4024, 0x4124, 0x4224, 0x4324, 0x4424, 0x4524, 0x4624, 0x4724)

Bits	Type	Name	Description	Initial Value
31:0	RO	RX_BOCT_CNT	Rx Bad Octets Error Count Counts the number of good bytes of data received with error.	0x0000 _0000

406. RGOCn: Rx Good Octet Counter of Port n (offset: 0x4028, 0x4128, 0x4228, 0x4328, 0x4428, 0x4528, 0x4628, 0x4728)

Bits	Type	Name	Description	Initial Value
31:0	RO	RX_GOCT_CNT	Rx Good Octets Count Counts the number of good bytes of data received without any error (excluding preamble bits but including FCS octets).	0x0000 _0000

407. REPC1n: Rx Event Packet Counter of Port n (offset: 0x402C, 0x412C, 0x422C, 0x432C, 0x442C, 0x452C, 0x462C, 0x472C)

Bits	Type	Name	Description	Initial Value
31:16	RO	RX_CTRL_DROP_CNT	Rx Control Drops Frame Count Counts the number of frames dropped due to an error interrupt issued by RX_CTRL.	0x0000
15:0	RO	RX_ING_DROP_CNT	Rx Ingress Limit Drop Frame Count Counts the number of frames dropped due to an ingress rate limit set by the Ingress rate limiter.	0x0000

408. REPC2n: Rx Event Packet Counter of Port n (offset: 0x4030, 0x4130, 0x4230, 0x4330, 0x4430, 0x4530, 0x4630, 0x4730)

Bits	Type	Name	Description	Initial Value
31:16	RO	RX_ARL_DROP_CNT	Rx ARL Drops Frame Count Counts the number of frames dropped by the ingress rate limit (including broadcast storm, trTCm, and ACL rate limit).	0x0000
15:0	RO	RX_FILTER_CNT	Rx Filtered Frames Count Counts the number of frame dropped by ARL security, length error, control frame or port map is equal to zero.	0x0000

409. MIBCNTEN: MIB Counter Enable (offset: 0x4800)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30:24	RW	MIB_CNT_EN	MIB Counter Enable Enables the MIB counter for each port. 0: Disable 1: Enable	0x7F
23	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
22:16	RW	MIB_INT_MASK	MIB Interrupt Mask for each port 0: Unmask 1: Mask	0x00
15:12	-	-	Reserved	0x0
11:8	RW	ARL_CNT_EN	ARL Event Counter Enable 0: Disable 1: Enable	0xF
7:4	-	-	Reserved	0x0
3:0	RW	ARL_CNT_MASK	ARL Event Counter Interrupt Mask 0: Unmask 1: Mask	0x0

410. AECNT1: ACL Event-I Counter (offset: 0x4804)

Bits	Type	Name	Description	Initial Value
31:16	RO	AE1CNT	ACL Event 1 Counter Counts the number of ACL event 1 that occurred.	0x0000
15:0	RO	AE0CNT	ACL Event 0 Counter Counts the number of ACL event 0 that occurred.	0x0000

411. AECNT2: ACL Event-II Counter (offset: 0x4808)

Bits	Type	Name	Description	Initial Value
31:16	RO	AE3CNT	ACL Event 3 Counter Counts the number of ACL event 3 that occurred.	0x0000
15:0	RO	AE2CNT	ACL Event 2 Counter Counts the number of ACL event 2 that occurred.	0x0000

412. AEISR: ACL Event Interrupt Status Register (offset: 0x480C)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	0x00000000
3	W1C	INT_AE3CNT	ACL Event 3 Counter Interrupt Asserts when AE3CNT reaches the total threshold level.	0x0
2	W1C	INT_AE2CNT	ACL Event 2 Counter Interrupt Asserts when AE2CNT reaches the total threshold level.	0x0
1	W1C	INT_AE1CNT	ACL Event 1 Counter Interrupt Asserts when AE1CNT reaches the total threshold level.	0x0

Bits	Type	Name	Description	Initial Value
0	W1C	INT_AE0CNT	ACL Event 0 Counter Interrupt Asserts when AE0CNT reaches the total threshold level.	0x0

NOTE:

Read

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

NOTE:

1. Late collision has precedence over excessive collision.

2. In the event that a frame is dropped because of late or excessive collision, the last collision fragment determines which counter will be updated.

3. Counts the number of bytes in the data + pad field

4. Bytes denoted as “good” are bytes in frames transmitted successfully. Bytes denoted as “bad” are bytes in collision fragments or frames with a deliberately destroyed CRC.

2.20.12 GSW Configuration Registers

2.20.12.1 List of Registers

No.	Offset	Register Name	Description	Page
413	0x7000	PPSC	PHY Polling and SMI Master Control	339
414	0x7004	PIAC	PHY Indirect Access Control	340
415	0x7008	IMR	Interrupt Mask Register	340
416	0x700C	ISR	Interrupt Status Register	340
417	0x7010	CPC	CPU Port Control	342
418	0x7014	GPC1	GIGA Port-I Control	343
419	0x7018	DBGP	Debug Probe Control	344
420	0x701C	GPC2	GIGA Port-II Control	345

2.20.12.2 Register Descriptions

413. PPSC: PHY Polling & SMI Master Control (offset: 0x7000)

Bits	Type	Name	Description	Initial Value
31	RW	PHY_AP_EN	PHY Auto Polling Enable Enables PHY status updates to the PHY status registers by the PHY auto-polling process. 0: Disable 1: Enable	0x0
30	RW	PHY_PRE_EN	PHY Preamble Enable Sets the SMI master to send preamble bits (32 bits) at each MDIO read/write transaction. 0: Disable. 1: Enable. NOTE: This bit will affect both PHY auto-polling mode and PHY indirect access mode.	0x1
29:24	RW	PHY_MDC_CFG	PHY MDC Clock Configuration Used to configure the divider N for MDC clock frequency. MDC clock is sourced from the 12.5 MHz system clock and divided by N. NOTE: MDC clock is gated or disabled when PHY_MDC_CFG is set to 0.	0x5
23	RW	EMB_AN_Env c	Embedded PHY Auto-Polling Enable Enables auto-polling on the embedded PHY. 1'b0: Only automatically check external EPHY (port 4 & 5). NOTE: PHY_ST_ADDR = P4 PHY address PHY_END_ADDR == P5 PHY address 1'b1: Full scan ports 0 to 5 NOTE: PHY_ST_ADDR== P0 PHY address PHY_END_ADDR== P5 PHY address	0x0
22	-	-	Reserved	0x0
21:16	RW	EEE_AN_EN	PHY EEE Auto-Polling Enable	0x0
15:13	-	-	Reserved	0x0
12:8	RW	PHY_END_ADDR	PHY Polling End Address Indicates the end PHY address of PHY auto-polling process.	0x5
7:5	-	-	Reserved	0x0
4:0	RW	PHY_ST_ADDR	PHY Polling Start Address Indicates the start PHY address of PHY auto-polling process.	0x4

414. PIAC: PHY Indirect Access Control (offset: 0x7004)

Bits	Type	Name	Description	Initial Value
31	W1C	PHY_ACS_ST	PHY Access Start Starts indirect access to the PHY register. When PHY register access is complete, this bit is self-cleared to 0. 0: Idle or indirect access complete 1: Start	0x0
30	-	-	Reserved	0x0
29:25	RW	MDIO_REG_ADDR	MDIO Register Address Configures the register address field.	0x0
24:20	RW	MDIO_PHY_ADDR	MDIO PHY Address Configures the PHY address field.	0x0
19:18	RW	MDIO_CMD	MDIO Command Field Sets MDIO commands to read or write. 2'b01: MDIO Write 2'b10: MDIO Read Others: Reserved	0x2
17:16	RW	MDIO_ST	MDIO Start Field 2'b01: Start Others: Reserved	0x1
15:0	RW	MDIO_RW_DATA	MDIO Read/Write Data Field This is used as a MDIO data field for MDIO read/write data access. When the MDIO write command is activated, this is used as MDIO write data field for both read/write access. When MDIO read command is activated, this is used as MDIO read data field for read access only.	0x0

415. IMR: Interrupt Mask Register (offset: 0x7008)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	INT_MSK	Interrupt Mask 1'b0: The corresponding interrupt status on ISR will trigger an external interrupt signal. 1'b1: The corresponding interrupt status is masked or disabled.	0xFFFF

416. ISR: Interrupt Status Register (offset: 0x700C)

Bits	Type	Name	Description	Initial Value
31	RO	BMU_INIT	BMU Initialization Done	0x1
30	RO	ADDR_INIT	ADDR Initialization Done	0x1
29	RO	VLAN_INIT	VLAN Initialization Done	0x1
28	RO	ACL_INIT	ACL Initialization Done	0x1

Bits	Type	Name	Description	Initial Value
27:26	-	-	Reserved	0x0
25	RO	MIB_INT	MIB Interrupt Asserts when a bit status is set in the IntSn and AEISR registers. It only can be reset after CPU read-clears the corresponding register.	0x0
24	RO	ACL_INT	ACL Interrupt Asserts when a bit status is set in the AISR register. It only can be reset after CPU read-clears the corresponding register.	0x0
23:18	-	-	Reserved	0x0
17	W1C	BMU_TOUT_INT	BMU Timeout Interrupt Asserts when the internal free buffer count is less than FC_FREE_BLK_LOTHD*2 (GFCCR0[7:0]) and the no de-queue process lasts for longer than 80 ms.	0x0
16	W1C	GLOBAL_PORT_INT	Global Port Interrupt Asserts when a bit status is set in GPINT_STS and its corresponding enable signal GPINT_EN. Users should read-clear the GPINT_STS first and write-1 -clear GLOBAL_PORT_INT.	0x0
15	-	-	Reserved	0x0
14	W1C	TAG_ALERT	ARL VLAN Tag Admission Alert Status interrupt Asserts when an incoming frame is dropped by VLAN Security defined on PVC.ACC_FRM.	0x0
13	W1C	VLAN_ALERT	ARL VLAN Security Alert Status interrupt Asserts when an incoming frame is dropped by VLAN Security defined on PCR.PORT_VLAN.	0x0
12	W1C	8021X_ALERT	ARL 802.1x Lock Alert Status interrupt Asserts when an incoming frame is dropped by RX Port lock or SA lock defined on PSC.SA_LOCK or PSC.RX_PORT_LOCK	0x0
11	W1C	BC_ALERT	ARL Broadcast Storm Alert Status interrupt Asserts when an incoming frame is dropped by Broadcast Storm Suppression defined on register BSR.	0x0
10	W1C	EQ_OV_EXCP	ARL Enqueue Overflow Exception Status interrupt	0x0
9	W1C	PQ_OV_EXCP	ARL Packet Queue Overflow Exception Status interrupt	0x0
8	W1C	ING_OV_EXCP	ARL Ingress Parser Overflow Exception Status interrupt	0x0
7	-	-	Reserved	0x0
6	W1C	P6_LINK_CHG	Port 6 (CPU) Link Status Change interrupt	0x0
5	W1C	P5_LINK_CHG	Port 5 Link Status Change interrupt	0x0

Bits	Type	Name	Description	Initial Value
4	W1C	P4_LINK_CHG	Port 4 Link Status Change interrupt	0x0
3	W1C	P3_LINK_CHG	Port 3 Link Status Change interrupt	0x0
2	W1C	P2_LINK_CHG	Port 2 Link Status Change interrupt	0x0
1	W1C	P1_LINK_CHG	Port 1 Link Status Change interrupt	0x0
0	W1C	P0_LINK_CHG	Port 0 Link Status Change interrupt	0x0

NOTE: Where applicable,
Read

0: Not asserted
1: Asserted

Write

1: Clears this bit

417. CPC: CPU Port Control (offset: 0x7010)

Bits	Type	Name	Description	Initial Value
31	RW	SW_EN	Enable Switch Core Logic 1'b0: Reset switch core logic, but excludes control registers. 1'b1: Enable switch core logic function.	0x1
30	RW	PBUS_EN	Enable Packet Buffer Access from PBus 1'b0: Internal buffer is only used by switch. 1'b1: Enable PBus access to internal packet buffer	0x0
29:28	-	-	Reserved	0x0
27	RW	FE_XFC	Enable Port-based Flow Control on Frame Engine Allows the embedded switch to directly pause the frame engine. 0: Disable 1: Enable	0x1
26	RW	WAN_XFC	Enable LAN/WAN Flow Control on FE PDMA The individual PDMA Tx Ring of the frame engine can be paused due to the egress LAN/WAN port congestion on the embedded switch. 0: Disable 1: Enable	0x0
25	RW	SWQUE_XFC	Enable Per-Queue Flow Control on Embedded Switch The individual queue of the embedded switch can be paused due to the Rx Ring congestion on the frame engine. 0: Disable 1: Enable	0x0

Bits	Type	Name	Description	Initial Value
24	RW	FEQUE_XFC	Enable Per-Queue Flow Control on FE PDMA The individual PDMA Tx Ring of the frame engine can be paused due to the egress queue congestion on the embedded switch. 0: Disable 1: Enable	0x0
23:16	RW	LAN_PAMP	LAN Port Map Displays the distribution of LAN ports on the embedded switch.	0x3E
15:8	RW	FE2SW_IPG	CPU to Embedded Switch IPG The inter-frame clock gap (IPG) when the back-to-back frames are sent from the CPU to the embedded switch. $IPG = (FE2SW_IPG + 2) * 8 \text{ ns}$	0xc
7:0	RW	SW2FE_IPG	Embedded Switch to CPU IPG The inter-frame clock gap (IPG) when the back-to-back frames are sent from the embedded switch to the CPU.	0x0

NOTE: Where applicable,
0: Disable
1: Enable

418. GPC1: GIGA Port-I Control (offset: 0x7014)

Bits	Type	Name	Description	Initial Value
31	RW	OLT_MODE	Select EPHY OLT Test Mode 1'b0: EPHY is power saving mode 1'b1: EPHY is active for test mode	0x0
30:29	-	-	Reserved	0x0
28:24	RW	PHY_DIS	Disable Internal 5-port EPHY. 0: Enable 1: Disable	0x0
23:21	-	-	Reserved	0x7
20:16	RW	PHY_BASE	Internal EPHY Base Address Sets the base PHY address of the internal 5-port EPHY. When you change the default value, you need to reset EPHY again to get the new EPHY base address.	0x0
15:14	RW	LED_SEL	LED Source Selection 2'b00: LED mode #0 (refer to EPHY datasheet) 2'b01: LED mode #1 2'b10: LED mode #2 2'b11: Disable	0x0
13	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
12:8	RW	LED_POLAR	LED Polarity Ports 0 to 4 LED polarity control. 1'b0: LED Pin is low active 1'b1: LED Pin is high active	0x0
7:6	-	-	Reserved	0x0
5	RW	TMII_FREQ	TMII Frequency Selection 0: 33 MHz 1: 50 MHz	0x0
4	RW	TMII_MODE	TMII Mode Switch to Turbo MII interface.	0x0
3	RW	TX_CLK_MODE	P5 Tx Clock Control 0: HP mode (clock and data are in-phase) 1: 3Com mode (clock and data is 90 degree offset)	0x1
2	RW	RX_CLK_MODE	P5 RX Clock Control 0: Delay 2 ns on input RX_CLK 1: No delay	0x1
1:0	RW	RX_SKEW	P5 RX Clock Skew Control 00: No delay 01: Delay 150 ps 10: Delay 300 ps 11: Clock inversion	0x0

419. DBGP: Debug Probe Control (offset: 0x7018)

Bits	Type	Name	Description	Initial Value
31:16	RO	DBG_PROBE	Internal Probe Signals	0x0
15	RW	DBG_SEL	Internal Probe Selection 1'b0: Probe Mux is selected by DBG_MUX[14:4] and UTIF[3:0] 1'b1: Probe Mux is selected by DBG_MUX[14:0]	0x0
14:10	-	-	Reserved	0x1F
9:0	RW	DBG_PROBE_SEL	Probe Mux Selection See table below	0x3F0

DBG_PROBE_SEL[9:0]

9	8	7	6	5	4	3	2	1	0	Internal Probe Signals
0	3'h0 to 3'h6 (port select)			0	0	4'h0 to 4'hF				Pn MAC
				0	1	4'h0 to 4'hF				Pn Port Ctrl
				1	0	4'h0 to 4'hF				Pn Scheduler
				1	1	4'h0 to 4'hF				Reserved
0	1	1	1	6'h00 to 6'h3F					ARL	
1	0	0	7'h00 to 7'h7F					BMU (See NOTE below)		
1	0	1	0	0	5'h00 to 5'h1F					PB_CTRL
1	0	1	0	1	5'h00 to 5'h1F					SW_CORE
1	0	1	1	0	5'h00 to 5'h1F					Reserved
1	0	1	1	1	5'h00 to 5'h1F					Reserved
1	1	8'h00 to 8'hFE							Reserved	
1	1	1	1	1	1	1	1	1	1	Clock

NOTE: Sub-groups of BMU

1	0	0	0	0	5'h00 to 5'h1F	LMU (PL_CTRL)
1	0	0	0	1	5'h00 to 5'h1F	LMU (FL_CTRL)
					5'h00	{SW_CLK, P0_Q1_O127, P0_Q1_QCNT[6:0], P0_Q0_O127, P0_Q0_QCNT[6:0]}
					5'h01	{SW_CLK, P0_Q3_O127, P0_Q3_QCNT[6:0], P0_Q2_O127, P1_Q2_QCNT[6:0]}
					5'h02	{SW_CLK, P0_Q5_O127, P2_Q5_QCNT[6:0], P0_Q4_O127, P0_Q4_QCNT[6:0]}
					5'h03	{SW_CLK, P0_Q7_O127, P0_Q7_QCNT[6:0], P0_Q6_O127, P0_Q6_QCNT[6:0]}
					5'h04 to 5'h07	Port 1 egress queue buffer count
					5'h08 to 5'h1F	Port #
1	0	0	1	0	5'h00 to 5'h1F	RLT_PROC
1	0	0	1	1	5'h00 to 5'h1F	FCTRL

420. GPC2: GIGA Port-II Control (offset: 0x701C)

Bits	Type	Name	Description	Initial Value
31:24	RW	FE2SW_IPG	PPE to Embedded Switch IPG The inter-frame clock gap when the back-to-back frames are sent from the PPE to the embedded switch. The period of IPG = (FE2SW_IPG+2) * 8 ns	0x7
23:16	RW	SW2FE_IPG	Embedded Switch to PPE IPG The inter-frame clock gap when the back-to-back frames are sent from the embedded switch to the PPE.	0x0
15:6	-	-	Reserved	0x0
5	RW	TMII_FREQ	TMII Frequency Selection 0: 33 MHz 1: 50 MHz	0x0

Bits	Type	Name	Description	Initial Value
4	RW	TMII_MODE	TMII Mode Switch to Turbo MII interface.	0x0
3	RW	TX_CLK_MODE	P4 Tx Clock Control 0: HP mode (clock and data are in-phase) 1: 3Com mode (clock and data is 90 degree offset)	0x1
2	RW	RX_CLK_MODE	P4 Rx Clock Control 0: Delay 2 ns on input RX_CLK 1: No delay	0x1
1:0	RW	RX_SKEW	P4 Rx Clock Skew Control 00: No delay 01: Delay 150 ps 10: Delay 300 ps 11: Clock inversion	0x0

2.20.13 MDIO Control

2.20.13.1 IntPHY and ExtPHY address for MDIO

Ethernet Switch includes an internal 5-port EPHY and a 1 or 2 RGMII interface for the external EPHY modules. All EPHY can be accessed by a 2-wire MDC/MDIO serial management interface. Each EPHY slave can decode its own PHY address from MDC/MDIO and send the response to the MDIO master. The default address for the internal EPHY starts from 0x0 (GPC1.PHY_BASE) to 0x4.

Two addressing systems are possible and are shown below. As indicated in Figure 2-30 the EPHY address (ExtPHY5) of GE1 must follow GE2 by one. ExtPHY4 can share the same PHY address since SYSCFG1.GE2_MODE decides the GMAC4 interface – RJ45 or RGMII. Alternatively, IntPHY4 and ExtPHY4 can use a different PHY address, as shown in Figure 2-31. ExtPHY4 uses a different PHY address from IntPHY addresses and ExtPHY5 of GE1 must follow GE2 by one.

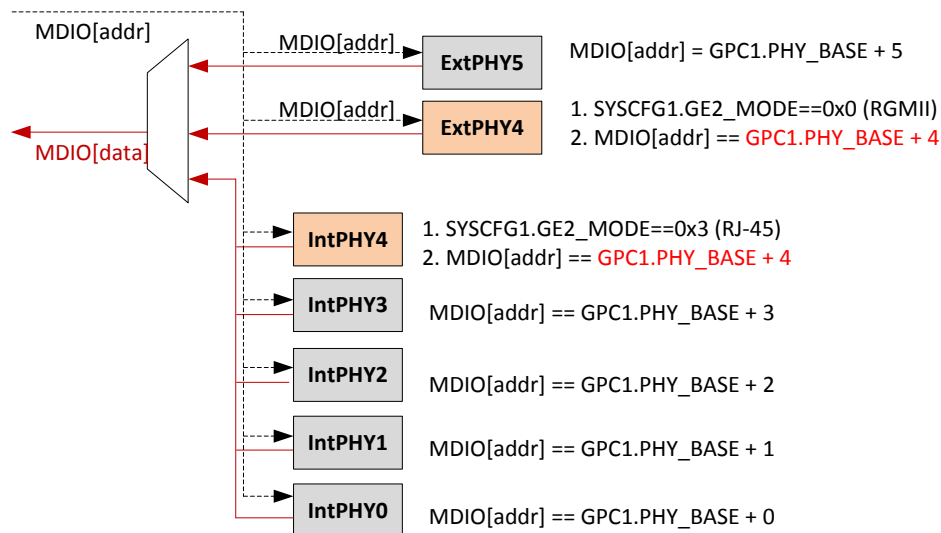


Figure 2-30 PHY Address Decoding (i)

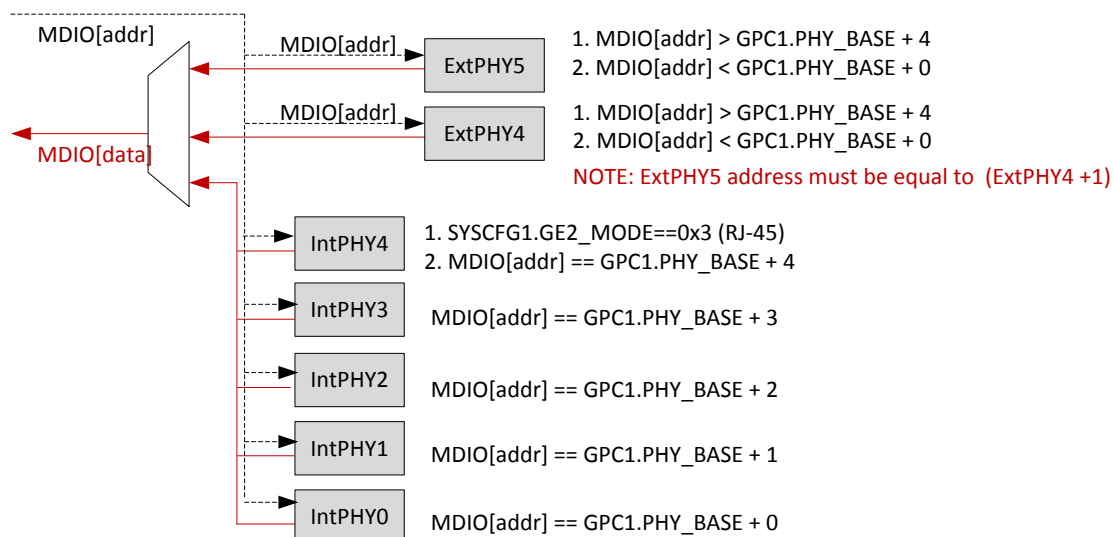


Figure 2-31 PHY Address Decoding (ii)

2.20.13.2 MDIO Register

These registers can be accessed by PIAC (PHY Indirect Access Control) indirectly. Among them, PHY register 0-1 and 4-6 are unique for each port. PHY register 2-3 are common for all 5 ports.

Legend:

SC: Self-clearing, RC: Read-clearing

LL: Latching Low, LH: Latching High

R/W: Read/write, RO: Read-Only

2.20.13.3 List of Registers

No.	CR Address	Register Name	Page
421	00(d00)	MII Control Register	350
422	01(d01)	MII Status Register	350
423	02(d02)	PHY Identifier Register	351
424	03(d03)	PHY Version Register	351
425	04(d04)	Auto-Negotiation Advertisement Register	351
426	05(d05)	Auto-Negotiation Link Partner (LP) Ability Register	352
427	06(d06)	Auto-Negotiation Expansion Register	352

2.20.13.4 Register Descriptions

421. MII Control Register, CR Address: 00(d00), Reset State: 3100

Bits	Type	Name	Description	Default
15	RW/SC	MR_MAIN_RESET	Resets all digital logic, except PHY_REG. 0: Normal 1: Reset	1'h0
14	RW	LOOPBACK_MII	MII loopback	1'h0
13	RW	FORCE_SPEED	0: 10 Mbps, when MR_AUTONEG_ENABLE = 1'b0 1: 100 Mbps	1'h1
12	RW	MR_AUTONEG_ENABLE	0: Normal 1: Enabled	1'h1
11	RW	POWERDOWN	Forces PHY to power down. Analog Tx, analog Rx, and analog AD are powered down.	1'h0
10	-	-	Reserved	1'h0
9	RW/SC	MR_RESTART_NEGOTIATION	0: Normal 1: Restart auto-negotiation	1'h0
8	RW	FORCE_DUPLEX	0: Half duplex, when MR_AUTONEG_ENABLE = 1'b0 1: Full duplex	1'h1
7:0		-	Reserved	8h00

422. MII Status Register, CR Address: 01(d01), Reset State: 7849

Bits	Type	Name	Description	Default
15	-	100 BASE T4	Not supported	1'h0
14	RO	100BASE-X Full Duplex	Indicates PHY supports full duplex 100BASE-X connections.	1'h1
13	RO	100BASE-X Half Duplex	Indicates PHY supports half duplex 100BASE-X connections.	1'h1
12	RO	10Mbps/s Full Duplex	Indicates PHY supports full duplex 10 Mbps connections.	1'h1
11	RO	10 Mb/s Half Duplex	Indicates PHY supports half duplex 10 Mbps connections.	1'h1
10	-	100BASE-T2 full duplex	Not supported	1'h0
9	-	100BASE-T2 half duplex	Not supported	1'h0
8:7	-	-	Reserved	2'h0
6	RO	MF Preamble Suppression	Indicates PHY accepts management frames with preamble suppression.	1'h1
5	RO	mr_autoneg_complete	Indicates the status of auto-negotiation. 0: Incomplete 1: Complete	1'h0
4	-	-	Reserved	1'h0

Bits	Type	Name	Description	Default
3	RO	Autoneg Ability	Indicates the availability of the PHY auto-negotiation capability. 0: PHY cannot auto-negotiate. 1: PHY can auto-negotiate.	1'h1
2	RO/LL	Link Status	Indicates link status. 0: Down 1: Up	1'h0
1	RO/LH/RC	Jabber Detect	Indicates whether a jabber condition is detected. 0: Not detected 1: Detected	1'h0
0	RO	Extended Capability	Indicates register capabilities. 0: Basic register set capabilities only 1: Extended register capabilities	1'h1

NOTE: Unless otherwise stated,
0: Not supported
1: Supported

423. PHY Identifier Register, CR Address: 02(d02), Reset State: 00C3

Bits	Type	Name	Description	Default
15:0	RO	PHY_ID[31-16]	OUI (bits 3-18). Ralink OUI = 000C43	16'h00c3

424. PHY Version Register, CR Address: 03(d03), Reset State: 0800

Bits	Type	Name	Description	Default
15:10	RO	PHY_ID[15-10]	OUI (bits 19-24)	6'h02
9:4	RO	PHY_ID[9-4]	Manufacturer's Model Number (bits 5-0)	6'h00
3:0	RO	PHY_ID[3-0]	Revision Number (bits 3:0); Register 3, bit 0 is LS bit of PHY Identifier	4'h0

425. Auto-Negotiation Advertisement Register, CR Address: 04(d04), Reset State: 05E1

Bits	Type	Name	Description	Default
15	RO	Next Page Enable	Indicates that the local device is set to use the next page. 0: Set to not use the next page. 1: Set to use the next page.	1'h0
14	-	-	Reserved	1'h0
13	RW	Remote Fault Enable	0: No remote fault 1: Auto-negotiation fault detected	1'h0
12:11	RO	Technology Ability A7-A6	Not Implemented	2'h0
10	RW	Technology Ability A5	Pause	1'h1
9	RO	Technology Ability A4	Not Implemented	1'h0
8	RW	100Base-TX Full Duplex Capable	0: Not Capable 1: Capable of Full Duplex	1'h1

Bits	Type	Name	Description	Default
7	RW	100 Base-TX Half Duplex Capable	0: Not Capable 1: Capable of Half Duplex	1'h1
6	RW	10 Base-T Full Duplex Capable	0: Not Capable 1: Capable of Full Duplex 10BASE-T	1'h1
5	RW	10 Base-T Half Duplex Capable	0: Not Capable 1: Capable of Half Duplex 10BASE-T	1'h1
4:0	RW	Selector Field	Identifies type of message	5'h01

426. Auto-Negotiation Link Partner (LP) Ability Register, CR Address: 05(d05), Reset State: 0000

Bits	Type	Name	Description	Default
15	RO	Next Page	0: Base page is requested. 1: Link partner is requesting next page function.	1'h0
14	RO	Acknowledge	0: Acknowledge not received. 1: Link partner acknowledge received successfully.	1'h0
13	RO	Remote Fault	0: No remote fault 1: Auto-negotiation fault detected.	1'h0
12:11	RO	Not implemented	Technology Ability A7-A6	2'h0
10	RO	Pause	Technology Ability A5	1'h0
9	RO	Not Implemented	Technology Ability A4	1'h0
8	RO	100Base-TX Full Duplex Capable	Indicates full duplex 100Base-TX connections are supported.	1'h0
7	RO	100 Base-TX Half Duplex Capable	Indicates half duplex 100Base-TX connections are supported.	1'h0
6	RO	10 Base-T Full Duplex Capable	Indicates full duplex 10Base-T connections are supported.	1'h0
5	RO	10 Base-T Half Duplex Capable	Indicates half duplex 10Base-T connections are supported.	1'h0
4:0	RO	Selector Field	Identifies type of message	5'h00

NOTE: Unless otherwise stated,

0: Not supported

1: Supported

427. Auto-Negotiation Expansion Register, CR Address: 06(d06), Reset State: 0000

Bits	Type	Name	Description	Default
15:5	-	-	Reserved	11'h0
4	RO/ LH/ RC	Parallel Detection Fault	Indicates that a local device parallel fault has been detected. 0: Not detected 1: Detected	1'h0
3	RO	Link Partner Next Page Able	Indicates that the link partner supports next paging. 0: Not supported 1: Supported	1'h0

Bits	Type	Name	Description	Default
2	RO	MR_NP_ABLE	Indicates that the local device supports next paging. 0: Not supported 1: Supported	1'h0
1	RO/ LH/ RC	Page Received	Indicates that a new page has been received. 0: Not received 1: Received	1'h0
0	RO	Link Partner Auto-negotiation Able	Indicates the link partner supports auto-negotiation. 0: Not supported 1: Supported	1'h0

2.21 PCI/PCIe Controller

PCI Express Controller

- Supports both RC(PCI-PCI bridge) and Endpoint mode
- Support PCIe Gen1 X1 lane
- Support maximum one external PCI Express endpoint when RC mode
- Supports PCI Express Active State Power Management (ASPM)
- Supports PCI Express Advanced Error Reporting

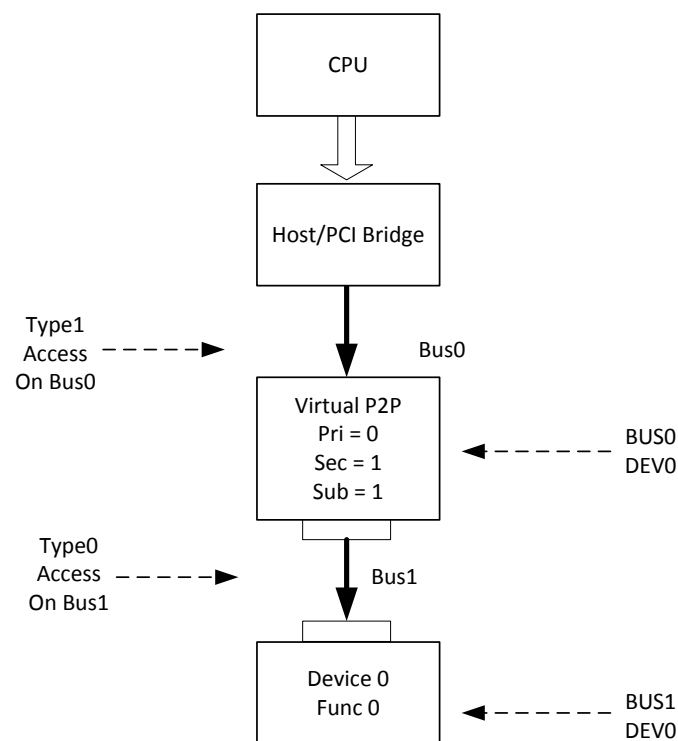


Figure 2-32 PCIe Host Topology

2.21.1 Block Diagram

2.21.1.1 Host bridge with PCIe Slot

AP Mode (as a standalone SoC)

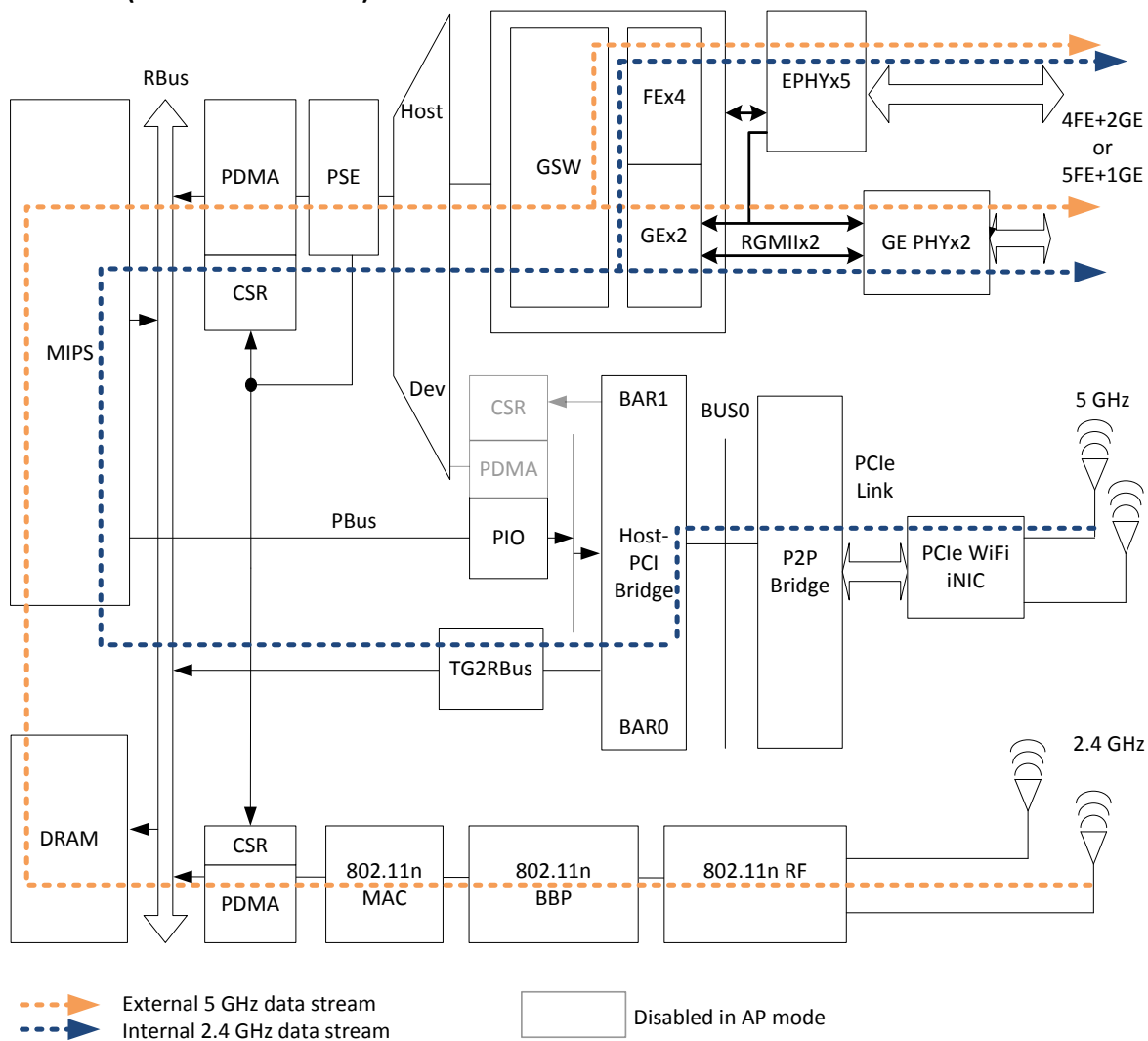


Figure 2-33 PCIe AP Mode

2.21.2 PCIe Controller Acting as a PCIe Device

For example, as shown in the following figure, MT7620 works as an intelligent NIC to offload the external third party SoC by performing wireless and Ethernet packet format conversion functions.

NOTE:

1. In this configuration, RGMII(port1) and PCIe interface are exclusive. That means you can select one of them as the iNIC host interface.
2. A dedicated PDMA can be seen by the third party SOC when MT7620 works as an intelligent NIC when the PCIe is selected as the interface. The operation of this PDMA is exactly the same as the one described in Frame Engine section. The first PDMA register can be accessed by PCI BAR1 in PCIe address space.

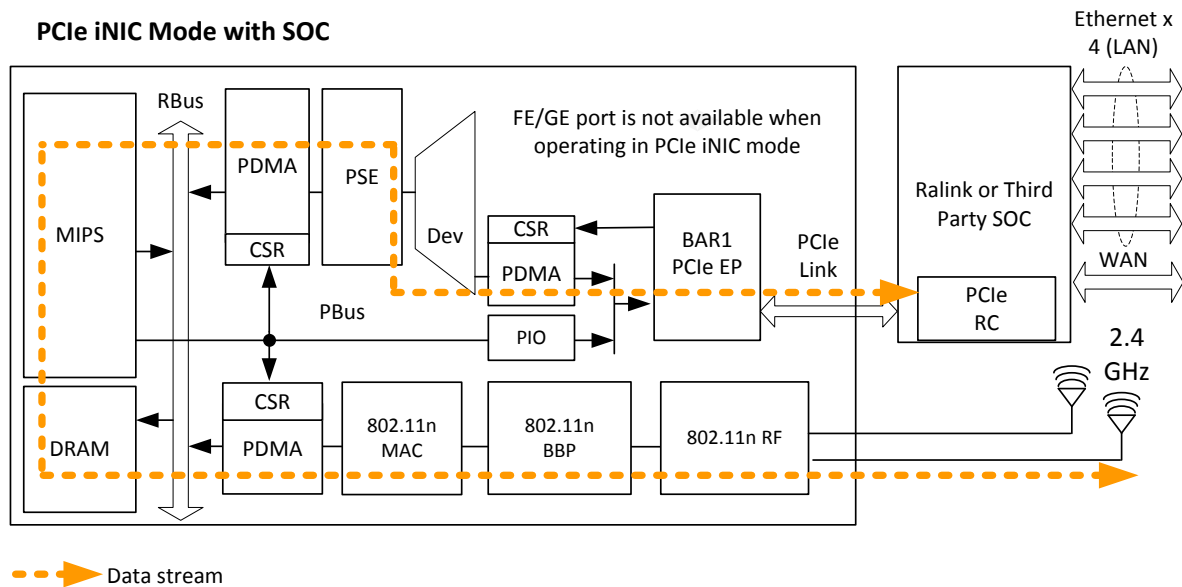


Figure 2-34 PCIe Controller Behaving as a PCIe Endpoint

Table 2-26 PCI/PCIe scenerio and relative control register settings

Pin Name	PCIe RC only	PCIe EP only	PCIe disable
PCIE_RC_MODE	1'b1	1'b0	Don't care
PCIE_SRST	1'b0	1'b0	1'b1
PCIE_CLK_EN	1'b1	1'b1	1'b0

2.21.3 Block Diagram

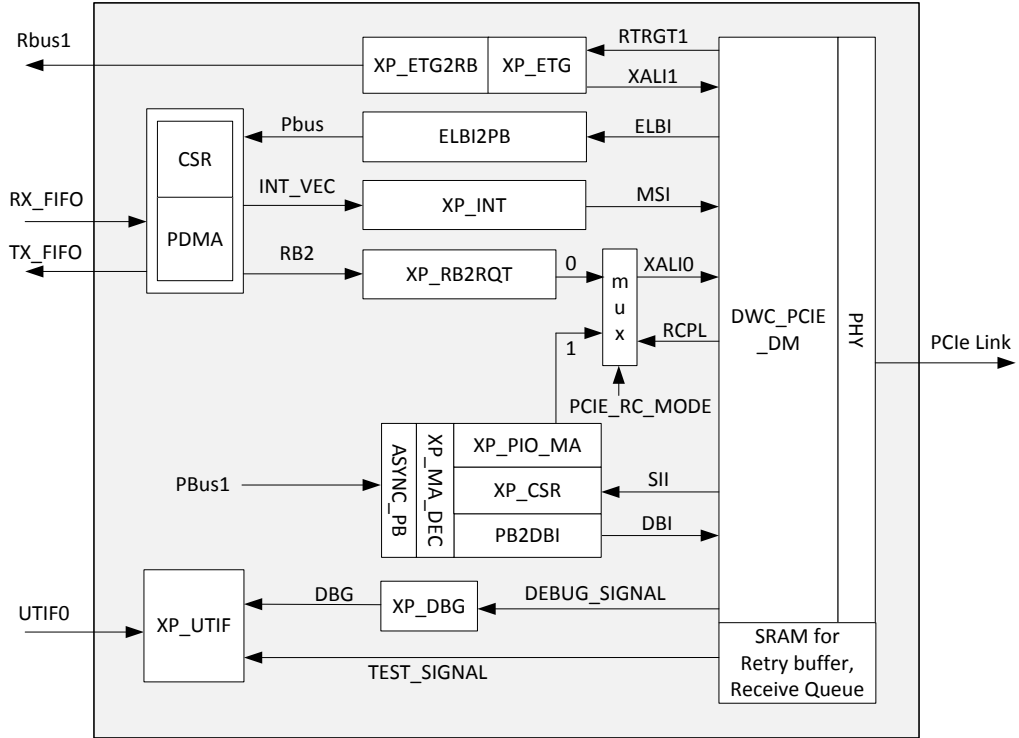


Figure 2-35 PCIe RC/EP Block Diagram

2.21.4 PCI/PCIe Master Access In Host Mode

For PCI/PCIe Memory space access, there are two approaches. One approach is fixed mapping the address space from 32'h2000_0000 to 32'h2FFF_FFFF (256 MByte). The other approach is PCI memory space programmable mapping which is supported via the membase register + memwin offset. For PCI I/O space access, the PCI controller supports programmable mapping via iobase register + iowin offset.

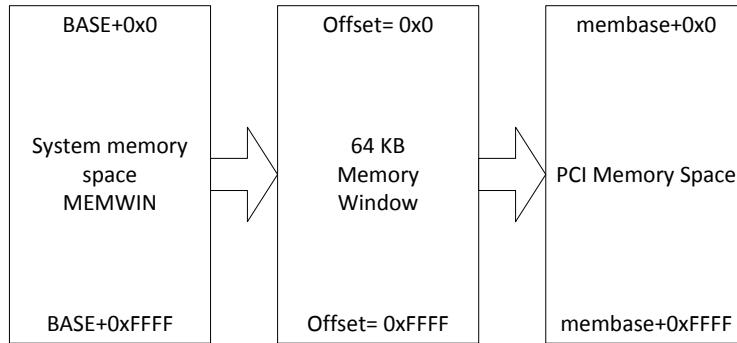


Figure 2-36 PCIe Memory Space Programmable Mapping

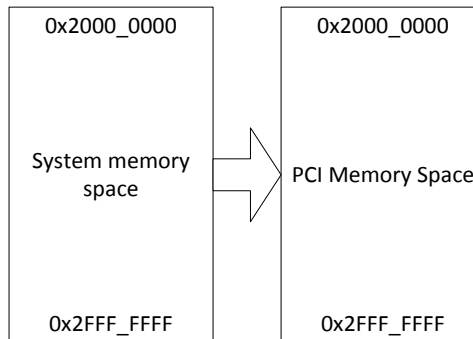


Figure 2-37 PCI Memory Space Fixed Mapping

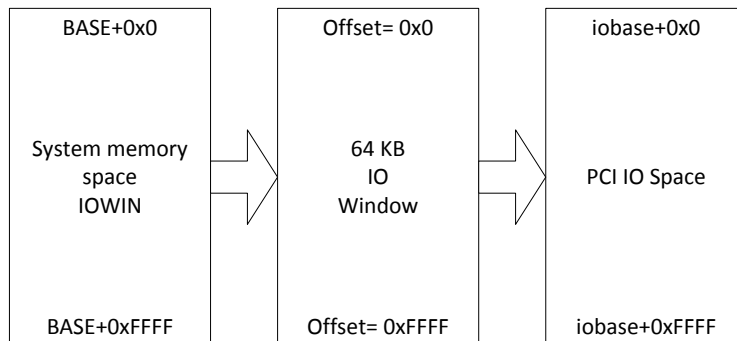


Figure 2-38 I/O Space Programmable Mapping

2.21.5 PCIe Controller Host Mode Initialization Example

1. Set the PCIRST bit in PCICFG register to assert reset the PCI device card, then reset the PCIRST bit to de-assert the reset output.
2. PCI driver performs PCI scan to detect PCIe devices and make device initialization.

2.21.6 Host-PCI Bridge Registers (base: 0x1014_0000)

2.21.6.1 List of Registers

No.	Offset	Register Name	Description	Page
428	0x0000	PCICFG	PCI Configuration and Status Register	360
429	0x0008	PCIINT	PCI Interrupt After Enable Mask	360
430	0x000C	PCIENA	PCI Interrupt Enable	360
431	0x0020	CFGADDR	CONFIG_ADDR Register	361
432	0x0024	CFGDATA	CONFIG_DATA Register	361
433	0x0028	MEMBASE	Base Address for Memory Space Window	361
434	0x002C	IOBASE	Base Address for IO Space Window	361
435	0x0090	PHY0_CFG	PCIe PHY0 Control Register via SPI Configuration	362

2.21.6.2 Register Descriptions

428. PCICFG: PCI Configuration and Status Register (offset: 0x0000)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:20	RW	P2P_BR_DEVNUM1	Device number setting of Virtual PCI-PCI bridge #1.	0x1
19:16	RW	P2P_BR_DEVNUM0	Device number setting of Virtual PCI-PCI bridge #0.	0x0
15:3	-	-	Reserved	-
2	-	-	Reserved	-
1	RW	PCIRST	PCI Reset Control 0: De-assert the PERST_N pin. 1: Assert the PERST_N pin. This bit is set to 1 at chip reset. (Available when PCIe Controller in Host mode)	0x1
0	-	-	Reserved	0x0

429. PCIINT: PCI Interrupt After Enable Mask (offset: 0x0008)

Bits	Type	Name	Description	Initial Value
31:22	-	-	Reserved	0x0
21	RO	PCIINT3	PCIe1 Interrupt Input in Host Mode This bit indicates the PCIe interrupt from PCIe1 slot.	0x0
20	RO	PCIINT2	PCIe0 Interrupt Input in Host Mode This bit indicates the PCIe interrupt from PCIe0 slot.	0x0
19	-	PCIINT1	Reserved	0x0
18	-	PCIINT0	Reserved	0x0
17:0	-	-	Reserved	0x0

430. PCIENA: PCI Interrupt Enable (offset: 0x000C)

Bits	Type	Name	Description	Initial Value
31:22	-	-	Reserved	0x0
21	RW	PCIINT3	PCIe1 Interrupt Input in RC (Root Complex) mode 0: Disable PCIe interrupt 1: Enable PCIe interrupt	0x0
20	RW	PCIINT2	PCIe0 Interrupt Input in RC Mode 0: Disable PCIe interrupt 1: Enable PCIe interrupt	0x0
19	-	PCIINT1	Reserved	0x0
18	-	PCIINT0	Reserved	0x0
17:0	-	-	Reserved	0x0

431. CFGADDR: CONFIG_ADDR Register (offset: 0x0020)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:24	RW	EXTREGNUM	Extent Register Number only available for PCIe	0x0
23:16	RW	BUSNUM	Bus Number	0x0
15:11	RW	DEVICENUM	Device Number	0x0
10:8	RW	FUNNUM	Function Number	0x0
7:2	RW	REGNUM	Register Number	0x0
1:0	-	-	Reserved	0x0

432. CFGDATA: CONFIG_DATA Register (offset: 0x0024)

Bits	Type	Name	Description	Initial Value
31:0	RW	CFGDATA	Configuration Data Register Writes or reads of this register generate a configuration cycle in host mode.	-

433. MEMBASE: Base Address for Memory Space Window (offset: 0x0028)

Bits	Type	Name	Description	Initial Value
31:16	RW	MEMBASE	Base Address for Memory Space Window This register specifies the base address of PCI memory space for master PIO accesses to PCI Memory space. When CPU accesses any of the MEMWIN registers, the PCI Controller will issue a single MEM r/w transfer to the PCI Memory address of MEMBASE+MEMWINx NOTE: This register is only used when the PCI core is in host mode.	0x0
15:0	-	-	Reserved	0x0

434. IOBASE: Base Address for IO Space Window (offset: 0x002C)

Bits	Type	Name	Description	Initial Value
31:16	RW	IOBASE	Base Address for IO Space Window This register specifies the base address of PCI IO space for master PIO accesses to external PCI IO space. When CPU accesses any of the IOWIN registers, the PCI Controller will issue a single IO r/w transfer to the PCI IO address of IOBASE+IOWINx. NOTE: This register is only used when the PCI core is in host mode.	0x1016
15:0	-	-	Reserved	0x0

435. PHY0_CFG: PCIe PHY0 Control Register via SPI Configuration (offset: 0x0090)

Bits	Type	Name	Description	Initial Value
31	R	SPI_BUSY	SPI Busy Status 0: Idle 1: Busy	0x0
30:24	-	-	Reserved	-
23	RW	SPI_WR	SPI Write Sets the SPI transfer to read or write. 0: Read 1: Write	0x0
22:16	-	-	Reserved	-
15:8	RW	SPI_ADDR	SPI Address Indicates the address for SPI master to access the PCIe PHY control register.	0x0
7:0	RW	SPI_DATA	SPI Data <i>Write</i> Contains data to be written to the PHY control register based on the SPI_ADDR field. <i>Read</i> Displays the value of the PHY control register. The data address is already written to the SPI_ADDR field. The SPI_BUSY flag indicates whether the data is ready to be read. Examples: 1. SPI write write data=0x55 to addr=0x33 Poll PHY0_CFG.SPI_BUSY bit until it becomes 0 then Set PHY0_CFG=0x00803355 2. SPI read write data from addr=0x33 Poll PHY0_CFG.SPI_BUSY bit until it becomes 0 then Set PHY0_CFG=0x00003300 Poll PHY0_CFG.SPI_BUSY bit until it becomes 0 then Rdata = PHY0_CFG.SPI_DATA	0x0

2.21.7 PCIe0 RC Control Registers (base: 0x1014_2000)

2.21.7.1 List of Registers

No.	Offset	Register Name	Description	Page
436	0x0010	PCIE0_BAR0SETUP	Setup for BAR0 of PCIe Controller	364
437	0x0014	PCIE0_BAR1SETUP	Setup for BAR1 of PCIe Controller	365
438	0x0018	PCIE0_IMBASEBAR0	Internal Memory Base address for BAR0 Space of PCIe Controller	366
439	0x0030	PCIE0_ID	Vendor and Device ID of PCIe Controller	366
440	0x0034	PCIE0_CLASS	Class Code and Revision ID of PCIe Controller	366
441	0x0038	PCIE0_SUBID	Sub Vendor and Device ID of PCIe Controller	366
442	0x0050	PCIE0_STATUS	PCIe Status Register	366
443	0x0060	DLECR	Datalink Layer Error Counter Register	366
444	0x0064	ECRC	Error Counter Register	367

2.21.7.2 Register Descriptions

436. PCIE0_BAROSETUP: Setup for BAR0 of PCIe Controller (offset: 0x0010)

Bits	Type	Name	Description	Initial Value																																				
31:16	RW	BAR0MSK	Mask Setup for Base Address Register BAR0 0: The corresponding address bit will be used for address comparison to determine an address hit. Each base address register can be mapped from 64 KB to 2 GB. 1: The corresponding address bit will be masked as a hit as if no address comparison has been made. The mask bit will be ignored when the corresponding enable bit is 0. <table><tr><td>BAR0MSK[31:16]</td><td>Space</td></tr><tr><td>Others</td><td>Not supported</td></tr><tr><td>0111111111111111</td><td>2 GB</td></tr><tr><td>0011111111111111</td><td>1 GB</td></tr><tr><td>0001111111111111</td><td>512 MB</td></tr><tr><td>0000111111111111</td><td>256 MB</td></tr><tr><td>0000011111111111</td><td>128 MB</td></tr><tr><td>0000001111111111</td><td>64 MB</td></tr><tr><td>0000000111111111</td><td>32 MB (default)</td></tr><tr><td>0000000011111111</td><td>16 MB</td></tr><tr><td>0000000001111111</td><td>8 MB</td></tr><tr><td>0000000000111111</td><td>4 MB</td></tr><tr><td>0000000000011111</td><td>2 MB</td></tr><tr><td>0000000000001111</td><td>1 MB</td></tr><tr><td>0000000000000011</td><td>512 KB</td></tr><tr><td>0000000000000001</td><td>256 KB</td></tr><tr><td>0000000000000000</td><td>128 KB</td></tr><tr><td>0000000000000000</td><td>64 KB</td></tr></table> NOTE: Set this value before the CfgWr to BAR0, otherwise the result of CFGWr to BAR0 will be unknown.	BAR0MSK[31:16]	Space	Others	Not supported	0111111111111111	2 GB	0011111111111111	1 GB	0001111111111111	512 MB	0000111111111111	256 MB	0000011111111111	128 MB	0000001111111111	64 MB	0000000111111111	32 MB (default)	0000000011111111	16 MB	0000000001111111	8 MB	0000000000111111	4 MB	0000000000011111	2 MB	0000000000001111	1 MB	0000000000000011	512 KB	0000000000000001	256 KB	0000000000000000	128 KB	0000000000000000	64 KB	0x1ff
BAR0MSK[31:16]	Space																																							
Others	Not supported																																							
0111111111111111	2 GB																																							
0011111111111111	1 GB																																							
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0000111111111111	256 MB																																							
0000011111111111	128 MB																																							
0000001111111111	64 MB																																							
0000000111111111	32 MB (default)																																							
0000000011111111	16 MB																																							
0000000001111111	8 MB																																							
0000000000111111	4 MB																																							
0000000000011111	2 MB																																							
0000000000001111	1 MB																																							
0000000000000011	512 KB																																							
0000000000000001	256 KB																																							
0000000000000000	128 KB																																							
0000000000000000	64 KB																																							
15:1	-	-	Reserved	0x0																																				
0	RW	BAR0ENB	Base Address Register BAR0 Enable 1'b0: The BAR0 register will not be created and the mask bit will be ignored. 1'b1: The BAR0 register will be created and the mask bit will be decoded.	0x1																																				

437. PCIE0_BAR1SETUP: Setup for BAR1 of PCIe Controller (offset: 0x0014)

Bits	Type	Name	Description	Initial Value																																				
31:16	RW	BAR1MSK	Mask Setup for Base Address Register BAR1 0: The corresponding address bit will be used for address comparison to determine an address hit. Each base address register can be mapped from 64 KB to 2 GB. 1: The corresponding address bit will be masked as a hit as if no address comparison has been made. The mask bit will be ignored when the corresponding enable bit is '0'. <table><tr><td>BAR0MSK[31:16]</td><td>Space</td></tr><tr><td>Others</td><td>Not supported</td></tr><tr><td>0111111111111111</td><td>2 GB</td></tr><tr><td>0011111111111111</td><td>1 GB</td></tr><tr><td>0001111111111111</td><td>512 MB</td></tr><tr><td>0000111111111111</td><td>256 MB</td></tr><tr><td>0000011111111111</td><td>128 MB</td></tr><tr><td>0000001111111111</td><td>64 MB</td></tr><tr><td>0000000111111111</td><td>32 MB (default)</td></tr><tr><td>0000000011111111</td><td>16 MB</td></tr><tr><td>0000000001111111</td><td>8 MB</td></tr><tr><td>0000000000111111</td><td>4 MB</td></tr><tr><td>0000000000011111</td><td>2 MB</td></tr><tr><td>0000000000001111</td><td>1 MB</td></tr><tr><td>0000000000000111</td><td>512 KB</td></tr><tr><td>0000000000000011</td><td>256 KB</td></tr><tr><td>0000000000000001</td><td>128 KB</td></tr><tr><td>0000000000000000</td><td>64 KB</td></tr></table> NOTE: Set this value before the CfgWr to BAR0, otherwise the result of CFGWr to BAR0 will be unknown.	BAR0MSK[31:16]	Space	Others	Not supported	0111111111111111	2 GB	0011111111111111	1 GB	0001111111111111	512 MB	0000111111111111	256 MB	0000011111111111	128 MB	0000001111111111	64 MB	0000000111111111	32 MB (default)	0000000011111111	16 MB	0000000001111111	8 MB	0000000000111111	4 MB	0000000000011111	2 MB	0000000000001111	1 MB	0000000000000111	512 KB	0000000000000011	256 KB	0000000000000001	128 KB	0000000000000000	64 KB	0x0
BAR0MSK[31:16]	Space																																							
Others	Not supported																																							
0111111111111111	2 GB																																							
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0000001111111111	64 MB																																							
0000000111111111	32 MB (default)																																							
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0000000001111111	8 MB																																							
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0000000000000111	512 KB																																							
0000000000000011	256 KB																																							
0000000000000001	128 KB																																							
0000000000000000	64 KB																																							
15:1	-	-	Reserved	0x0																																				
0	RW	BAR1ENB	Base Address Register BAR1 Enable 1'b0: The BAR1 register will not be created and the mask bit will be ignored. 1'b1: The BAR1 register will be created and the mask bit will be decoded.	0x1																																				

438. PCIE0_IMBASEBAR0: Internal Memory Base address for BAR0 Space of PCIe Controller (offset: 0x0018)

Bits	Type	Name	Description	Initial Value
31:16	RW	IMBASEBAR0	Internal Memory Base address for BAR0 This register is used when CHIP behaves as a PCI Express RC. The actual internal memory address being accessed by an external PCI host can be obtained from the following formula: CHIP address begin accessed = (PCI Address – BAR0) + IMBASEBAR0. When writing to this register, the related bit will take effect when the corresponding bit in BAR0MSK bit is 1 and BAR0ENB is 1.	0x0
15:0	-	-	Reserved	0x0

439. PCIE0_ID: Vendor and Device ID of PCIe Controller (offset: 0x0030)

Bits	Type	Name	Description	Initial Value
31:16	RW	DEVID	Device ID	0x801
15:0	RW	VENID	Vendor ID	0x1814

440. PCIE0_CLASS: Class Code and Revision ID of PCIe Controller (offset: 0x0034)

Bits	Type	Name	Description	Initial Value
31:8	RW	CCODE	Class Code	0xd8000
7:0	RW	REVID	Revision ID	0x1

441. PCIE_SUBID: Sub Vendor and Device ID of PCIe Controller (offset: 0x0038)

Bits	Type	Name	Description	Initial Value
31:16	RW	SUBSYSID	Sub System ID	0x6352
15:0	RW	SUBVENID	Sub Vendor ID	0x1814

This register is valid when PCIE_RC_MODE = 0. See SYSCFG1 (offset: 0x0014).

442. PCIE0_STATUS: PCIe Status Register (offset: 0x0050)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	0x0
0	RO	PCIE_LINK_UP_ST	PCIe LTSSM Link up indicator This bit will reflect the PCIe link up status. Users can use this bit to see if any device is plugged into the slot.	0x0

443. DLECR: Datalink Layer Error Counter Register (offset: 0x0060)

Bits	Type	Name	Description	Initial Value
31:0	W1C	DLLP_ERR_CNT	Datalink Layer Error Counter Records how many times a datalink layer error occurred.	0x0

444. ECRC: Error Counter Register (offset: 0x0064)

Bits	Type	Name	Description	Initial Value
31:0	W1C	ECRC_ERR_CNT	ECRC Error Counter Records how many times an ECRC error occurred.	0x0

2.21.8 Memory Windows Registers (base: 0x1015_0000)

445. MEMWINx: PCI Memory Space Access Window (offset: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	RW	MEMWIN	PCI Memory Space Access Window <i>Read</i> Initiates a bus master read access to an external PCI device's memory space. <i>Write</i> Initiates a bus master write access to an external PCI device's memory space. The address accessed is specified as requested address (0 if MEMWIN00 is accessed, 4 if MEMWIN04 is accessed, etc.) plus MEMBASE.	0x0

2.21.9 IO Windows (base: 0x1016_0000)

446. IOWINx: PCI IO Space Access Window (offset: 0x0002_0000)

Bits	Type	Name	Description	Initial Value
31:0	RW	IOWIN	PCI IO Space Access Window <i>Read</i> Initiates a bus master read access to an external PCI device's IO space. <i>Write</i> Initiates a bus master write access to an external PCI device's IO space; The address accessed is specified as requested address (0 if IOWIN00 is accessed, 4 if IOWIN04 is accessed, etc.) plus IOBASE. NOTE: This register is only used when the PCI core is functioning as a master.	0x0

2.22 802.11n 2T2R MAC/BBP

2.22.1 Features

- 1x1/1x2/2x1/2x2 modes
- 300 MHz PHY Rate Support
- Legacy and high throughput modes
- 20 MHz/40 MHz bandwidth
- Reverse direction data flow and frame aggregation
- WEP 64/128, WPA, WPA2 Support
- QoS – WMM, WMM-PS
- Wake-on wireless LAN
- Multiple BSSID support
- Supports international standards - 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 compliance
- Bluetooth Co-existence
- Low power with advanced power management

2.22.2 Block Diagram

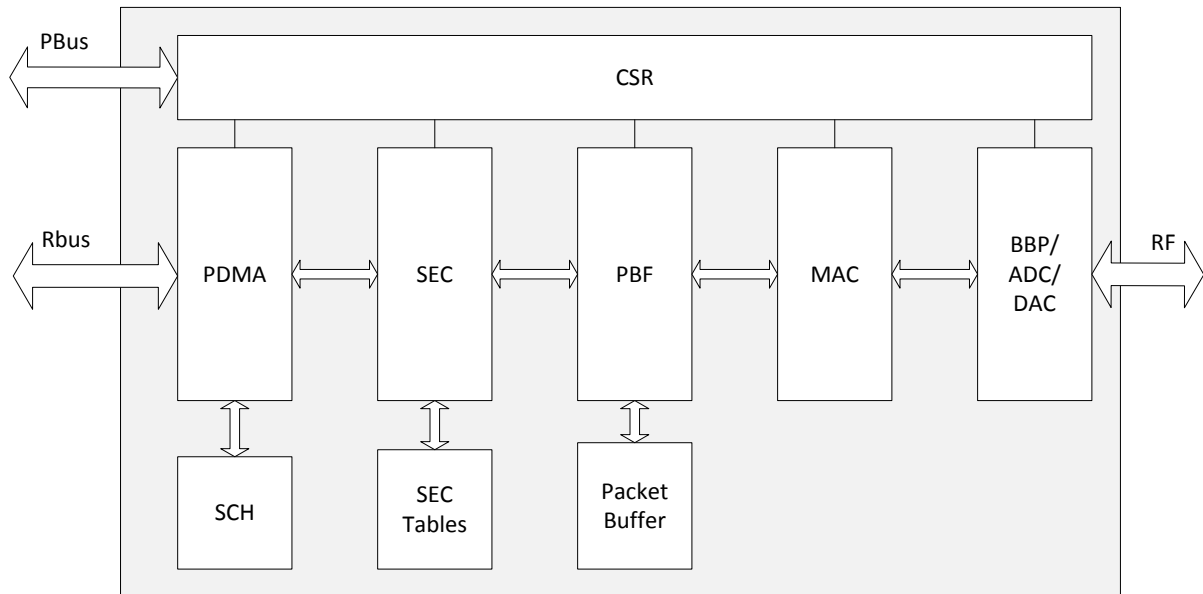


Figure 2-39 802.11n 2T2R MAC/BBP Block Diagram

2.22.3 802.11n 2T2R MAC/BBP Register Map

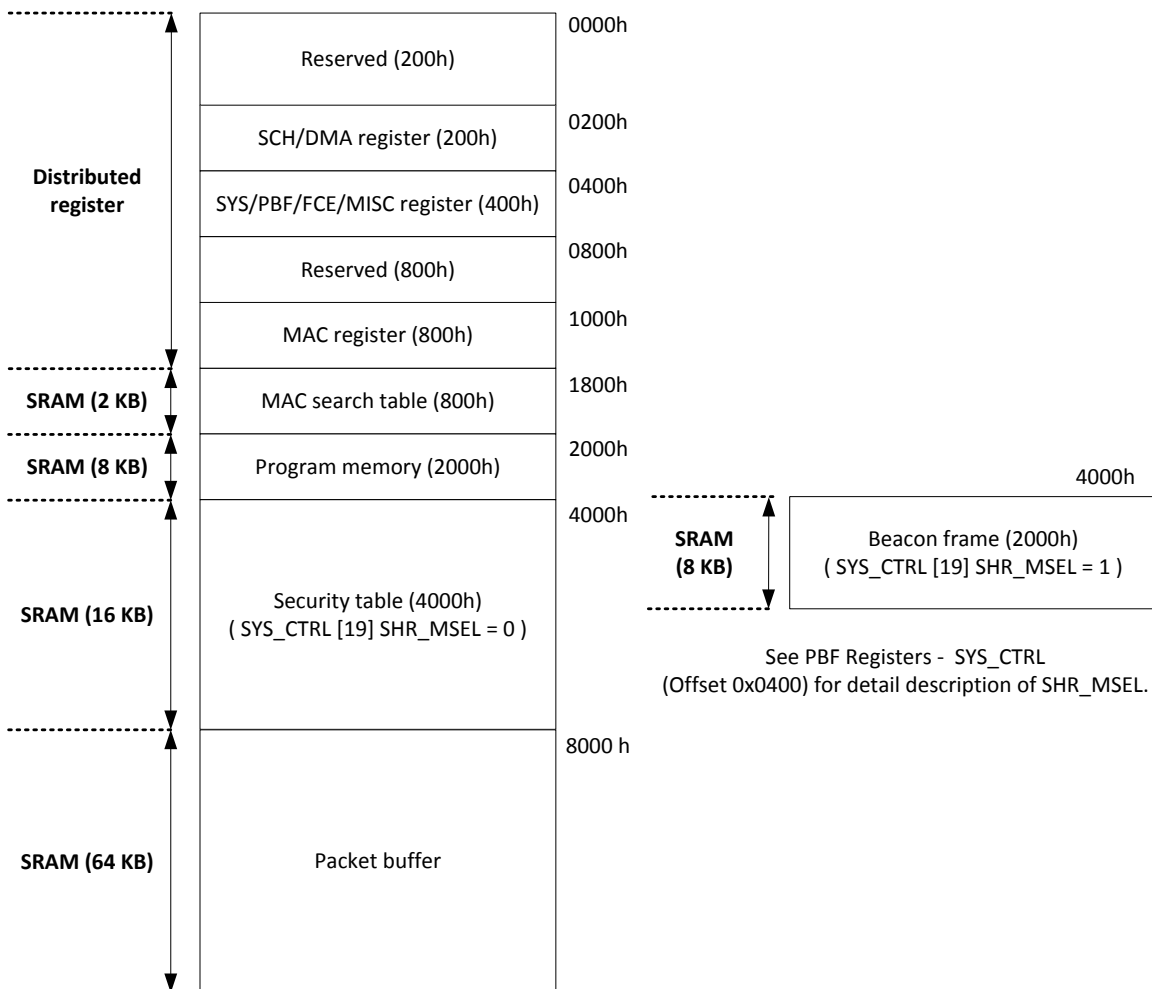


Figure 2-40 802.11n 2T2R MAC/BBP Register Map

2.22.4 SCH/WPDMA Registers (base: 0x1018_0000)

2.22.4.1 List of Registers

No.	Offset	Register Name	Description	Page
447	0x0200	INT_STATUS	Interrupt Status	371
448	0x0204	INT_MASK	Interrupt Mask	372
449	0x0208	WPDMA_GLO_CFG	WPDMA Global Configuration	374
450	0x020C	WPDMA_RST_IDX	WPDMA Reset Index	375
451	0x0210	DELAY_INT_CFG	Delay Interrupt Configuration	376
452	0x0214	WMM_AIFSN_CFG	Wi-Fi MultiMedia (WMM) Arbitration Inter-Frame Spacing Number Configuration	377
453	0x0218	WMM_CWMIN_CFG	WMM Minimum Contention Window Configuration	377
454	0x021C	WMM_CWMAX_CFG	WMM Maximum Contention Window Configuration	378
455	0x0220	WMM_TXOP0_CFG	WMM Transmit Opportunity 0 Configuration	379
456	0x0224	WMM_TXOP1_CFG	WMM Transmit Opportunity 1 Configuration	379
457	0x0230, 0x0240, 0x0250, 0x0260, 0x0270, 0x0280	TX_BASE_PTR_n	Transmit Base Pointer 0	379
458	0x0234, 0x0244, 0x0254, 0x0264, 0x0274, 0x0284	TX_MAX_CNT_n	Transmit Maximum Count 0	379
459	0x0238, 0x0248, 0x0258, 0x0268, 0x0278, 0x0288	TX_CTX_IDX_n	Transmit CPU Transmit Index 0	380
460	0x023C, 0x024C, 0x025C, 0x026C, 0x027C, 0x028C	TX_DTX_IDX_n	Transmit DMA Transmit Index 0	380
461	0x0290	RX_BASE_PTR	Receive Base Address Pointer	380
462	0x0294	RX_MAX_CNT	Receive Maximum Count	380
463	0x0298	RX_CALC_IDX	Receive CPU Allocate Index	380
464	0x029C	FS_DRX_IDX	Frequency Domain Spreading DMA Receive Index	380
465	0x02A4	US_CYC_CNT	USB Cycle Count	381

2.22.4.2 Register Descriptions

447. INT_STATUS: (offset: 0x0200)

Bits	Type	Name	Description	Initial Value
31:21	-	-	Reserved	0x0
20	R/ W1C	RADAR_INT	Baseband Radar Interrupt Asserts when the BBP has detected radar tones.	0x0
19:18	-	-	Reserved	0x0
17	R/ W1C	TX_COHERENT	Tx Coherent Interrupt Asserts when the Tx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0
16	R/ W1C	RX_COHERENT	Rx Coherent Interrupt Asserts when the Rx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0
15	R/ W1C	MAC_INT_4	MAC Interrupt 4: General Purpose Timer Interrupt Asserts when the GP timer has timed out. Configure this timer using the INT_TIMER_CFG register.	0x0
14	R/ W1C	MAC_INT_3	MAC Interrupt 3: Auto-wakeup Interrupt Asserts when the auto-wakeup function has been triggered. Configure this interrupt using the AUTO_WAKEUP_CFG register.	0x0
13	R/ W1C	MAC_INT_2	MAC Interrupt 2: Tx Status Interrupt Asserts when the status of the Tx queue becomes valid.	0x0
12	R/ W1C	MAC_INT_1	MAC Interrupt 1: Pre-TBTT Interrupt Asserts at an interval before the TBTT interrupt is triggered. Configure this interrupt using the INT_TIMER_CFG register.	0x0
11	R/ W1C	MAC_INT_0	Asserts when the TBTT timer has counted down to zero. Configure this interrupt using the BCN_TIME_CFG register.	0x0
10	RO	TX_RX_COHERENT	Tx/Rx Coherent Interrupt Asserts when TX_COHERENT [17] or RX_COHERENT [18] asserts.	0x0
9	R/ W1C	MCU_CMD_INT	MCU Command Interrupt Asserts when MCU has made a command and asserted an interrupt to the host.	0x0
8	R/ W1C	TX_DONE_INT5	Tx Queue 5 Done Interrupt Asserts when a Tx Queue 5 packet is transmitted.	0x0

Bits	Type	Name	Description	Initial Value
7	R/ W1C	TX_DONE_INT4	Tx Queue 4 Done Interrupt Asserts when a Tx Queue 4 packet is transmitted.	0x0
6	R/ W1C	TX_DONE_INT3	Tx Queue 3 Done Interrupt Asserts when a Tx Queue 3 packet is transmitted.	0x0
5	R/ W1C	TX_DONE_INT2	Tx Queue 2 Done Interrupt Asserts when a Tx Queue 2 packet is transmitted.	0x0
4	R/ W1C	TX_DONE_INT1	Tx Queue 1 Done Interrupt Asserts when a Tx Queue 1 packet is transmitted.	0x0
3	R/ W1C	TX_DONE_INT0	Tx Queue 0 Done Interrupt Asserts when a Tx Queue 0 packet is transmitted.	0x0
2	R/ W1C	RX_DONE_INT	Rx Done Interrupt Asserts when an Rx packet is received.	0x0
1	R/ W1C	TX_DLY_INT	Tx Delay Interrupt Asserts when the number of pending Tx interrupts has reached a specified level, or when the pending time is reached. Configure this interrupt using the DELAY_INT_CFG register.	0x0
0	R/ W1C	RX_DLY_INT	Tx Delay Interrupt Asserts when the number of pended Rx interrupts has reached a specified level, or when the pending time is reached. Configure this interrupt using the DELAY_INT_CFG register.	0x0

NOTE:

Read

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

448. INT_MASK: (offset: 0x0204)

Bits	Type	Name	Description	Initial Value
31:21	-	-	Reserved	0x0
20	RW	RADAR_INT_EN	Enables the Baseband Radar interrupt. This interrupt asserts when the BBP has detected radar tones.	0x0
19:18	-	-	Reserved	0x0
17	RW	TX_COHERENT_EN	Enables the Tx Coherent interrupt. This interrupt asserts when the Tx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0

Bits	Type	Name	Description	Initial Value
16	RW	RX_COHERENT_EN	Enables the Rx Coherent interrupt. This interrupt asserts when the Rx DMA is ready to handle a queue, but cannot access the queue because the driver is not ready.	0x0
14	RW	MAC_INT4_EN	Enables MAC interrupt 4: General Purpose timer interrupt. This interrupt indicates the GP timer has timed out. Configure this timer using the INT_TIMER_CFG register.	0x0
14	RW	MAC_INT3_EN	Enables MAC interrupt 3: Auto wakeup interrupt. This interrupt asserts when the auto-wakeup function has been triggered. Configure this interrupt using the AUTO_WAKEUP_CFG register.	0x0
13	RW	MAC_INT2_EN	Enables MAC interrupt 2: Tx status interrupt. This interrupt asserts when the status of the Tx queue becomes valid.	0x0
12	RW	MAC_INT1_EN	Enables MAC interrupt 1: Pre-TBTT interrupt. This interrupt asserts at an interval before the TBTT interrupt is triggered. Configure this interrupt using the INT_TIMER_CFG register.	0x0
11	RW	MAC_INT0_EN	Enables MAC interrupt 0: TBTT interrupt. This interrupt asserts when the TBTT timer has counted down to zero. Configure this interrupt using the TBTT_TIMER register.	0x0
10	-	-	Reserved	0x0
9	RW	MCU_CMD_INT_MSK	Masks the MCU Command interrupt. This interrupt asserts when MCU has made a command and asserted an interrupt to the host.	0x0
8	RW	TX_DONE_INT_MSK5	Masks the Tx Queue 5 Done interrupt. This interrupt asserts when Tx Queue 5 has transmitted a packet.	0x0
7	RW	TX_DONE_INT_MSK4	Masks the Tx Queue 4 Done interrupt. This interrupt asserts when Tx Queue 4 has transmitted a packet.	0x0
6	RW	TX_DONE_INT_MSK 3	Masks the Tx Queue 3 Done interrupt. This interrupt asserts when Tx Queue 3 has transmitted a packet.	0x0
5	RW	TX_DONE_INT_MSK 2	Masks the Tx Queue 2 Done interrupt. This interrupt asserts when Tx Queue 2 has transmitted a packet.	0x0
4	RW	TX_DONE_INT_MSK 1	Masks the Tx Queue 1 Done interrupt. This interrupt asserts when Tx Queue 1 has transmitted a packet.	0x0

Bits	Type	Name	Description	Initial Value
3	RW	TX_DONE_INT_MSK 0	Masks the Tx Queue 0 Done interrupt. This interrupt asserts when Tx Queue 0 has transmitted a packet.	0x0
2	RW	RX_DONE_INT_MSK	Masks the Rx Done interrupt. This interrupt asserts a packet is received.	0x0
1	RW	TX_DLY_INT_MSK	Masks the Tx Delay interrupt. This interrupt asserts when the number of delayed Tx interrupts has reached a specified level, or when the delay time is reached.	0x0
0	RW	RX_DLY_INT_MSK	Masks the Rx Delay interrupt. This interrupt asserts when the number of delayed Rx interrupts has reached a specified level, or when the delay time is reached.	0x0

NOTE: Where applicable,

0: Disable

1: Enable

0: Not masked

1: Masked

449. WPDMA_GLO_CFG: (offset: 0x0208)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RW	HDR_SEG_LEN	Header Segment Length 0: Disable header/payload scattering. Not 0: Specify the header segment size in bytes to support the Rx header/payload scattering function.	0x0
8	RW	DESC_32B	32 Byte Descriptor Enables support for 32-byte PDMA descriptors. 0: Disable 1: Enable	0x0
7	RW	BIG_ENDIAN	Selects the endian mode. DMA applies the endian rule to convert payload and Tx/Rx information. DMA does not apply endian rule to register or descriptor. 0: Little endian 1: Big endian	0x0
6	RW	TX_WB_DDONE	Tx Writeback DDONE Enables writes of the DDONE bit to the TXD by the TX_DMA. 0: Disable 1: Enable	0x1
5:4	RW	WPDMA_BT_SIZE	WPDMA Burst Size Defines the burst size of WPDMA. 0: 4 DWORD (16 bytes) 1: 8 DWORD (32 bytes) 2: 16 DWORD (64 bytes) 3: 32 DWORD (128 bytes)	0x2

Bits	Type	Name	Description	Initial Value
3	RO	RX_DMA_BUSY	Rx DMA Busy Indicates the busy status of the Rx DMA. 0: Not busy. 1: Busy.	0x0
2	RW	RX_DMA_EN	Rx DMA Enable Enables the Rx DMA. When disabled, RX_DMA finishes processing the current received packet, then stops. 0: Disable 1: Enable	0x0
1	RO	TX_DMA_BUSY	Tx DMA Busy Indicates the busy status of the Tx DMA. 0: Not busy. 1: Busy.	0x0
0	RW	TX_DMA_EN	Tx DMA Enable Enables the Tx DMA. When disabled, TX_DMA finishes sending the current packet, then stops. 0: Disable 1: Enable	0x0

450. WPDMA_RST_IDX: (offset: 0x020C)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
16	W1C	RST_DRX_IDX0	Reset RX_DMARX_IDX0 Resets index 0 of the Rx link table to 0.	0x0
15:6	-	-	Reserved	0x0
5	W1C	RST_DTX_IDX3	Reset TX_DMATX_IDX5 Resets index 5 of the Tx link table to 0.	0x0
4	W1C	RST_DTX_IDX2	Reset TX_DMATX_IDX4 Resets index 4 of the Tx link table to 0.	0x0
3	W1C	RST_DTX_IDX3	Reset TX_DMATX_IDX3 Resets index 3 of the Tx link table to 0.	0x0
2	W1C	RST_DTX_IDX2	Reset TX_DMATX_IDX2 Resets index 2 of the Tx link table to 0.	0x0
1	W1C	RST_DTX_IDX1	Reset TX_DMATX_IDX1 Resets index 1 of the Tx link table to 0.	0x0
0	W1C	RST_DTX_IDX0	Reset TX_DMATX_IDX0 Resets index 0 of the Tx link table to 0.	0x0

NOTE:

0: Disassert reset
1: Reset

451. DELAY_INT_CFG: (offset: 0x0210)

Bits	Type	Name	Description	Initial Value
31	RW	TXDLY_INT_EN	Tx Delay Interrupt Enable Enables the Tx delayed interrupt mechanism. 0: Disable 1: Enable	0x0
30:24	RW	TXMAX_PINT	Tx Maximum Pending Interrupts Sets the maximum pended interrupts. When the number of pended interrupts is equal to or greater than the value specified here or interrupt pending time has reached the limit (see below), a final TX_DLY_INT is generated. 0: Disables the pending interrupt count check.	0x0
23:16	RW	TXMAX_PTIME	Tx Maximum Pending Time Reads or sets the maximum pending time for the internal TX_DONE_INT0-5. When the pending time is equal to or greater than TXMAX_PTIME x 20 μ s or the number of pended TX_DONE_INT0-5 is equal to or greater than TXMAX_PINT (see above), a final TX_DLY_INT is generated. 0: Disables the pending interrupt time check.	0x0
15	RW	RXDLY_INT_EN	Rx Delay Interrupt Enable Enables the Rx delayed interrupt mechanism. 0: Disable 1: Enable	0x0
14:8	RW	RXMAX_PINT	Rx Maximum Pended Interrupts Sets the maximum pended interrupts. When the number of pended interrupts is equal to or greater than the value specified here or interrupt pending time reach the limit (see below), a final RX_DLY_INT is generated. 0: Disables the pending interrupt count check.	0x0
7:0	RW	RXMAX_PTIME	Rx Maximum Pending Time Sets the maximum pending time for the internal RX_DONE_INT. When the pending time is equal to or greater than RXMAX_PTIME x 20 μ s, or the number of pended RX_DONE_INT is equal to or greater than RXMAX_PCNT (see above), a final RX_DLY_INT is generated. 0: Disables the pending interrupt time check.	0x0

452. WMM_AIFSN_CFG: (offset: 0x0214)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:12	RW	AIFSN3	AIFSN for Access Category 3 The arbitration inter-frame spacing number which specifies the channel idle period after which a back-off occurs in AC3. (unit: slot time)	0x0
11:8	RW	AIFSN2	AIFSN for Access Category 2 The arbitration inter-frame spacing number which specifies the channel idle period after which a back-off occurs in AC2. (unit: slot time)	0x0
7:4	RW	AIFSN1	AIFSN for Access Category 1 The arbitration inter-frame spacing number which specifies the channel idle period after which a back-off occurs in AC1. (unit: slot time)	0x0
3:0	RW	AIFSN0	AIFSN for Access Category 0 The arbitration inter-frame spacing number which specifies the channel idle period after which a back-off occurs in AC0. (unit: slot time)	0x0

453. WMM_CWMIN_CFG: (offset: 0x0218)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:12	RW	CW_MIN3	CWmin for Access Category 3 The minimum contention window from which the back-off timer value is derived in AC3. $AC3\ CWmin = 2^{CW_MIN3}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0
11:8	RW	CW_MIN2	CWmin for Access Category 2 The minimum contention window from which the back-off timer value is derived in AC2. $AC2\ CWmin = 2^{CW_MIN2}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0

Bits	Type	Name	Description	Initial Value
7:4	RW	CW_MIN1	CWmin for Access Category 1 The minimum contention window from which the back-off timer value is derived in AC1. $AC1\ CWmin = 2^{CW_MIN1}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0
3:0	RW	CW_MIN0	CWmin for Access Category 0 The minimum contention window from which the back-off timer value is derived in AC0. $AC0\ CWmin = 2^{CW_MIN0}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0

454. WMM_CWMAX_CFG: (offset: 0x021C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:12	RW	CW_MAX3	CWmax for Access Category 3 The maximum contention window which specifies the maximum value for the back-off timer in AC3. $AC3\ CWmax = 2^{CW_MAX3}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0
11:8	RW	CW_MAX2	CWmax for Access Category 2 The maximum contention window which specifies maximum value for the back-off timer in AC2. $AC2\ CWmax = 2^{CW_MAX2}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0
7:4	RW	CW_MAX1	CWmax for Access Category 1 The maximum contention window which specifies maximum value for the back-off timer in AC1. $AC1\ CWmax = 2^{CW_MAX1}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0

Bits	Type	Name	Description	Initial Value
3:0	RW	CW_MAX0	CWmax for Access Category 0 The maximum contention window which specifies maximum value for the back-off timer in AC0. $AC0\ CW_{max} = 2^{CW_MAX0}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x0

455. WMM_TXOP0_CFG: (offset: 0x0220)

Bits	Type	Name	Description	Initial Value
31:16	RW	TXOP1	TXOP for Access Category 1 The transmit opportunity which specifies the interval in which a station may transmit in AC1. (unit: μ s)	0x0
15:0	RW	TXOP0	TXOP for Access Category 0 The transmit opportunity which specifies the interval in which a station may transmit in AC0. (unit: μ s)	0x0

456. WMM_TXOP1_CFG: (offset: 0x0224)

Bits	Type	Name	Description	Initial Value
31:16	RW	TXOP3	TXOP for Access Category 3 The transmit opportunity which specifies the interval in which a station may transmit in AC3. (unit: μ s)	0x0
15:0	RW	TXOP2	TXOP for Access Category 2 The transmit opportunity which specifies the interval in which a station may transmit in AC2. (unit: μ s)	0x0

457. TX_BASE_PTR_n: (offset: 0x0230, 0x0240, 0x0250, 0x0260, 0x0270, 0x0280) (n: 0 to 5)

Bits	Type	Name	Description	Initial Value
31:0	RW	TX_BASE_PTRn	Tx Base Pointer n Points to the base address of TX_Ring n (4-DWORD aligned address)	0x0

458. TX_MAX_CNT_n: (offset: 0x0234, 0x0244, 0x0254, 0x0264, 0x0274, 0x0284) (n: 0 to 5)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:0	RW	TX_MAX_CNTn	Tx Maximum TXD Count n Sets the maximum TXD count in TXD_Ring n.	0x0

459. TX_CTX_IDX_n: (offset: 0x0238, 0x0248, 0x0258, 0x0268, 0x0278, 0x0288) (n: 0 to 5)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:0	RW	TX_CTX_IDXn	Tx CPU TXD Index n Points to the next TXD to be used by the CPU.	0x0

460. TX_DTX_IDX_n: (offset: 0x023C, 0x024C, 0x025C, 0x026C, 0x027C, 0x028C) (n: 0 to 5)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:0	RO	TX_DTX_IDXn	Tx DMA TXD Index n Points to the next TXD to be used by the DMA.	0x0

461. RX_BASE_PTR: (offset: 0x0290)

Bits	Type	Name	Description	Initial Value
31:0	RW	RX_BASE_PTR0	Rx Base Pointer 0 Points to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address.	0x0

462. RX_MAX_CNT: (offset: 0x0294)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:0	RW	RX_MAX_CNT0	Rx Maximum Count 0 Sets the maximum number of RXD in RXD_Ring n.	0x0

463. RX_CALC_IDX: (offset: 0x0298)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:0	RW	RX_CALC_IDX0	Rx CPU RXD Index 0 Points to the next RXD that the CPU will allocate to Rx Ring n.	0x0

464. FS_DRX_IDX: (offset: 0x029C)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:0	RW	RX_DRX_IDX0	Rx DMA RXD Index 0 Points to the next RXD that the DMA will use in FDS Ring n. It should be a 4-DWORD aligned address.	0x0

465. US_CYC_CNT: (offset: 0x02A4)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24	RW	TEST_EN	Enables test mode. 0: Disable 1: Enable	0x0
23:16	RW	TEST_SEL	Selects test mode.	0xf0
15:9	-	-	Reserved	0x0
8	RW	BT_MODE_EN	Enables Bluetooth mode. 0: Disable 1: Enable	0x0
7:0	RW	US_CYC_CNT	Sets the clock cycle count. The setting depends on the interface clock rate. If the system clock rate = 125 Mhz, set 8'h7D. If the system clock rate = 133 Mhz, set 8'h85. (unit: 1 μ s) 8'h21: PCI 33 8'h7D: PCI express 8'h1E: USB	0x21

2.22.5 PBF Registers (base: 0x1018_0000)

2.22.5.1 List of Registers

No.	Offset	Register Name	Description	Page
466	0x0400	SYS_CTRL	System Control	383
467	0x0404	HOST_CMD	Host Command	384
468	0x0408	PBF_CFG	Packet Buffer Configuration	384
469	0x040C	MAX_PCNT	Maximum Packet Count	385
470	0x0410	BUF_CTRL	Buffer Control	385
471	0x0414	MCU_INT_STA	Master Control Unit Interrupt Status	386
472	0x0418	MCU_INT_ENA	Master Control Unit Interrupt Enable	387
473	0x041C	TX0Q_IO	Transmit Queue 0 Input/Output	389
474	0x0420	TX1Q_IO	Transmit Queue 1 Input/Output	389
475	0x0424	TX2Q_IO	Transmit Queue 2 Input/Output	389
476	0x0428	RX0Q_IO	Receive Queue 0 Input/Output	389
477	0x042C	BCN_OFFSET0	Beacon Offset 0	390
478	0x0430	BCN_OFFSET1	Beacon Offset 1	390
479	0x0434	TXRXQ_STA	Transmit/Receive Queue Station	390
480	0x0438	TXRXQ_PCNT	Transmit/Receive Queue Packet Count	391
481	0x043C	PBF_DBG	Packet Buffer Debug	391
482	0x0440	CAP_CTRL	Capture Control	391

2.22.5.2 Register Descriptions

466. SYS_CTRL: (offset: 0x0400)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RW	SHR_MSEL	Shared Memory Select Sets access to shared memory. 0: Map address 0x4000 – 0x7FFF to the lower 16 KB of shared memory. 1: Map address 0x4000 – 0x5FFF to the higher 4 KB of shared memory.	0x0
18:17	RW	PBF_MSEL	Packet Buffer Memory Select Sets access to packet buffer memory. 00: Map address 0x8000 – 0xFFFF to the first 32 KB of packet buffer. 01: Map address 0x8000 – 0xFFFF to second 32 KB of packet buffer. 10: Maps address 0x8000 – 0xFFFF to the third 32 KB of the packet buffer.	0x0
16	RW	HST_PM_SEL	Host Program Memory Select Sets whether the host can write to the MCU program memory. 0: Program memory is used by MCU and the host cannot write to the memory. 1: Stops on-chip MCU and writes to the program memory. MCU is reset if this register is set to 1.	0x0
15	-	-	Reserved	0x0
14	RW	CAP_MODE	Capture Mode Sets the packet buffer capture mode. 0: Normal mode. 1: BBP capture mode.	0x0
13	-	-	Reserved	0x1
12	RW	CLKSELECT	Clock Select Sets the MAC/PBF clock source. 0: From PLL 1: From 40 MHz clock input	0x0
11	RW	PBF_CLKEN	Enables the PBF clock.	0x0
10	RW	MAC_CLK_EN	Enables the MAC clock.	0x0
9	RW	DMA_CLK_EN	Enables the DMA clock.	0x0
8	-	-	Reserved	0x0
7	RW	MCU_READY	Indicates MCU is ready. 8051 writes 1 to this bit to inform the host the internal MCU is ready.	0x0
6:5	-	-	Reserved	0x0
4	RW	ASY_RESET	Resets the ASYNC interface.	0x0

Bits	Type	Name	Description	Initial Value
3	RW	PBF_RESET	Resets the PBF hardware.	0x0
2	RW	MAC_RESET	Resets the MAC hardware.	0x0
1	RW	DMA_RESET	Resets the DMA hardware.	0x0
0	W1C	MCU_RESET	Resets the MCU hardware. This bit is auto-cleared after several clock cycles.	0x0

NOTE: Where applicable,

0: Disable

1: Enable

0: Disassert reset

1: Reset

467. HOST_CMD: (offset: 0x0404)

Bits	Type	Name	Description	Initial Value
31:0	RW	HST_CMD	Host command code Host writing to this register triggers an interrupt to 8051.	0x0

468. PBF_CFG: (offset: 0x0408)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:21	RW	TX1Q_NUM	Queue depth of Tx1Q. The maximum packet number is 7.	0x7
20:16	RW	TX2Q_NUM	Queue depth of Tx2Q. The maximum packet number is 20.	0x14
15	RW	NULL0_MODE	HCCA NULL0 Frame Auto Mode Enables HCCA NULL0 Frame Auto mode. In this mode, a NULL0 frame is automatically transmitted if TXQ1 is enabled but empty. After the NULL0 frame is transmitted, TXQ1 is disabled.	0x0
14	RW	NULL1_MODE	HCCA NULL1 Frame Auto Mode Enables HCCA NULL1 Frame Auto mode. In this mode, all TXQ (0/1/2) are disabled after a NULL1 frame is transmitted.	0x0
13	RW	RX_DROP_MODE	Rx Drop Mode Sets PBF to drop Rx packets before they enter the DMA. 0: Normal mode 1: Drop mode	0x0
12	RW	TX0Q_MODE	Tx0Q Operation Mode 0: Auto mode 1: Manual mode	0x0
11	RW	TX1Q_MODE	Tx1Q Operation Mode 0: Auto mode 1: Manual mode	0x0

Bits	Type	Name	Description	Initial Value
10	RW	TX2Q_MODE	Tx2Q Operation Mode 0: Auto mode 1: Manual mode	0x0
9	RW	RX0Q_MODE	Rx0Q Operation Mode 0: Auto mode 1: Manual mode	0x0
8	RW	HCCA_MODE	HCCA Auto Mode Enables HCCA Auto mode. In this mode, TXQ1 is enabled when CF-POLL arrives.	0x0
7:5	-	-	Reserved	0x0
4	RW	TX0Q_EN	Enables Tx0Q.	0x1
3	RW	TX1Q_EN	Enables Tx1Q.	0x0
2	RW	TX2Q_EN	Enables Tx2Q.	0x1
1	RW	RX0Q_EN	Enables Rx0Q.	0x1
0	-	-	Reserved	0x0

NOTE: where applicable,
0: Disable
1: Enable

469. MAX_PCNT: (offset: 0x040C)

Bits	Type	Name	Description	Initial Value
31:24	RW	MAX_TX0Q_PCNT	The maximum buffer page count for Tx0Q.	0x1f
23:16	RW	MAX_TX1Q_PCNT	The maximum buffer page count for Tx1Q.	0x3f
15:8	RW	MAX_TX2Q_PCNT	The maximum buffer page count for Tx2Q.	0x9f
7:0	RW	MAX_RX0Q_PCNT	The maximum buffer page count for Rx0Q.	0x9f

470. BUF_CTRL: (offset: 0x0410)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11	W1C	WRITE_TX0Q	Manually writes to Tx0Q.	0x0
10	W1C	WRITE_TX1Q	Manually writes to Tx1Q.	0x0
9	W1C	WRITE_TX2Q	Manually writes to Tx2Q	0x0
8	W1C	WRITE_RX0Q	Manually writes to Rx0Q	0x0
7	W1C	NULL0_KICK	Kicks out NULL0 frame. This bit is cleared after the NULL0 frame is transmitted.	0x0
6	W1C	NULL1_KICK	Kicks out NULL1 frame. This bit is cleared after the NULL1 frame is transmitted.	0x0
5	W1C	BUF_RESET	Resets the buffer. 0: Disassert reset 1: Reset	0x0
4	-	-	Reserved	0x0
3	W1C	READ_TX0Q	Manually reads Tx0Q.	0x0

Bits	Type	Name	Description	Initial Value
2	W1C	READ_TX1Q	Manually reads Tx1Q.	0x0
1	W1C	READ_TX2Q	Manually reads Tx2Q.	0x0
0	W1C	READ_RX0Q	Manually reads Rx0Q.	0x0

471. MCU_INT_STA: (offset: 0x0414)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	MAC_INT_11	MAC interrupt 11: Reserved	0x0
26	RW	MAC_INT_10	MAC interrupt 10: Reserved	0x0
25	RW	MAC_INT_9	MAC interrupt 9: Reserved	0x0
24	RW	MAC_INT_8	MAC interrupt 8: Rx QoS CF-Poll interrupt Asserts after receiving a QoS Data (+) CF-Poll frame.	0x0
23	RW	MAC_INT_7	MAC interrupt 7: TXOP early termination interrupt. Asserts if Tx finishes before TXOP time is complete.	0x0
22	RW	MAC_INT_6	MAC interrupt 6: TXOP early timeout interrupt. Asserts if TXOP times out before Tx is complete.	0x0
21	RW	MAC_INT_5	MAC interrupt 5: Reserved	0x0
20	RW	MAC_INT_4	MAC Interrupt 4: General Purpose (GP) Timer Interrupt Asserts when the GP timer has timed out. Configure this timer using the INT_TIMER_CFG register.	0x0
19	RW	MAC_INT_3	MAC Interrupt 3: Auto-Wakeup Interrupt Asserts when the auto-wakeup function has been triggered. Configure this interrupt using the AUTO_WAKEUP_CFG register.	0x0
18	RW	MAC_INT_2	MAC Interrupt 2: Tx Status Interrupt Asserts when the status of the Tx queue becomes valid.	0x0
17	RW	MAC_INT_1	MAC interrupt 1: Pre-TBTT interrupt Asserts at an interval before the TBTT interrupt is triggered. Configure this timer using the INT_TIMER_CFG register.	0x0
16	RW	MAC_INT_0	MAC Interrupt 0: TBTT Interrupt Asserts when the TBTT timer has counted down to zero. Configure this timer using the TBTT_TIMER register.	0x0
15	-	-	Reserved	0x0
14	RW	RX_SD_INT	RF Rx Signal Detection Interrupt Asserts when the RF detects a signal.	0x0
13:12	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
11	RW	DTX0_INT	DMA Tx Queue 0 Interrupt Asserts when frame transfer from the DMA to TX0Q is complete.	0x0
10	RW	DTX1_INT	DMA Tx Queue1 Interrupt Asserts when frame transfer from the DMA to TX1Q is complete.	0x0
9	RW	DTX2_INT	DMA Tx Queue2 Interrupt Asserts when frame transfer from the DMA to TX2Q is complete.	0x0
8	RW	DRX0_INT	DMA Rx Queue 0 Interrupt Asserts when frame transfer from the RX0Q to DMA is complete.	0x0
7	RW	HCMD_INT	Host Command Interrupt Asserts when the Host writes to the HOST_CMD register.	0x0
6	RW	NOTX_INT	Null0 Frame Tx Interrupt Asserts when NULL0 frame Tx is complete.	0x0
5	RW	N1TX_INT	Null1 Frame Tx Interrupt Asserts when NULL1 frame Tx is complete.	0x0
4	RW	BCNTX_INT	Beacon Frame Tx Interrupt Asserts when Beacon frame Tx is complete.	0x0
3	RW	MTX0_INT	Tx Queue 0 MAC Interrupt Asserts when frame transfer from the TX0Q to the MAC is complete.	0x0
2	RW	MTX1_INT	Tx Queue 1 MAC Interrupt Asserts when frame transfer from the TX1Q to the MAC is complete.	0x0
1	RW	MTX2_INT	Tx Queue 2 MAC Interrupt Asserts when frame transfer from the TX2Q to the MAC is complete.	0x0
0	RW	MRX0_INT	Rx Queue 0 MAC Interrupt Asserts when frame transfer from the MAC to RX0Q is complete.	0x0

NOTE: This register is only for 8051

Read

0: Interrupt not asserted.

1: Interrupt asserted

Write

1: Clear the interrupt

472. MCU_INT_ENA: (offset: 0x0418)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27	RW	MAC_INT11_EN	Enables MAC interrupt 11: Reserved	0x0
26	RW	MAC_INT10_EN	Enables MAC interrupt 10: Reserved	0x0
25	RW	MAC_INT9_EN	Enables MAC interrupt 9: Reserved	0x0

Bits	Type	Name	Description	Initial Value
24	RW	MAC_INT8_EN	Enables MAC Interrupt 8: Rx QoS CF-Poll Interrupt. This interrupt asserts after receiving a QoS Data (+) CF-Poll frame.	0x0
23	RW	MAC_INT7_EN	Enables MAC interrupt 7.	0x0
22	RW	MAC_INT6_EN	Enables MAC interrupt 6.	0x0
21	RW	MAC_INT5_EN	Enables MAC interrupt 5.	0x0
20	RW	MAC_INT4_EN	Enables MAC Interrupt 4: GP Timer Interrupt. This interrupt asserts when the general purpose timer has timed out. Configure this timer using the INT_TIMER_CFG register.	0x0
19	RW	MAC_INT3_EN	Enables MAC Interrupt 3: Auto-Wakeup Interrupt. This interrupt asserts when the auto-wakeup function has been triggered. Configure this interrupt using the AUTO_WAKEUP_CFG register.	0x0
18	RW	MAC_INT2_EN	Enables MAC Interrupt 2: Tx Status Interrupt. This interrupt asserts when the status of the Tx queue becomes valid.	0x0
17	RW	MAC_INT1_EN	Enables MAC Interrupt 1: Pre-TBTT Interrupt. This interrupt asserts at an interval before the TBTT interrupt is triggered. Configure this timer using the INT_TIMER_CFG register.	0x0
16	RW	MAC_INT0_EN	Enables MAC Interrupt 0: TBTT Interrupt. This interrupt asserts depending on the configuration of the TBTT timer. Configure this interrupt using the TBTT_TIMER register.	0x0
15:12	-	-	Reserved	0x0
11	RW	DTX0_INT_EN	Enables the DMA Tx Queue 0 Interrupt. This interrupt asserts when frame transfer from the TX0Q to DMA is complete.	0x0
10	RW	DTX1_INT_EN	Enables the DMA Tx Queue 1 Interrupt. This interrupt asserts when frame transfer from the TX1Q to DMA is complete.	0x0
9	RW	DTX2_INT_EN	Enables the DMA Tx Queue 2 Interrupt. This interrupt asserts when frame transfer from the TX2Q to DMA is complete.	0x0
8	RW	DRX0_INT_EN	Enables the DMA Rx Queue 0 Interrupt. This interrupt asserts when frame transfer from the RX0Q to DMA is complete.	0x0
7	RW	HCMD_INT_EN	Enables the Host Command Interrupt. This interrupt asserts when the Host writes to the HOST_CMD register.	0x0
6	RW	NOTX_INT_EN	Enables the Null 0 Frame Tx Interrupt. This interrupt asserts when NULL0 frame Tx is complete.	0x0

Bits	Type	Name	Description	Initial Value
5	RW	N1TX_INT_EN	Enables the Null 1 Frame Tx Interrupt. This interrupt asserts when NULL1 frame Tx is complete.	0x0
4	RW	BCNTX_INT_EN	Enables the Beacon Frame Tx Interrupt. This interrupt asserts when Beacon frame Tx is complete.	0x0
3	RW	MTX0_INT_EN	Enables the Tx Queue 0 MAC Interrupt. This interrupt asserts when frame transfer from the TX0Q to the MAC is complete.	0x0
2	RW	MTX1_INT_EN	Enables the Tx Queue 1 MAC Interrupt. This interrupt asserts when frame transfer from the TX1Q to the MAC is complete.	0x0
1	RW	MTX2_INT_EN	Enables the Tx Queue 2 MAC Interrupt. This interrupt asserts when frame transfer from the TX2Q to the MAC is complete.	0x0
0	RW	MRX0_INT_EN	Enables the Rx Queue 0 MAC Interrupt. This interrupt asserts when frame transfer from the MAC to RX0Q is complete.	0x0

NOTE: This register is only for 8051

0: Disable

1: Enable

473. TX0Q_IO: (offset: 0x041C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	TX0Q_IO	TX0Q IO port. This register is used in manual mode.	0x0

474. TX1Q_IO: (offset: 0x0420)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	TX1Q_IO	TX1Q IO port. This register is used in manual mode.	0x0

475. TX2Q_IO: (offset: 0x0424)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RW	TX2Q_IO	TX2Q IO port. This register is used in manual mode.	0x0

476. RX0Q_IO: (offset: 0x0428)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
15:0	RW	RX0Q_IO	RX0Q IO port. This register is used in manual mode.	0x0

477. BCN_OFFSET0: (offset: 0x042C)

Bits	Type	Name	Description	Initial Value
31:24	RW	BCN3_OFFSET	Beacon 3 address offset in shared memory. (unit: 64 bytes)	0xec
23:16	RW	BCN2_OFFSET	Beacon 2 address offset in shared memory. (unit: 64 bytes)	0xe8
15:8	RW	BCN1_OFFSET	Beacon 1 address offset in shared memory. (unit: 64 bytes)	0xe4
7:0	RW	BCN0_OFFSET	Beacon 0 address offset in shared memory. (unit: 64 bytes)	0xe0

NOTE: There are two beacon frame buffers on this chip. They are located at 0x4000 - 0x4FFF (SHR_MSEL = 1) and 0x6000 - 0x7FFF (SHR_MSEL = 0).

The physical address of beacon frame is calculated by:

If OFFSET < 0x40

Set SHR_MSEL = 1 (SYS_CTRL[19] = 1)

Beacon frame starting address = OFFSET * 64 + 0x4000 (0x4000 - 0x4FFF)

Else if OFFSET >= 0x80

Set SHR_MSEL = 0 (SYS_CTRL[19] = 0)

Beacon frame starting address = OFFSET * 64 + 0x4000 (0x6000 - 0x7FFF)

Else

This address cannot be the beacon buffer.

478. BCN_OFFSET1: (offset: 0x0430)

Bits	Type	Name	Description	Initial Value
31:24	RW	BCN7_OFFSET	Beacon 7 address offset in shared memory. (unit: 64 bytes)	0xFC
23:16	RW	BCN6_OFFSET	Beacon 6 address offset in shared memory. (unit: 64 bytes)	0xF8
15:8	RW	BCN5_OFFSET	Beacon 5 address offset in shared memory. (unit: 64 bytes)	0xF4
7:0	RW	BCN4_OFFSET	Beacon 4 address offset in shared memory. (unit: 64 bytes)	0xf0

479. TXRXQ_STA: (offset: 0x0434)

Bits	Type	Name	Description	Initial Value
31:24	RO	RX0Q_STA	Indicates the status of RxQ.	0x22
23:16	RO	TX2Q_STA	Indicates the status of Tx2Q.	0x2
15:8	RO	TX1Q_STA	Indicates the status of Tx1Q.	0x2
7:0	RO	TX0Q_STA	Indicates the status of Tx0Q.	0x2

NOTE:

Bits [7:4] indicate the IN queue is full, empty or has an error.

Bits [3:0] indicate the OUT queue is full, empty or has an error.

480. TXRXQ_PCNT: (offset: 0x0438)

Bits	Type	Name	Description	Initial Value
31:24	RO	RX0Q_PCNT	Page count in RxQ	0x0
23:16	RO	TX2Q_PCNT	Page count in Tx2Q	0x0
15:8	RO	TX1Q_PCNT	Page count in Tx1Q	0x0
7:0	RO	TX0Q_PCNT	Page count in Tx0Q	0x0

481. PBF_DBG: (offset: 0x043C)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RO	FREE_PCNT	Free page count	0xFE

482. CAP_CTRL: (offset: 0x0440)

Bits	Type	Name	Description	Initial Value
31	RW	CAP_ADC_FEQ	Selects the source for data capture. 0: Data from the ADC output 1: Data from the FEQ output	0x0
30	WC	CAP_START	Starts data capture. 0: No action 1: Start data capture (cleared automatically after capture finished)	0x0
29	W1C	MAN_TRIG	Manual capture trigger	0x0
28:16	RW	TRIG_OFFSET	Starting address offset before trigger point.	0x140
15:13	-	-	Reserved	0x0
12:0	RO	START_ADDR	Starting address of captured data.	0x0

2.22.6 RF TEST Registers (base: 0x1018_0000)

2.22.6.1 List of Registers

No.	Offset	Register Name	Description	Page
483	0x0500	RF_CFG	Radio Frequency (RF) Configuration	392
484	0x0504 to 0x0560	Reserved	-	392

2.22.6.2 Register Descriptions

483. RF_CFG: (offset: 0x0500)

Bits	Type	Name	Description	Initial Value
31:26	-	-	Reserved	0x0
25:16	RW	TESTCSR_RFACC _REGNUM	RF register ID Bits [25:22] contains 4 bits which indicate the bank number. Bits [21:16] contain 6 bits which indicate the register number.	0x0
15:8	RW	RF_CSR_DATA	RF Control Status Register Data <i>Write:</i> Data to be written to the RF. <i>Read:</i> Data read back from the RF.	0x0
7:5	-	-	Reserved	0x0
4	RW	RF_CSR_WR	RF Control Status Register Write Sets this register to read or write to the RF register. 0: Read 1: Write	0x0
3:1	-	-	Reserved	0x0
0	WC	RF_CSR_KICK	RF Control Status Register Kick Read this bit to find the status of RF read/write operations, or write to this bit to start read/writes to the RF register. <i>Read:</i> 0: Read/writes done 1: Busy <i>Write:</i> 1: Start read/writes	0x0

484. Reserved: (offset: 0x0504 to 0x0560)

2.22.7 MAC Registers (base: 0x1018_0000)

2.22.7.1 List of Registers

No.	Offset	Register Name	Description	Page
485	0x1000	ASIC_VER_ID	ASIC Verification ID	394
486	0x1004	MAC_SYS_CTRL	MAC System Control	394
487	0x1008	MAC_ADDR_DW0	MAC Address DWORD 0	395
488	0x100C	MAC_ADDR_DW1	MAC Address DWORD 1	395
489	0x1010	MAC_BSSID_DW0	MAC Base Station ID DWORD 0	395
490	0x1014	MAC_BSSID_DW1	MAC Base Station ID DWORD 1	396
491	0x1018	MAX_LEN_CFG	Maximum Length Configuration	398
492	0x101C	BBP_CSR_CFG	Baseband Control Status Register Configuration	398
493	0x1020	RF_CSR_CFG0	RF Control Status Register Configuration 0	399
494	0x1024	RF_CSR_CFG1	RF Control Status Register Configuration 1	399
495	0x1028	RF_CSR_CFG2	RF Control Status Register Configuration 2	400
496	0x102C	LED_CFG	LED Configuration	400
497	0x1030	AMPDU_MAX_LEN_20M1S	A-MPDU Maximum Length Bandwidth 20 MHz Stream 1	401
498	0x1034	AMPDU_MAX_LEN_20M2S	A-MPDU Maximum Length Bandwidth 20 MHz Stream 2	401
499	0x1038	AMPDU_MAX_LEN_40M1S	A-MPDU Maximum Length Bandwidth 40 MHz Stream 1	402
500	0x103C	AMPDU_MAX_LEN_40M2S	A-MPDU Maximum Length Bandwidth 40 MHz Stream 2	402
501	0x1040	AMPDU_BA_WINSIZE	A-MPDU Block Acknowledgement Window Size	403
502	0x106C	TX_WCID_DROP_MASK0	Tx Wireless Client ID Drop Mask 0	403
...	...	...	...	...
509	0x1088	TX_WCID_DROP_MASK7	Tx Wireless Client ID Drop Mask 7	405
510	0x108C	TX_BCN_BYPASS_MASK	Tx Beacon Bypass Mask	405
511	0x1090	AP_CLIENT_BSSID0_L	AP Client Base Station ID 0 Low	405
512	0x1094	AP_CLIENT_BSSID0_H	AP Client Base Station ID 0 High	405
...	...	...	...	...
525	0x10C8	AP_CLIENT_BSSID7_L	AP Client Base Station ID 0 Low	407
526	0x10CC	AP_CLIENT_BSSID7_H	AP Client Base Station ID 0 High	408
527	0x10D0	BT_WINDOW_CFG	Bluetooth Window Configuration	408
528	0x10D4	BT_COEX_CFG	Bluetooth Coexistence Configuration	408

2.22.7.2 Register Descriptions

485. ASIC_VER_ID: (offset: 0x1000)

Bits	Type	Name	Description	Initial Value
31:16	RO	VER_ID	ASIC version ID	0x5390
15:0	-	-	Reserved	0x0

486. MAC_SYS_CTRL: (offset: 0x1004)

Bits	Type	Name	Description	Initial Value
31:15	-	-	Reserved	0x0
14:12	RW	WLAN_ACT_MASK	Masks WLAN activity. Bit[12]: Tx is reported as WLAN active. Bit[13]: Rx is reported as WLAN active. Bit[14]: SIFS is reported as WLAN active.	0x7
11:8	RW	BT_HALT_WLAN_EN	Bluetooth Halt WLAN Enable Allows Bluetooth to halt WLAN activity. Bit[8]: BT halts WLAN when {LNA_PE_G1, GPIO0}=2'b00. Bit[9]: BT halts WLAN when {LNA_PE_G1, GPIO0}=2'b01. Bit[10]: BT halts WLAN when {LNA_PE_G1, GPIO0}=2'b10. Bit[11]: BT halts WLAN when {LNA_PE_G1, GPIO0}=2'b11.	0x0
7	RW	RX_TS_EN	Rx Timestamp Enable Writes a 32-bit hardware Rx timestamp instead of (RXWI->RSSI), and writes (RXWI->RSSI) instead of (RXWI->SNR). NOTE: For QA Rx sniffer mode only.	0x0
6	RW	WLAN_HALT_EN	WLAN Halt Enable Enables an external WLAN halt control signal.	0x0
5	RW	PBF_LOOP_EN	Packet Buffer Loopback Enable Enables packet buffer loopback. (Tx->Rx).	0x0
4	RW	CONT_TX_TEST	Continuous Tx Test Enables continuous Tx production test, and overrides MAC_RX_EN and MAC_TX_EN.	0x0
3	RW	MAC_RX_EN	Enables MAC Rx.	0x0
2	RW	MAC_TX_EN	Enables MAC Tx.	0x0
1	RW	BBP_HRST	BBP Hard-Reset 0: BBP in normal state 1: BBP in reset state NOTE: The whole BBP including BBP registers will be reset.	0x1

Bits	Type	Name	Description	Initial Value
0	RW	MAC_SRST	MAC Soft-Reset 0: MAC in normal state 1: MAC in reset state NOTE: 1. MAC registers and tables are NOT reset. 2. MAC hard-reset is outside the scope of MAC registers.	0x1

NOTE: Where applicable,
0: Disable
1: Enable

487. MAC_ADDR_DW0: (offset: 0x1008)

Bits	Type	Name	Description	Initial Value
31:24	RW	MAC_ADDR_3	MAC address byte3	0x0
23:16	RW	MAC_ADDR_2	MAC address byte2	0x0
15:8	RW	MAC_ADDR_1	MAC address byte1	0x0
7:0	RW	MAC_ADDR_0	MAC address byte0	0x0

488. MAC_ADDR_DW1: (offset: 0x100C)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RW	MAC_ADDR_5	MAC address byte5	0x0
7:0	RW	MAC_ADDR_4	MAC address byte4	0x0

NOTE: Byte0 is the first byte on network. Its LSB bit is the first bit on the network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

489. MAC_BSSID_DW0: (offset: 0x1010)

Bits	Type	Name	Description	Initial Value
31:24	RW	BSSID_3	BSSID byte3	0x0
23:16	RW	BSSID_2	BSSID byte2	0x0
15:8	RW	BSSID_1	BSSID byte1	0x0
7:0	RW	BSSID_0	BSSID byte0	0x0

490. MAC_BSSID_DW1: (offset: 0x1014)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26:24	RW	MULTI_BSSID_BYTE_SEL	Multiple BSSID Index Byte Selection (only for New BSSID mode) 0: Use MAC address byte0.bit[5:2] as BSSID index 1: Use MAC address byte1.bit[3:0] as BSSID index 2: Use MAC address byte2.bit[3:0] as BSSID index 3: Use MAC address byte3.bit[3:0] as BSSID index 4: Use MAC address byte4.bit[3:0] as BSSID index 5: Use MAC address byte5.bit[3:0] as BSSID index	0x0
23	RW	MULTI_BCN_NUM_B3	Multiple BSSID Beacon Number (extension bit 3) Use together with MULTI_BCN_NUM: (MULTI_BCN_NUM_BIT3 * 8) + MULTI_BCN_NUM = total number of multiple BSSID Beacons. 0: One back-off Beacon 1-15: SIFS-burst Beacon count	0x0
22	RW	MULTI_BSSID_MODE_B2	Multiple BSSID Mode (extension bit 2) Use together with MULTI_BSSID_MODE: (MULTI_BSSID_MODE_BIT2 * 4) + MULTI_BSSID_MODE = 0: 1-BSSID mode 1: 2-BSSID mode 2: 4-BSSID mode 3: 8-BSSID mode 4: 16-BSSID mode 5-7: Undefined	0x0

Bits	Type	Name	Description	Initial Value
21	RW	NEW_MULTI_BSSID_MODE	New Multiple BSSID Mode 0: Disable. Use MAC address Byte5 to distinguish different BSSID. 1: Enable. Use MAC address Byte0.bit[5:0] as local administration bit for multiple BSSID addresses, as follows. New BSSID numbering rule: - Byte0.bit0 of the MAC address is a broadcast/multicast bit. - Byte0.bit1 of the MAC address is a local administration bit and should be set to 1 in extended multiple BSSIDs. - Byte0.bit[5:2] of the MAC address is the extended multiple BSSID index if 16-MBSS mode is set. NOTE: The following reserved-bit rules apply. - Byte0.bit[5:2] should be reserved as 0 in 16-MBSS mode. - Byte0.bit[4:2] should be reserved as 0 in 8-MBSS mode. - Byte0.bit[3:2] should be reserved as 0 in 4-MBSS mode. - Byte0.bit 2 should be reserved as 0 in 2-MBSS mode. For example: In 4-BSSID mode with the MAC address set to 00:0c:43:28:60:01, based on the new rule, the extended 3-BSSID is 02:0c:43:28:60:01, 06:0c:43:28:60:01, and 0a:0c:43:28:60:01.	0x0
20:18	RW	MULTI_BCN_NUM	Multiple Beacon Number Sets the number of BSSID Beacons transmitted in a Beacon interval. 0: One back-off Beacon 1-7: One back-off Beacon and the specified number of SIFS-burst Beacons.	0x0
17:16	RW	MULTI_BSSID_MODE	Multiple BSSID Mode In multiple-BSSID AP mode, BSSID is the same as MAC_ADDR, that is, this device owns multiple MAC_ADDR in this mode. The multiple MAC_ADDR/BSSID are distinguished by [bit2: bit0] of byte5. 0: 1-BSSID mode (BSS index = 0) 1: 2-BSSID mode (byte5.bit0 is the BSS index) 2: 4-BSSID mode (byte5.bit[1:0] is the BSS index) 3: 8-BSSID mode (byte5.bit[2:0] is the BSS index)	0x0
15:8	RW	BSSID_5	BSSID byte5	0x0

Bits	Type	Name	Description	Initial Value
7:0	RW	BSSID_4	BSSID byte4	0x0

NOTE: RXINFO bit17 is extension BSS_INDEX bit 3, it is used together with RXWI BSS_INDEX bit2:bit0 to represent 16 multiple BSS.

491. MAX_LEN_CFG: (offset: 0x1018)

Bits	Type	Name	Description	Initial Value
31:22	-	-	Reserved	0x0
21:20	RW	MAX_MPDU_LEN_EXT	Maximum MPDU Length Extension Use together with MAX_MPDU_LEN as MSB extension to represent a 14-bit maximum MPDU length.	0x0
19:16	RW	MIN_MPDU_LEN	Minimum MPDU Length MAC drops the MPDU if the length is less than this limitation. Applied only in MAC Rx. (unit: bytes)	0xA
15	-	-	Reserved	0x0
14:12	RW	MAX_PSDU_LEN	Maximum PSDU Length (power factor) 0: 2 ¹³ = 8 Kilobytes 1: 2 ¹⁴ = 16 Kilobytes 2: 2 ¹⁵ = 32 Kilobytes 3: 2 ¹⁶ = 64 Kilobytes 4: 2 ¹⁷ = 128 Kilobytes 5: 2 ¹⁸ = 256 Kilobytes 6: 2 ¹⁸ = 512 Kilobytes 7: 2 ¹⁸ = 1024 Kilobytes MAC will NOT generate A-MPDU with length greater than this limitation. Applied only in MAC TX.	0x0
11:0	RW	MAX_MPDU_LEN	Maximum MPDU Length MAC drops the MPDU if the length is greater than this limitation. Applied only in MAC Rx. (unit: bytes)	0xFFF

492. BBP_CSR_CFG: (offset: 0x101C)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RW	BBP_RW_MODE	BBP Register R/W Mode 0: Serial mode 1: Parallel mode	0x1
18	RW	BBP_PAR_DUR	BBP Register Parallel R/W Pulse Width 0: Pulse width = 62.5 ns 1: Pulse width = 112.5 ns NOTE: Please set BBP_PAR_DUR=1 in 802.11J mode.	0x0

Bits	Type	Name	Description	Initial Value
17	RW	BBP_CSR_KICK	Baseband Control Status Register Kick Read this bit to find the status of BBP read/write operations, or write to this bit to start read/writes to the BBP register. <i>Read:</i> 0: Read/writes done 1: Busy <i>Write:</i> 1: Start read/writes	0x0
16	RW	BBP_CSR_RW	Baseband Control Status Register Read/Write 0: Write 1: Read	0x0
15:8	RW	BBP_ADDR	BBP register ID 0: R0 1: R1, and so on.	0x0
7:0	RW	BBP_DATA	Baseband Data <i>Read:</i> Data to be read from BBP <i>Write:</i> Data to be written to BBP	0x0

493. RF_CSR_CFG0: (offset: 0x1020)

Bits	Type	Name	Description	Initial Value
31	RW	RF_REG_CTRL	RF Register Control Read this bit to find the status of the RF read/write operations. Write to this bit to start writing data from RF registers 0/1/2 to the RF block, or to start reads of the RF block. <i>Read:</i> 0: Read/writes done 1: Busy <i>Write:</i> 1: Start read/writes	0x0
30	RW	RF_LE_SEL	RF_LE selection 0: RF_LE0 activate 1: RF_LE1 activate	0x0
29	RW	RF_LE_STBY	RF_LE standby mode 0: RF_LE is high when standby 1: RF_LE is low when standby	0x0
28:24	RW	RF_REG_WIDTH	RF register bit width	0x16
23:0	RW	RF_REG_0	RF register0 ID and content	0x0

494. RF_CSR_CFG1: (offset: 0x1024)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
24	RW	RF_DUR	RF Duration Gap between BB_CONTROL_RF and RF_LE 0: 3 system clock cycle (37.5 usec) 1: 5 system clock cycle (62.5 usec)	0x0
23:0	RW	RF_REG_1	RF register1 ID and contents	0x0

495. RF_CSR_CFG2: (offset: 0x1028)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:0	RW	RF_REG_2	RF register2 ID and contents	0x0

NOTE: Software should make sure the first bit (MSB in the specified bit number) written to RF is 0 for RF chip mode selection.

496. LED_CFG: (offset: 0x102C)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30	RW	LED_POL	LED Polarity 0: Active low 1: Active high	0x0
29:28	RW	Y_LED_MODE (LED_ACT_N)	Yellow LED Mode Sets the method the LED_ACT_N pin uses to indicate wireless activity. 0: Off 1: Blinking upon Tx 2: Periodic slow blinking 3: Always on	0x0
27:26	-	-	Reserved	0x0
25:24	RW	R_LED_MODE (LED_RDYG_N)	Red LED Mode Sets the method the LED_RDYG_N pin uses to indicate 2.4 GHz wireless transmission 0: Off 1: Blinking upon Tx 2: Periodic slow blinking 3: Always on	0x0
23:22	-	-	Reserved	0x0
21:16	RW	SLOW_BLK_TIME	Slow Blinking Period (unit: sec)	0x3
15:8	RW	LED_OFF_TIME	Tx Blinking Off Period (unit: ms)	0x1E
7:0	RW	LED_ON_TIME	Tx Blinking On Period (unit: ms)	0x46

497. AMPDU_MAX_LEN_20M1S: (offset: 0x1030)

Bits	Type	Name	Description	Initial Value
31:28	RW	AMPDU_MAX_BW20_MCS7	Maximum A-MPDU for BW=20 MHz, MCS 7	0x7
27:24	RW	AMPDU_MAX_BW20_MCS6	Maximum A-MPDU for BW=20 MHz, MCS 6	0x7
23:20	RW	AMPDU_MAX_BW20_MCS5	Maximum A-MPDU for BW=20 MHz, MCS 5	0x7
19:16	RW	AMPDU_MAX_BW20_MCS4	Maximum A-MPDU for BW=20 MHz, MCS 4	0x7
15:12	RW	AMPDU_MAX_BW20_MCS3	Maximum A-MPDU for BW=20 MHz, MCS 3	0x7
11:08	RW	AMPDU_MAX_BW20_MCS2	Maximum A-MPDU for BW=20 MHz, MCS 2	0x7
07:04	RW	AMPDU_MAX_BW20_MCS1	Maximum A-MPDU for BW=20 MHz, MCS 1	0x7
03:00	RW	AMPDU_MAX_BW20_MCS0	Maximum A-MPDU for BW=20 MHz, MCS 0	0x7

NOTE:

- 1: Per MCS maximum A-MPDU length = $2^{(\text{AMPDU_MAX} - 5)}$ bytes. For example, set to 15 means the maximum A-MPDU length is 1024 KB
2. The maximum AMPDU length depends on either the maximum AMPDU length set in this register or the maximum length set by 0x1018 MAX_PSDU_LEN. The smaller of these two values is the maximum AMPDU length.

498. AMPDU_MAX_LEN_20M2S: (offset: 0x1034)

Bits	Type	Name	Description	Initial Value
31:28	RW	AMPDU_MAX_BW20_MCS15	Maximum A-MPDU for BW=20 MHz, MCS 15	0x7
27:24	RW	AMPDU_MAX_BW20_MCS14	Maximum A-MPDU for BW=20 MHz, MCS 14	0x7
23:20	RW	AMPDU_MAX_BW20_MCS13	Maximum A-MPDU for BW=20 MHz, MCS 13	0x7
19:16	RW	AMPDU_MAX_BW20_MCS12	Maximum A-MPDU for BW=20 MHz, MCS 12	0x7
15:12	RW	AMPDU_MAX_BW20_MCS11	Maximum A-MPDU for BW=20 MHz, MCS 11	0x7
11:08	RW	AMPDU_MAX_BW20_MCS10	Maximum A-MPDU for BW=20 MHz, MCS 10	0x7
07:04	RW	AMPDU_MAX_BW20_MCS9	Maximum A-MPDU for BW=20 MHz, MCS 9	0x7
03:00	RW	AMPDU_MAX_BW20_MCS8	Maximum A-MPDU for BW=20 MHz, MCS 8	0x7

NOTE:

- 1: Per MCS maximum A-MPDU length = $2^{(AMPDU_MAX - 5)}$ bytes. For example, set to 15 means the maximum A-MPDU length is 1024 KB.
2. The maximum AMPDU length depends on either the maximum AMPDU length set in this register or the maximum length set by 0x1018 MAX_PSDU_LEN. The smaller of these two values is the maximum AMPDU length.

499. AMPDU_MAX_LEN_40M1S: (offset: 0x1038)

Bits	Type	Name	Description	Initial Value
31:28	RW	AMPDU_MAX_BW40_MCS7	Maximum A-MPDU for BW=40 MHz, MCS 7	0x7
27:24	RW	AMPDU_MAX_BW40_MCS6	Maximum A-MPDU for BW=40 MHz, MCS 6	0x7
23:20	RW	AMPDU_MAX_BW40_MCS5	Maximum A-MPDU for BW=40 MHz, MCS 5	0x7
19:16	RW	AMPDU_MAX_BW40_MCS4	Maximum A-MPDU for BW=40 MHz, MCS 4	0x7
15:12	RW	AMPDU_MAX_BW40_MCS3	Maximum A-MPDU for BW=40 MHz, MCS 3	0x7
11:08	RW	AMPDU_MAX_BW40_MCS2	Maximum A-MPDU for BW=40 MHz, MCS 2	0x7
07:04	RW	AMPDU_MAX_BW40_MCS1	Maximum A-MPDU for BW=40 MHz, MCS 1	0x7
03:00	RW	AMPDU_MAX_BW40_MCS0	Maximum A-MPDU for BW=40 MHz, MCS 0	0x7

NOTE:

- 1: Per MCS maximum A-MPDU length = $2^{(AMPDU_MAX - 5)}$ bytes. For example, set to 15 means the maximum A-MPDU length is 1024 KB
2. The maximum AMPDU length depends on either the maximum AMPDU length set in this register or the maximum length set by 0x1018 MAX_PSDU_LEN. The smaller of these two values is the maximum AMPDU length.

500. AMPDU_MAX_LEN_40M2S: (offset: 0x103C)

Bits	Type	Name	Description	Initial Value
31:28	RW	AMPDU_MAX_BW40_MCS15	Maximum A-MPDU for BW=40 MHz, MCS 15	0x7
27:24	RW	AMPDU_MAX_BW40_MCS14	Maximum A-MPDU for BW=40 MHz, MCS 14	0x7
23:20	RW	AMPDU_MAX_BW40_MCS13	Maximum A-MPDU for BW=40 MHz, MCS 13	0x7
19:16	RW	AMPDU_MAX_BW40_MCS12	Maximum A-MPDU for BW=40 MHz, MCS 12	0x7
15:12	RW	AMPDU_MAX_BW40_MCS11	Maximum A-MPDU for BW=40 MHz, MCS 11	0x7
11:08	RW	AMPDU_MAX_BW40_MCS10	Maximum A-MPDU for BW=40 MHz, MCS 10	0x7

Bits	Type	Name	Description	Initial Value
07:04	RW	AMPDU_MAX_BW40_MCS9	Maximum A-MPDU for BW=40 MHz, MCS 9	0x7
03:00	RW	AMPDU_MAX_BW40_MCS8	Maximum A-MPDU for BW=40 MHz, MCS 8	0x7

NOTE:

- 1: Per MCS maximum A-MPDU length = $2^{(AMPDU_MAX - 5)}$ bytes. For example, set to 15 means the maximum A-MPDU length is 1024 KB
2. The maximum AMPDU length depends on either the maximum AMPDU length set in this register or the maximum length set by 0x1018 MAX_PSDU_LEN. The smaller of these two values is the maximum AMPDU length.

501. AMPDU_BA_WINSIZE: (offset: 0x1040)

Bits	Type	Name	Description	Initial Value
31:07	-	-	Reserved	0x0
06	RW	FORCE_BA_WINSIZE_EN	Force BA Window Size Enable Force sets the BA window size over the BA window size value set in TXWI. 0: Disable 1: Enable	0x0
05:00	RW	FORCE_BA_WINSIZE	Forced BA Window Size	0x0

502. TX_WCID_DROP_MASK0: Tx Wireless Client ID Drop Mask 0 (offset: 0x106C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_WCID_DROP_MASK0-31	Drops the Tx frame with the specified WCID. 0: WCID0 1: WCID1 ... 31: WCID31 0: Disable 1: Enable	0x0000_0000

503. TX_WCID_DROP_MASK1: Tx Wireless Client ID Drop Mask 1 (offset: 0x1070, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_WCID_DROP_MASK32-63	Drops the Tx frame with the specified WCID. 0: WCID32 1: WCID33 ... 31: WCID63 0: Disable 1: Enable	0x0000_0000

504. TX_WCID_DROP_MASK2: Tx Wireless Client ID Drop Mask 2 (offset: 0x1074, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_WCID_DROP_MASK64-95	Drops the Tx frame with the specified WCID. 0: WCID64 1: WCID65 ... 31: WCID95 0: Disable 1: Enable	0x0000_0000

505. TX_WCID_DROP_MASK3: Tx Wireless Client ID Drop Mask 3 (offset: 0x1078, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_WCID_DROP_MASK96-127	Drops the Tx frame with the specified WCID. 0: WCID96 1: WCID97 ... 31: WCID127 0: Disable 1: Enable	0x0000_0000

506. TX_WCID_DROP_MASK4: Tx Wireless Client ID Drop Mask 4 (offset: 0x107C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_WCID_DROP_MASK128-159	Drops the Tx frame with the specified WCID. 0: WCID128 1: WCID129 ... 31: WCID159 0: Disable 1: Enable	0x0000_0000

507. TX_WCID_DROP_MASK5: Tx Wireless Client ID Drop Mask 5 (offset: 0x1080, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_WCID_DROP_MASK160-191	Drops the Tx frame with the specified WCID. 0: WCID160 1: WCID161 ... 31: WCID191 0: Disable 1: Enable	0x0000_0000

508. TX_WCID_DROP_MASK6: Tx Wireless Client ID Drop Mask 6 (offset: 0x1084, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:0	R/W	TX_WCID_DROP_MASK192-223	Drops the Tx frame with the specified WCID. 0: WCID192 1: WCID193 ... 31: WCID223 0: Disable 1: Enable	0x0000_0000

509. TX_WCID_DROP_MASK7: Tx Wireless Client ID Drop Mask 7 (offset: 0x1088, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
	R/W	TX_WCID_DROP_MASK224-255	Drops the Tx frame with the specified WCID. 0: WCID224 1: WCID225 ... 31: WCID255 0: Disable 1: Enable	0x0000_0000

510. TX_BCN_BYPASS_MASK: Tx Beacon Bypass Mask (offset: 0x108C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:0	R/W	TX_BCN_DROP_MASK0-15	Directly bypasses the Tx Beacon frame with the specified Beacon number. Bit0=Nth Beacon, bit1=(N-1)th Beacon,... etc. N is the number of Beacons defined in the MULTI_BCN_NUM field in the MAC_BSSID_DW1(offset: 0x1014) register. 0: Disable 1: Enable	0x0000

511. AP_CLIENT_BSSID0_L: AP Client Base Station ID 0 Low (offset: 0x1090, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID0_3	AP client BSSID0 byte3	0x00
23:16	R/W	APC_BSSID0_2	AP client BSSID0 byte2	0x00
15:8	R/W	APC_BSSID0_1	AP client BSSID0 byte1	0x00
7:0	R/W	APC_BSSID0_0	AP client BSSID0 byte0	0x00

512. AP_CLIENT_BSSID0_H: AP Client Base Station ID 0 High (offset: 0x1094, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0000
16	R/W	APC_BSSID_EN	Enables AP client mode (occupy BSSIDX8-16 of multiple BSSID mode). 0: Disable 1: Enable	0x0
15:8	R/W	APC_BSSID0_5	AP client BSSID0 byte5	0x00

Bits	Type	Name	Description	Initial Value
7:0	R/W	APC_BSSID0_4	AP client BSSID0 byte4	0x00

513. AP_CLIENT_BSSID1_L: AP Client Base Station ID 1 Low (offset: 0x1098, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID1_3	AP client BSSID1 byte3	0x00
23:16	R/W	APC_BSSID1_2	AP client BSSID1 byte2	0x00
15:8	R/W	APC_BSSID1_1	AP client BSSID1 byte1	0x00
7:0	R/W	APC_BSSID1_0	AP client BSSID1 byte0	0x00

514. AP_CLIENT_BSSID1_H: AP Client Base Station ID 1 High (offset: 0x109C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	R/W	APC_BSSID1_5	AP client BSSID1 byte5	0x00
7:0	R/W	APC_BSSID1_4	AP client BSSID1 byte4	0x00

515. AP_CLIENT_BSSID2_L: AP Client Base Station ID 2 Low (offset: 0x10A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID2_3	AP client BSSID2 byte3	0x00
23:16	R/W	APC_BSSID2_2	AP client BSSID2 byte2	0x00
15:8	R/W	APC_BSSID2_1	AP client BSSID2 byte1	0x00
7:0	R/W	APC_BSSID2_0	AP client BSSID2 byte0	0x00

516. AP_CLIENT_BSSID2_H: AP Client Base Station ID 2 High (offset: 0x10A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	R/W	APC_BSSID2_5	AP client BSSID2 byte5	0x00
7:0	R/W	APC_BSSID2_4	AP client BSSID2 byte4	0x00

517. AP_CLIENT_BSSID3_L: AP Client Base Station ID 3 Low (offset: 0x10A8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID3_3	AP client BSSID3 byte3	0x00
23:16	R/W	APC_BSSID3_2	AP client BSSID3 byte2	0x00
15:8	R/W	APC_BSSID3_1	AP client BSSID3 byte1	0x00
7:0	R/W	APC_BSSID3_0	AP client BSSID3 byte0	0x00

518. AP_CLIENT_BSSID3_H: AP Client Base Station ID 3 High (offset: 0x10AC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	R/W	APC_BSSID3_5	AP client BSSID3 byte5	0x00
7:0	R/W	APC_BSSID3_4	AP client BSSID3 byte4	0x00

519. AP_CLIENT_BSSID4_L: AP Client Base Station ID 4 Low (offset: 0x10B0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID4_3	AP client BSSID4 byte3	0x00
23:16	R/W	APC_BSSID4_2	AP client BSSID4 byte2	0x00
15:8	R/W	APC_BSSID4_1	AP client BSSID4 byte1	0x00
7:0	R/W	APC_BSSID4_0	AP client BSSID4 byte0	0x00

520. AP_CLIENT_BSSID4_H: AP Client Base Station ID 4 High (offset: 0x10B4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	R/W	APC_BSSID4_5	AP client BSSID4 byte5	0x00
7:0	R/W	APC_BSSID4_4	AP client BSSID4 byte4	0x00

521. AP_CLIENT_BSSID5_L: AP Client Base Station ID 5 Low (offset: 0x10B8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID5_3	AP client BSSID5 byte3	0x00
23:16	R/W	APC_BSSID5_2	AP client BSSID5 byte2	0x00
15:8	R/W	APC_BSSID5_1	AP client BSSID5 byte1	0x00
7:0	R/W	APC_BSSID5_0	AP client BSSID5 byte0	0x00

522. AP_CLIENT_BSSID5_H: AP Client Base Station ID 5 High (offset: 0x10BC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	R/W	APC_BSSID5_5	AP client BSSID5 byte5	0x00
7:0	R/W	APC_BSSID5_4	AP client BSSID5 byte4	0x00

523. AP_CLIENT_BSSID6_L: AP Client Base Station ID 6 Low (offset: 0x10C0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID6_3	AP client BSSID6 byte3	0x00
23:16	R/W	APC_BSSID6_2	AP client BSSID6 byte2	0x00
15:8	R/W	APC_BSSID6_1	AP client BSSID6 byte1	0x00
7:0	R/W	APC_BSSID6_0	AP client BSSID6 byte0	0x00

524. AP_CLIENT_BSSID6_H: AP Client Base Station ID 6 High (offset: 0x10C4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	R/W	APC_BSSID6_5	AP client BSSID6 byte5	0x00
7:0	R/W	APC_BSSID6_4	AP client BSSID6 byte4	0x00

525. AP_CLIENT_BSSID7_L: AP Client Base Station ID 7 Low (offset: 0x10C8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:24	R/W	APC_BSSID7_3	AP client BSSID7 byte3	0x00
23:16	R/W	APC_BSSID7_2	AP client BSSID7 byte2	0x00

Bits	Type	Name	Description	Initial Value
15:8	R/W	APC_BSSID7_1	AP client BSSID7 byte1	0x00
7:0	R/W	APC_BSSID7_0	AP client BSSID7 byte0	0x00

526. AP_CLIENT_BSSID7_H: AP Client Base Station ID 7 High (offset: 0x10CC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0000
15:8	R/W	APC_BSSID7_5	AP client BSSID7 byte5	0x00
7:0	R/W	APC_BSSID7_4	AP client BSSID7 byte4	0x00

527. BT_WINDOW_CFG: Bluetooth Window Configuration (offset: 0x10D0, default: 0x04E2_00FA)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26:16	R/W	BT_WIN_SIZE	Bluetooth slot window size for Bluetooth slot phase tracking (unit: μ sec)	1250
15:11	-	-	Reserved	0x0
10:0	R/W	PRE_BT_WIN_SIZE	Pre-Bluetooth slot window size (unit: μ sec) Pre-Bluetooth slot window will block WLAN Tx.	250

528. BT_COEX_CFG (offset: 0x10D4, default: 0x0010_D3FF)

Bits	Type	Name	Description	Initial Value
31:22	R		Reserved	0
21:16	R/W	BT_RPI_WIN_SIZE	Bluetooth priority indication window in 3-wire/4-wire mode (unit: usec)	0x10
15:8	R/W	WLAN_BT_DIS	WLAN high priority event (higher priority than Bluetooth) Bit8: non-Beacon TX event Bit9: Beacon TX event Bit10: RX event Bit11: ACK RX event Bit12: ACK TX event Bit13: CTS TX event Bit14: implicit BA TX event Bit15: explicit BA TX event	0xD3
7:0	R/W	WLAN_BT_EN	Truth table of Bluetooth halt WLAN activity condition {BT_AUX_IN, BT_HIGH_PRIORITY, BT_TX_STATE}	0xFF

2.22.8 MAC Timing Control Registers (base: 0x1018_0000)

2.22.8.1 List of Registers

No.	Offset	Register Name	Description	Page
529	0x1100	XIFS_TIME_CFG	Inter-Frame Space Time Configuration	410
530	0x1104	BKOFF_SLOT_CFG	Back-off Slot Configuration	410
531	0x1108	NAV_TIME_CFG	Network Allocation Vector Time Configuration	411
532	0x110C	CH_TIME_CFG	Channel Time Configuration	411
533	0x1110	PBF_LIFE_TIMER	Packet Buffer Life Timer	412
534	0x1114	BCN_TIME_CFG	Beacon Time Configuration	412
535	0x1118	TBTT_SYNC_CFG	Target Beacon Transmission Time (TBTT) Synchronization Configuration	413
536	0x111C	TSF_TIMER_DW0	Timing Synchronization Function Timer DWORD 0	413
537	0x1120	TSF_TIMER_DW1	Timing Synchronization Function Timer DWORD 1	413
538	0x1124	TBTT_TIMER	TBTT Timer	414
539	0x1128	INT_TIMER_CFG	Internal Timer Configuration	414
540	0x112C	INT_TIMER_EN	Internal Timer Enable	414
541	0x1130	CH_IDLE_STA	Channel Idle Status	414
542	0x1134	CH_BUSY_STA	Channel Busy Status	414
543	0x1138	EXT_CH_BUSY_STA	External Channel Busy Status	415
544	0x113C	BBP_IPI_TIMER	Baseband Idle Power Indicator Timer	415

2.22.8.2 Register Descriptions

529. XIFS_TIME_CFG: (offset: 0x1100)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x0
29	RW	BB_RXEND_EN	Enables the BB_RX_END signal. Starts deferring the Short Inter-Frame Space (SIFS) from the BB_RX_END signal from the BBP Rx logic circuit. 0: Disable 1: Enable	0x1
28:20	RW	EIFS_TIME	The defer time after receiving a CRC error packet. After deferring EIFS (Extended Inter-Frame Space), the normal back-off process may proceed. (unit: μ s)	0x13A
19:16	RW	OFDM_XIFS_TIME	Delayed OFDM SIFS time compensator When BB_RX_END from BBP is a delayed version the SIFS deferred is (OFDM_SIFS_TIME - OFDM_XIFS_TIME). (unit: μ s)	0x4
15:8	RW	OFDM_SIFS_TIME	OFDM SIFS time Applied after OFDM Tx/Rx. (unit: μ s)	0x10
7:0	RW	CCK_SIFS_TIME	CCK SIFS time Applied after CCK Tx/Rx. (unit: μ s)	0xA

NOTE:

1: EIFS = SIFS + ACK @ 1 Mbps + DIFS = 10 μ s (SIFS) + 192 μ s (long preamble) + 14*8 μ s (ACK) + 50 μ s (DIFS) = 364. However, MAC should start back-off procedure after (EIFS-DIFS).

2: EIFS is not applied if MAC is a TXOP initiator that owns the channel.

3: EIFS is not started if A-MPDU is only partially corrupted.

Caution: It is recommended that neither CCK_SIFS_TIME nor OFDM_SIFS_TIME are less than the Tx/Rx transition time. If the SIFS value is not long enough, a SIFS burst transmission may be replaced with a PIFS burst.

530. BKOFF_SLOT_CFG: (offset: 0x1104)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:8	RW	CC_DELAY_TIME	Channel Clear Delay This value specifies the Tx guard time after the channel is clear. (unit: μ s)	0x2

Bits	Type	Name	Description	Initial Value
7:0	RW	SLOT_TIME	Slot Time This value specifies the slot boundary after deferring SIFS time. NOTE: Default 20 μ s is for 11b/g. 11a and 11g-short-slot-mode is 9 μ s. (unit: μ s)	0x14

531. NAV_TIME_CFG: (offset: 0x1108)

Bits	Type	Name	Description	Initial Value
31	W1C	NAV_UPD	NAV Update Manually updates the NAV timer. 0: No effect. 1: Update NAV timer with NAV_UPD_VAL.	0x0
30:16	RW	NAV_UPD_VAL	NAV Update Value Sets the NAV timer manual update period. (unit: 1 μ s)	0x0
15	RW	NAV_CLR_EN	NAV Clear Enable Enables auto-clear of the NAV timer. When enabled, MAC auto-clears the NAV timer after receiving a CF-End frame from the previous NAV holder STA. 0: Disable 1: Enable	0x1
14:0	RW	NAV_TIMER	NAV Timer The timer is set by other STA and auto-counts down to zero. The STA which sets the NAV timer is called the NAV holder. When the NAV timer is non-zero, MAC does not send any packets. (unit: 1 μ s)	0x0

532. CH_TIME_CFG: (offset: 0x110C)

Bits	Type	Name	Description	Initial Value
31:5	-	-	Reserved	0x0
4	RW	EIFS_AS_CH_BUSY	Treats EIFS as a busy channel.	0x1
3	RW	NAV_AS_CH_BUSY	Treats NAV as a busy channel.	0x1
2	RW	RX_AS_CH_BUSY	Treats Rx as a busy channel.	0x1
1	RW	TX_AS_CH_BUSY	Treats Tx as a busy channel.	0x1
0	RW	CH_STA_TIMER_EN	Enables the channel statistic timer.	0x0

NOTE:

0: Disable

1: Enable

533. PBF_LIFE_TIMER: (offset: 0x1110)

Bits	Type	Name	Description	Initial Value
31:0	RO	PBF_LIFE_TIMER	Reads the current time value of the Tx/Rx MPDU timestamp timer (always in free run mode) (unit: 1 μ s)	0x0

534. BCN_TIME_CFG: (offset: 0x1114)

Bits	Type	Name	Description	Initial Value
31:24	RW	TSF_INS_COMP	TSF Insertion Compensation Value When inserting TSF (Timing Synchronization Function), add this value to the current value of the local TSF timer to make the Beacon frame's Tx timestamp. (unit: μ s)	0x0
23:21	-	-	Reserved	0x0
20	RW	BCN_TX_EN	Beacon Frame Tx Enable Sets the the MAC to send a Beacon frame when triggered by the TBTT interrupt. 0: Disable 1: Enable	0x0
19	RW	TBTT_TIMER_EN	TBTT Timer Enable When enabled, a TBTT interrupt is issued periodically at intervals specified in BCN_INTVAL (see below). 0: Disable 1: Enable	0x0
18:17	RW	TSF_SYNC_MODE	Sets the local 64-bit TSF timer synchronization mode. 00: Disable 01: (STA infrastructure mode) Upon receiving a Beacon frame from an associated BSS, the local TSF is always updated with a remote TSF. 10: (STA ad-hoc mode) Upon receiving a Beacon frame from an associated BSS, the local TSF is updated with a remote TSF only if the remote TSF is greater than local TSF. 11: (AP mode) does not SYNC with any station.	0x0
16	RW	TSF_TIMER_EN	Enables the local 64-bit TSF timer. When enabled, the TSF timer re-starts from zero. 0: Disable 1: Enable	0x0

Bits	Type	Name	Description	Initial Value
15:0	RW	BCN_INTVAL	Beacon Interval This value specifies the interval between Beacon frames. The maximum Beacon interval is approx. 4 sec. The minimum is approx. 100 msec. (unit: 64 μ s)	0x640

535. TBTT_SYNC_CFG: (offset: 0x1118)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:20	RW	BCN_CWMIN	Beacon CWmin Sets beacon transmission CWmin after the TBTT interrupt. (unit: slot time)	0x4
19:16	RW	BCN_AIFSN	Beacon AIFSN Sets beacon transmission AIFSN after the TBTT interrupt (unit: slot time)	0x2
15:8	RW	BCN_EXP_WIN	Beacon Expecting Window Duration Sets the period when the client listens for the Beacon. The window starts from the TBTT interrupt. The phase of "TBTT interrupt train" is NOT adjusted by the arrival of a Beacon within the window. (unit: 64 μ s)	0x20
7:0	RW	TBTT_ADJUST	IBSS Mode TBTT Phase Adaptive Adjustment Step In IBSS mode (ad hoc), if consecutive Tx Beacon failures (or consecutive successes) occur, the TBTT timer adjusts its phase to meet the external ad hoc TBTT time. (unit: μ s)	0x10

536. TSF_TIMER_DW0: (offset: 0x111C)

Bits	Type	Name	Description	Initial Value
31:0	RO	TSF_TIMER_DW0	Bit[31:0] of the 64-bit local TSF timer (unit: 1 μ s)	0x0

537. TSF_TIMER_DW1: (offset: 0x1120)

Bits	Type	Name	Description	Initial Value
31:0	RO	TSF_TIMER_DW1	Bit[63:32] of the 64-bit local TSF timer (unit: 1 μ s)	0x0

538. TBTT_TIMER: (offset: 0x1124)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
16:0	RO	TBTT_TIMER	TBTT Timer Shows the time remaining on the TBTT timer as it counts down to the TBTT. 0: The timer is disabled and stays at 0. 1: The timer counts down from BCN_INTVAL to 0. (unit: 32 μ s)	0x0

539. INT_TIMER_CFG: (offset: 0x1128)

Bits	Type	Name	Description	Initial Value
31:16	RW	GP_TIMER	General Purpose Timer Sets the time for the general purpose timer to trigger an interrupt. (unit: 64 μ s)	0x0
15:0	RW	PRE_TBTT_TIMER	Pre-TBTT Interrupt Timer Sets the interval before the TBTT when the pre-TBTT interrupt is triggered. (unit: 64 μ s)	0x0

540. INT_TIMER_EN: (offset: 0x112C)

Bits	Type	Name	Description	Initial Value
31:2	-	-	Reserved	0x0
1	RW	GP_TIMER_EN	Enables the periodic general purpose interrupt timer.	0x0
0	RW	PRE_TBTT_INT_EN	Enables the pre-TBTT interrupt.	0x0

NOTE:

0: Disable

1: Enable

541. CH_IDLE_STA: (offset: 0x1130)

Bits	Type	Name	Description	Initial Value
31:0	RC	CH_IDLE_TIME	Channel Idle Time The channel busy time can be derived by the equation: $CH_BUSY_TIME = \text{host polling period} - CH_IDLE_TIME$ (unit: μ s)	0x0

542. CH_BUSY_STA: (offset: 0x1134)

Bits	Type	Name	Description	Initial Value
31:0	RC	CH_BUSY_TIME	Channel Busy Time (unit: μ s)	0x0

543. EXT_CH_BUSY_STA: (offset: 0x1138)

Bits	Type	Name	Description	Initial Value
31:0	RC	EXT_CH_BUSY_TIME	Extension Channel Busy Time (unit: μ s)	0x0

544. BBP_IPI_TIMER: (offset: 0x113C)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
16	RW	BBP_IPI_KICK	Baseband IPI Kick Begins measurement of the BBP idle power indicator (IPI). <i>Read:</i> 0: No effect 1: BBP IPI begun <i>Write:</i> 1: Starts the measurement of BBP IPI.	0x0
15:0	RW	BBP_IPI_TIMER	Baseband IPI Timer Measurement period of BBP IPI (unit: 1.024 ms)	0x0

2.22.9 MAC Power Save Configuration Registers (base: 0x1018_0000)

2.22.9.1 List of Registers

No.	Offset	Register Name	Description	Page
545	0x1200	MAC_STATUS_REG	MAC Status Register	417
546	0x1204	PWR_PIN_CFG	Power Pin Configuration	417
547	0x1208	AUTO_WAKEUP_CFG	Auto-Wakeup Configuration	417
548	0x120C	AUX_CLK_EN	Auxiliary Clock Enable	418
549	0x1210	MIMO_PS_CFG	MIMO Power-save Configuration	418
550	0x1214	BB_PA_MODE_CFG0	Baseband Power Amplifier Mode Configuration 0	418
551	0x1218	BB_PA_MODE_CFG1	Baseband Power Amplifier Mode Configuration 1	419
552	0x121C	RF_PA_MODE_CFG0	RF Power Amplifier Mode Configuration 0	419
553	0x1220	RF_PA_MODE_CFG1	RF Power Amplifier Mode Configuration 1	420

2.22.9.2 Register Descriptions

545. MAC_STATUS_REG: (offset: 0x1200)

Bits	Type	Name	Description	Initial Value
31:2	-	-	Reserved	0x0
1	RO	RX_STATUS	Rx Status Indicates that Rx is busy. 0: Idle 1: Busy	0x0
0	RO	TX_STATUS	Tx Status. Indicates that Tx is busy. 0: Idle 1: Busy	0x0

546. PWR_PIN_CFG: (offset: 0x1204)

Bits	Type	Name	Description	Initial Value
31:4	-	-	Reserved	0x0
3	RW	IO_ADDA_PD	AD/DA Power-Down Powers down the AD/DA.	0x1
2	RW	IO_PLL_PD	PLL Power-Down Powers down the PLL.	0x0
1	RW	IO_RA_PE	Radio Power Enable Enables power to the radio block.	0x1
0	RW	IO_RF_PE	RF Power Enable Enables power to the radio Tx/Rx unit.	0x0

NOTE:

0: Disable

1: Enable

547. AUTO_WAKEUP_CFG: (offset: 0x1208)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15	RW	AUTO_WAKEUP_EN	Auto-Wakeup Enable Enables the auto-wakeup interrupt. The auto-wakeup interrupt is issued at the time determined by the following equation: Auto-wakeup interrupt time = (SLEEP_TBTT_NUM + 1) * TBTT - WAKEUP_LEAD_TIME 0: Disable 1: Enable NOTE: Please make sure TBTT_TIMER_EN is enabled.	0x0
14:8	RW	SLEEP_TBTT_NUM	Sleep Mode TBTT Number Number of TBTT interrupts to be ignored during sleep mode.	0x0

Bits	Type	Name	Description	Initial Value
7:0	RW	WAKEUP_LEAD_TIME	Auto-Wakeup Lead Time Sets the auto-wakeup lead time. (unit: 1 TU (1024 μ s))	0x14

548. AUX_CLK_EN (offset: 0x120C, default: 0x0000_0001)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	0
0	R/W	AUX_CLK_EN	Auxiliary Clock Enable Enables slow clock for power-saving period. 0: Disable 1: Enable	1

549. MIMO_PS_CFG (offset: 0x1210, default: 0x0000_0004)

Bits	Type	Name	Description	Initial Value
31:6	-	-	Reserved	0
5	R/W	RX_RX_STBY0	RF RX0 standby control	0
4	R/W	RX_STBY_POL	RF RX standby polarity 0: High active 1: Low active	0
3	R/W	MMPS_RF_EN	RF MIMO power save mode 0: Disable 1: Enable	0
2:1	R/W	MMPS_RX_ANT_NUM	Number of RX antenna in MIMO power save mode.	2
0	R/W	MMPS_BB_EN	BB MIMO power save mode 0: Disable 1: Enable	0

550. BB_PA_MODE_CFG0 (offset: 0x1214, default: 0x0100_55ff)

Bits	Type	Name	Description	Initial Value
31:26	-	-	Reserved	0x0
25:24	R/W	BB_PA_MODE_MCS32	BB PA MCS32 Mode Select	0x1
23:22	R/W	BB_PA_MODE_OFDM54	BB PA OFDM54 Mode Select	0x0
21:20	R/W	BB_PA_MODE_OFDM48	BB PA OFDM48 Mode Select	0x0
19:18	R/W	BB_PA_MODE_OFDM36	BB PA OFDM36 Mode Select	0x0
17:16	R/W	BB_PA_MODE_OFDM24	BB PA OFDM24 Mode Select	0x0
15:14	R/W	BB_PA_MODE_OFDM18	BB PA OFDM18 Mode Select	0x1
13:12	R/W	BB_PA_MODE_OFDM12	BB PA OFDM12 Mode Select	0x1
11:10	R/W	BB_PA_MODE_OFDM9	BB PA OFDM9 Mode Select	0x1
9:8	R/W	BB_PA_MODE_OFDM6	BB PA OFDM6 Mode Select	0x1
7:6	R/W	BB_PA_MODE_CCK11	BB PA CCK11 Mode Select	0x3
5:4	R/W	BB_PA_MODE_CCK5	BB PA CCK5 Mode Select	0x3

Bits	Type	Name	Description	Initial Value
3:2	R/W	BB_PA_MODE_CCK2	BB PA CCK2 Mode Select	0x3
1:0	R/W	BB_PA_MODE_CCK1	BB PA CCK1 Mode Select	0x3

NOTE:

00: OFDM EVM limited

01: OFDM spectrum mask limited

10: CCK EVM limited

11: CCK spectrum mask limited

551. BB_PA_MODE_CFG1 (offset: 0x1218, default: 0x0055_0055)

Bits	Type	Name	Description	Initial Value
31:30	R/W	BB_PA_MODE_HT15	BB PA HT 15 Mode Select	0x0
29:28	R/W	BB_PA_MODE_HT14	BB PA HT14 Mode Select	0x0
27:26	R/W	BB_PA_MODE_HT13	BB PA HT13 Mode Select	0x0
25:24	R/W	BB_PA_MODE_HT12	BB PA HT12 Mode Select	0x0
23:22	R/W	BB_PA_MODE_HT11	BB PA HT11 Mode Select	0x1
21:20	R/W	BB_PA_MODE_HT10	BB PA HT10 Mode Select	0x1
19:18	R/W	BB_PA_MODE_HT9	BB PA HT9 Mode Select	0x1
17:16	R/W	BB_PA_MODE_HT8	BB PA HT8 Mode Select	0x1
15:14	R/W	BB_PA_MODE_HT7	BB PA HT7 Mode Select	0x0
13:12	R/W	BB_PA_MODE_HT6	BB PA HT6 Mode Select	0x0
11:10	R/W	BB_PA_MODE_HT5	BB PA HT5 Mode Select	0x0
9:8	R/W	BB_PA_MODE_HT4	BB PA HT4 Mode Select	0x0
7:6	R/W	BB_PA_MODE_HT3	BB PA HT3 Mode Select	0x1
5:4	R/W	BB_PA_MODE_HT2	BB PA HT2 Mode Select	0x1
3:2	R/W	BB_PA_MODE_HT1	BB PA HT1 Mode Select	0x1
1:0	R/W	BB_PA_MODE_HT0	BB PA HT0 Mode Select	0x1

NOTE:

00: OFDM EVM limited

01: OFDM spectrum mask limited

10: CCK EVM limited

11: CCK spectrum mask limited

552. RF_PA_MODE_CFG0 (offset: 0x121C, default: 0x0100_55ff)

Bits	Type	Name	Description	Initial Value
31:26	-	-	Reserved	0x0
25:24	R/W	RF_PA_MODE_MCS32	BB PA MCS32 Mode Select	0x1
23:22	R/W	RF_PA_MODE_OFDM54	BB PA OFDM54 Mode Select	0x0
21:20	R/W	RF_PA_MODE_OFDM48	BB PA OFDM48 Mode Select	0x0
19:18	R/W	RF_PA_MODE_OFDM36	BB PA OFDM36 Mode Select	0x0
17:16	R/W	RF_PA_MODE_OFDM24	BB PA OFDM24 Mode Select	0x0
15:14	R/W	RF_PA_MODE_OFDM18	BB PA OFDM18 Mode Select	0x1
13:12	R/W	RF_PA_MODE_OFDM12	BB PA OFDM12 Mode Select	0x1

Bits	Type	Name	Description	Initial Value
11:10	R/W	RF_PA_MODE_OFDM9	BB PA OFDM9 Mode Select	0x1
9:8	R/W	RF_PA_MODE_OFDM6	BB PA OFDM6 Mode Select	0x1
7:6	R/W	RF_PA_MODE_CCK11	BB PA CCK11 Mode Select	0xf
5:4	R/W	RF_PA_MODE_CCK5	BB PA CCK5 Mode Select	0xf
3:2	R/W	RF_PA_MODE_CCK2	BB PA CCK2 Mode Select	0xf
1:0	R/W	RF_PA_MODE_CCK1	BB PA CCK1 Mode Select	0xf

NOTE:

00: OFDM EVM limited

01: OFDM spectrum mask limited

10: CCK EVM limited

11: CCK spectrum mask limited

553. RF_PA_MODE_CFG1 (offset: 0x1220, default: 0x0055_0055)

Bits	Type	Name	Description	Initial Value
31:30	R/W	RF_PA_MODE_HT15	BB PA HT15 Mode Select	0x0
29:28	R/W	RF_PA_MODE_HT14	BB PA HT14 Mode Select	0x0
27:26	R/W	RF_PA_MODE_HT13	BB PA HT13 Mode Select	0x0
25:24	R/W	RF_PA_MODE_HT12	BB PA HT12 Mode Select	0x0
23:22	R/W	RF_PA_MODE_HT11	BB PA HT11 Mode Select	0x1
21:20	R/W	RF_PA_MODE_HT10	BB PA HT10 Mode Select	0x1
19:18	R/W	RF_PA_MODE_HT9	BB PA HT9 Mode Select	0x1
17:16	R/W	RF_PA_MODE_HT8	BB PA HT8 Mode Select	0x1
15:14	R/W	RF_PA_MODE_HT7	BB PA HT7 Mode Select	0x0
13:12	R/W	RF_PA_MODE_HT6	BB PA HT6 Mode Select	0x0
11:10	R/W	RF_PA_MODE_HT5	BB PA HT5 Mode Select	0x0
9:8	R/W	RF_PA_MODE_HT4	BB PA HT4 Mode Select	0x0
7:6	R/W	RF_PA_MODE_HT3	BB PA HT3 Mode Select	0x1
5:4	R/W	RF_PA_MODE_HT2	BB PA HT2 Mode Select	0x1
3:2	R/W	RF_PA_MODE_HT1	BB PA HT1 Mode Select	0x1
1:0	R/W	RF_PA_MODE_HT0	BB PA HT0 Mode Select	0x1

NOTE:

00: OFDM EVM limited

01: OFDM spectrum mask limited

10: CCK EVM limited

11: CCK spectrum mask limited

2.22.10 MAC Tx Configuration Registers (base: 0x1018_0000)

2.22.10.1 List of Registers

No.	Offset	Register Name	Description	Page
554	0x1300	EDCA_AC0_CFG (BE)	Enhanced Distributed Channel Access (EDCA) Access Category 0 Configuration (Best Effort)	423
555	0x1304	EDCA_AC1_CFG (BK)	EDCA Access Category 1 Configuration (Background)	423
556	0x1308	EDCA_AC2_CFG (VI)	EDCA Access Category 2 Configuration (Video)	424
557	0x130C	EDCA_AC3_CFG (VO)	EDCA Access Category 3 Configuration (Voice)	424
558	0x1310	EDCA_TID_AC_MAP	EDCA Traffic ID Access Category Mapping	424
559	0x1314	TX_PWR_CFG_0	Transmit Power Configuration 0	425
...	...	...	...	
566	0x13DC	TX_PWR_CFG_9	Transmit Power Configuration 7	426
567	0x1328	TX_PIN_CFG	Transmit Pin Configuration	426
568	0x132C	TX_BAND_CFG	Transmit Bandwidth Configuration	428
569	0x1330	TX_SW_CFG0	Transmit Switch Configuration 0	428
570	0x1334	TX_SW_CFG1	Transmit Switch Configuration 1	428
571	0x1338	TX_SW_CFG2	Transmit Switch Configuration 2	429
572	0x133C	TXOP_THRES_CFG	Transmit Opportunity Threshold Configuration	429
573	0x1340	TXOP_CTRL_CFG	Transmit Opportunity Control Configuration	430
574	0x1344	TX_RTS_CFG	Transmit Request to Send Configuration	431
575	0x1348	TX_TIMEOUT_CFG	Transmit Timeout Configuration	431
576	0x134C	TX_RTY_CFG	Transmit Retry Configuration	431
577	0x1350	TX_LINK_CFG	Transmit Link Configuration	432
578	0x1354	HT_FBK_CFG0	High Throughput Fallback Configuration 0	432
579	0x1358	HT_FBK_CFG1	High Throughput Fallback Configuration 1	433
580	0x135C	LG_FBK_CFG0	Legacy Fallback Configuration 0	433
581	0x1360	LG_FBK_CFG1	Legacy Fallback Configuration 1	433
582	0x1364	CCK_PROT_CFG	Complementary Code Keying Protection Configuration	434
583	0x1368	OFDM_PROT_CFG	OFDM Protection Configuration	435
584	0x136C	MM20_PROT_CFG	Mixed Mode 20 MHz Protection Configuration	435
585	0x1370	MM40_PROT_CFG	Mixed Mode 40 MHz Protection Configuration	436
586	0x1374	GF20_PROT_CFG	Green Field 20 MHz Protection Configuration	437
587	0x1378	GF40_PROT_CFG	Green Field 40 MHz Protection Configuration	438
588	0x137C	EXP_CTS_TIME	Expected Clear to Send Time	439
589	0x1380	EXP_ACK_TIME	Expected Acknowledgement Time	439
590	0x1384	HT_FBK_TO_LEGACY	High Throughput Fallback To Legacy	439
591	0x1388	TX_MPDU_ADJ_INT	Tx MPDU Adjustment Interval	440
592	0x138C	TX_AMPDU_ADJ_INT	Tx A-MPDU Adjustment Interval	440

593	0x1390	TX_MPDU_UP_DOWN_THRES	Tx MPDU Upgrade Downgrade Threshold	441
594	0x1394	TX_AMPDU_UP_DOWN_THRES	Tx A-MPDU Upgrade Downgrade Threshold	441
595	0x1398	TX_FBK_LIMIT	Tx Fallback Limit	441
596	0x13A0	TX0_RF_GAIN_CORRECT	Tx0 RF Gain Correction	442
597	0x13A4	TX1_RF_GAIN_CORRECT	Tx1 RF Gain Correction	442
598	0x13A8	TX0_RF_GAIN_ATTEN	Tx0 RF Gain Attenuation	443
599	0x13AC	TX1_RF_GAIN_ATTEN	Tx1 RF Gain Correction	443
600	0x13B0	TX_ALC_CFG_0	Tx Automatic Level Control Configuration 0	444
601	0x13B4	TX_ALC_CFG_1	Tx Automatic Level Control Configuration 1	444
602	0x13B8	TX_ALC_DBG_1	Tx Automatic Level Control Debug 1	445
603	0x13C0	TX0_BB_GAIN_ATTEN	Tx0 Baseband Gain Attenuation	446
604	0x13C4	TX1_BB_GAIN_ATTEN	Tx1 Baseband Gain Attenuation	446
605	0x13C8	TX_ALC_VGA3	Tx Automatic Level Correction Variable Gain Amplifier 3	447
606	0x13CC	TX_AC_RTY_LIMIT	Tx Access Control Retry Limit	447
607	0x13D0	TX_AC_FBK_SPEED	Tx Access Control Fallback Speed	447
608	0x13EC	PIFS_TX_CFG	PCF Interframe Space Tx Configuration	448

2.22.10.2 Register Descriptions

554. EDCA_ACO_CFG (BE): (offset: 0x1300)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19:16	RW	ACO_CWMAX	Sets the maximum contention window for access category 0. $ACO\ CW_{max} = 2^{ACO_CWMAX}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x7
15:12	RW	ACO_CWMIN	Sets the minimum contention window for access category 0 as follows: $ACO\ CW_{min} = 2^{ACO_CWMIN}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x3
11:8	RW	ACO_AIFSN	Access Category 0 AIFSN (unit: slot time)	0x2
7:0	RW	ACO_TXOP	Access Category 0 Tx Opportunity Limit (unit: 32 μ s)	0x0

555. EDCA_AC1_CFG (BK): (offset: 0x1304)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19:16	RW	AC1_CWMAX	Sets the maximum contention window for access category 1 as follows: $AC1\ CW_{max} = 2^{AC1_CWMAX}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x7
15:12	RW	AC1_CWMIN	Sets the minimum contention window for access category 1 as follows: $AC1\ CW_{min} = 2^{AC1_CWMIN}$ 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x3
11:8	RW	AC1_AIFSN	Access Category 1 AIFSN (unit: slot time)	0x2
7:0	RW	AC1_TXOP	Access Category 1 Tx Opportunity Limit (unit: 32 μ s)	0x0

556. EDCA_AC2_CFG (VI): (offset: 0x1308)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19:16	RW	AC2_CWMAX	Sets the maximum contention window for access category 2 as follows: AC2 CWmax = 2^{AC2_CWMAX} 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x7
15:12	RW	AC2_CWMIN	Sets the minimum contention window for access category 2 as follows: AC2 CWmin = 2^{AC2_CWMIN} 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x3
11:8	RW	AC2_AIFSN	Access Category 2 AIFSN (unit: slot time)	0x2
7:0	RW	AC2_TXOP	Access Category 2 Tx Opportunity Limit (unit: 32 μ s)	0x0

557. EDCA_AC3_CFG (VO): (offset: 0x130C)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19:16	RW	AC3_CWMAX	Sets the maximum contention window for access category 3 as follows: AC3 CWmax = 2^{AC3_CWMAX} 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x7
15:12	RW	AC3_CWMIN	Sets the minimum contention window for access category 3 as follows: AC3 CWmin = 2^{AC3_CWMIN} 0: 1 1: 2 2: 4, and so on (unit: slot time)	0x3
11:8	RW	AC3_AIFSN	Access Category 3 AIFSN (unit: slot time)	0x2
7:0	RW	AC3_TXOP	Access Category 3 Tx Opportunity Limit (unit: 32 μ s)	0x0

558. EDCA_TID_AC_MAP: (offset: 0x1310)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
15:14	RW	TID7_AC_MAP	Traffic ID 7 Access Control Mapping Sets the AC value when TID=7.	0x3
13:12	RW	TID6_AC_MAP	Traffic ID 6 Access Control Mapping Sets the AC value when TID=6.	0x3
11:10	RW	TID5_AC_MAP	Traffic ID 5 Access Control Mapping Sets the AC value when TID=5.	0x2
9:8	RW	TID4_AC_MAP	Traffic ID 4 Access Control Mapping Sets the AC value when TID=4.	0x2
7:6	RW	TID3_AC_MAP	Traffic ID 3 Access Control Mapping Sets the AC value when TID=3.	0x0
5:4	RW	TID2_AC_MAP	Traffic ID 2 Access Control Mapping Sets the AC value when TID=2.	0x1
3:2	RW	TID1_AC_MAP	Traffic ID 1 Access Control Mapping Sets the AC value when TID=1.	0x1
1:0	RW	TID0_AC_MAP	Traffic ID 0 Access Control Mapping Sets the AC value when TID=0.	0x0

NOTE: Default according 802.11e Table 20.23—User priority to Access Category mappings.

559. TX_PWR_CFG_0: (offset: 0x1314)

Bits	Type	Name	Description	Initial Value
31:24	RW	TX_PWR_OFDM_12	Tx power for OFDM 12 Mbps/18 Mbps	0x0
23:16	RW	TX_PWR_OFDM_6	Tx power for OFDM 6 Mbps/9 Mbps	0x0
15:8	RW	TX_PWR_CCK_5	Tx power for CCK 5.5 Mbps/11 Mbps	0x0
7:0	RW	TX_PWR_CCK_1	Tx power for CCK 1 Mbps/2 Mbps	0x0

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

560. TX_PWR_CFG_1: (offset: 0x1318)

Bits	Type	Name	Description	Initial Value
31:24	RW	TX_PWR_MCS_2	Tx power for HT MCS=2, 3	0x0
23:16	RW	TX_PWR_MCS_0	Tx power for HT MCS=0, 1	0x0
15:8	RW	TX_PWR_OFDM_48	Tx power for OFDM 48 Mbps	0x0
7:0	RW	TX_PWR_OFDM_24	Tx power for OFDM 24 Mbps/36 Mbps.	0x0

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

561. TX_PWR_CFG_2: (offset: 0x131C)

Bits	Type	Name	Description	Initial Value
31:24	RW	TX_PWR_MCS_10	Tx power for HT MCS=10, 11	0x66
23:16	RW	TX_PWR_MCS_8	Tx power for HT MCS=8, 9	0x66
15:8	RW	TX_PWR_MCS_6	Tx power for HT MCS=6, 7	0x66
7:0	RW	TX_PWR_MCS_4	Tx power for HT MCS=4, 5	0x66

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

562. TX_PWR_CFG_3: (offset: 0x1320)

Bits	Type	Name	Description	Initial Value
31:24	RW	TX_PWR_STBC_2	Tx power for STBC MCS=2, 3	0x0
23:16	RW	TX_PWR_STBC_0	Tx power for STBC MCS=0, 1	0x0
15:8	RW	TX_PWR_MCS_14	Tx power for HT MCS=14	0x0
7:0	RW	TX_PWR_MCS_12	Tx power for HT MCS=12, 13	0x0

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

563. TX_PWR_CFG_4: (offset: 0x1324)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RW	TX_PWR_STBC_6	Tx power for STBC MCS=6	0x0
7:0	RW	TX_PWR_STBC_4	Tx power for STBC MCS=4, 5	0x0

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

564. TX_PWR_CFG_7: (offset: 0x13D4)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	TX_PWR_MCS_7	Tx power for HT MCS=7	0x0
15:8	-	-	Reserved	0x0
7:0	RW	TX_PWR_OFDM_54	Tx power for OFDM 54	0x0

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

565. TX_PWR_CFG_8: (offset: 0x13D8)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7:0	RW	TX_PWR_MCS_15	Tx power for HT MCS=15	0x0

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

566. TX_PWR_CFG_9: (offset: 0x13DC)

Bits	Type	Name	Description	Initial Value
31:8	-	-	Reserved	0x0
7	RW	TX_PWR_STBC_7	Tx power for STBC MCS=7	0x0

NOTE:

8-bit signed value (unit: 0.5 dB), valid range: -16 dB to 15.5 dB

567. TX_PIN_CFG: (offset: 0x1328)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:22	-	-	Reserved	0x0
21	RW	RFRX_POL	RF Receive Polarity Sets the polarity of the RF Rx.	0x0
20	RW	RFRX_EN	RF Receive Enable Enables RF Receiving	0x1
19	RW	TRSW_POL	Transmit Switch Polarity Sets the polarity of the antenna switch.	0x0
18	RW	TRSW_EN	Transmit Switch Enable Enables the antenna switch.	0x1
17	RW	RFTR_POL	RF Transmit Polarity Sets the polarity of the RF Tx.	0x0
16	RW	RFTR_EN	RF Transmit Enable Enables RF transmission.	0x1
15	RW	LNA_PE_G1_POL	2.4 GHz LNA Polarity Sets the polarity of the 2.4 GHz dual LNA on channel 1.	0x0
14	-	-	Reserved	0x0
13	RW	LNA_PE_G0_POL	2.4 GHz LNA Polarity Sets the polarity of the 2.4 GHz dual LNA on channel 0.	0x0
12	-	-	Reserved	0x0
11	RW	LNA_PE_G1_EN	2.4 GHz LNA Enable Enables the dual 2.4 GHz LNA on channel 1.	0x1
10	-	-	Reserved	0x1
9	RW	LNA_PE_G0_EN	2.4 GHz LNA Enable Enables the 2.4 GHz dual LNA on channel 0.	0x1
8	-	-	Reserved	0x1
7	RW	PA_PE_G1_POL	2.4 GHz Power Amplifier Polarity Sets the polarity of the 2.4 GHz power amplifier on channel 1.	0x0
6	-	-	Reserved	0x0
5	RW	PA_PE_G0_POL	2.4 GHz Power Amplifier Polarity Sets the polarity of the 2.4 GHz power amplifier on channel 0.	0x0
4	-	-	Reserved	0x0
3	RW	PA_PE_G1_EN	2.4 GHz Power Amplifier Enable Enables the 2.4 GHz power amplifier on channel 1.	0x1
2	-	-	Reserved	0x1
1	RW	PA_PE_G0_EN	2.4 GHz Power Amplifier Enable Enables the 2.4 GHz power amplifier on channel 0.	0x1
0	-	-	Reserved	0x1

NOTE: Where applicable,
0: Disable
1: Enable

0: Maintain original polarity settings.
1: Invert existing polarity settings.

568. TX_BAND_CFG: (offset: 0x132C)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	0x2
0	RW	TX_BAND_SEL	Tx Band Selection Selects the lower or upper 40 MHz band in 20 MHz Tx. 0: Use the lower 40 Mhz band. 1: Use the upper 40 Mhz band.	0x0

NOTE: TX_BAND_SEL is effective only when Tx/Rx bandwidth control register R4 of BBP is set to 40 Mhz.

569. TX_SW_CFG0: (offset: 0x1330)

Bits	Type	Name	Description	Initial Value
31:24	RW	DLY_RFTR_EN	Delay of RF Transmit Assertion Sets the delay period for assertion of the RF_TR interrupt, from when Tx begins, to when the interrupt is asserted.	0x2
23:16	RW	DLY_TRSW_EN	Delay of Transmit Switch Assertion Sets the delay period for assertion of the RF_TR interrupt, from when Tx is switched to Rx, or vice versa, to when the interrupt is asserted.	0x4
15:8	RW	DLY_PAPE_EN	Delay of PA_PE Interrupt Assertion Sets the delay period for assertion of the PA_PE interrupt, from when the power amplifier is turned on, to when the interrupt is asserted.	0x8
7:0	RW	DLY_TXPE_EN	Delay of TX_PE Interrupt Assertion Sets the delay period for assertion of the TX_PE interrupt, from when Tx is turned on, to when the interrupt is asserted.	0xC

NOTE:
The time unit for these delays is 0.25 μ s.

570. TX_SW_CFG1: (offset: 0x1334)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	DLY_RFTR_DIS	Delay of TX_PE Disassertion Sets the delay period for disassertion of the TX_PE interrupt, from when Tx is turned off, to when the interrupt is disasserted.	0xC

Bits	Type	Name	Description	Initial Value
15:8	RW	DLY_TRSW_DIS	Delay of TR_SW Disassertion Sets the delay period for disassertion of the TRSW interrupt, from when a switch between Rx and Tx occurs, to when the interrupt is disasserted.	0x8
7:0	RW	DLY_PAPE_DIS	Delay of PA_PE Disassertion Sets the delay period for dis-assertion of the PA_PE interrupt, from when the power amplifier is turned off, to when the interrupt is disasserted.	0x2

NOTE:

- 1: The time unit for these delays is 0.25 μ s.
- 2: The delay is started from TX_END event of BBP.
- 3: TX_PE is disasserted automatically when the last data byte is passed to BBP.

571. TX_SW_CFG2: (offset: 0x1338)

Bits	Type	Name	Description	Initial Value
31:24	RW	DLY_LNA_EN	Delay of LNA* Assertion Sets the delay period for assertion of the LNA* interrupt, from when the low noise amplifier is enabled, to when the interrupt is asserted.	0x0
23:16	RW	DLY_LNA_DIS	Delay of LNA* Disassertion Sets the delay period for disassertion of the LNA* interrupt, from when the low noise amplifier is disabled, to when the interrupt is disasserted.	0xC
15:8	RW	DLY_DAC_EN	Delay of DAC_PE Assertion Sets the delay period for assertion of the DAC interrupt, from when the digital-to-analog converter is enabled, to when the interrupt is asserted.	0x4
7:0	RW	DLY_DAC_DIS	Delay of DAC_PE Disassertion Sets the delay period for disassertion of the DAC interrupt, from when the digital-to-analog converter is disabled, to when the interrupt is disasserted.	0x8

NOTE:

1. The time unit for these delays is 0.25 μ s.
2. LNA* includes LNA_G0, LNA_G1.

572. TXOP_THRES_CFG: (offset: 0x133C)

Bits	Type	Name	Description	Initial Value
31:24	RW	TXOP_REM_THRES	Remaining TXOP Threshold When the remaining TXOP is below the threshold, the TXOP is passed silently.	0x0

Bits	Type	Name	Description	Initial Value
23:16	RW	CF_END_THRES	CF-END Threshold When the remaining TXOP is greater than the threshold, the CF-END is sent to release the remaining TXOP reserved by long NAV. 0xFF: Disable CF-END transmission.	0x0
15:8	RW	RDG_IN_THRES	Rx RDG Threshold When the remaining TXOP (specified in the duration field of the Rx frame with RDG=1) is greater than or equal to the threshold, the granted reverse direction TXOP may be used.	0x0
7:0	RW	RDG_OUT_THRES	Tx RDG Threshold When the remaining TXOP is greater than or equal to the threshold, RDG in the Tx frame is set to one.	0x0

NOTE:

The time unit for these thresholds is 32 μ s.

573. TXOP_CTRL_CFG: (offset: 0x1340)

Bits	Type	Name	Description	Initial Value
31:24	RW	EXT_CCA_MUTE	Extension CCA de-glitch time window (unit: μ sec)	0x0
23:21	-	-	Reserved	0x0
20	RW	ED_CCA_EN	Primary 20 ED/PD CCA blocking Tx 0: Disable 1: Enable	0x0
19:16	RW	EXT_CW_MIN	CWmin for Extension Channel Backoff When EXT_CCA_EN is enabled, 40 Mhz transmission is suppressed to 20 Mhz if the extension CCA is busy or extension channel backoff is not finished. Default: CWmin=0, disabled.	0x0
15:8	RW	EXT_CCA_DLY	Extension CCA Signal Delay Time Creates a delayed version of extension CCA signal reference time for extension channel IFS. Default: (OFDM SIFS) + (long slot time) = 16+20 = 36 (μ s) (unit: μ sec)	0x24
7	RW	EXT_CCA_EN	Extension CCA Reference Enable When transmitting in 40 Mhz mode, transmission is deferred until extension CCA is also clear. 0: Disable 1: Enable	0x0
6	RW	LSIG_TXOP_EN	L-SIG TXOP Protection Enable Enables extension of mixed mode L-SIG protection range to the following ACK/CTS.	0x0

Bits	Type	Name	Description	Initial Value
5:0	RW	TXOP_TRUN_EN	Enables TXOP truncation. Bit5: Reserved Bit4: Truncation for MIMO power save RTS/CTS Bit3: Truncation for user TXOP mode Bit2: Truncation for Tx rate group change Bit1: Truncation for AC change Bit0: TXOP timeout truncation 0: Disable 1: Enable	0x3F

574. TX_RTS_CFG: (offset: 0x1344)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
24	RW	RTS_FBK_EN	RTS rate fallback enable	0x0
23:8	RW	RTS_THRES	RTS Threshold MPDU or AMPDU with length greater than the RTS threshold are protected with an RTS/CTS exchange at the beginning of a TXOP. (unit: bytes)	0xFFFF
7:0	RW	RTS_RETRY_LIMIT	Auto RTS retry limit	0x7

575. TX_TIMEOUT_CFG: (offset: 0x1348)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
23:16	RW	TXOP_TIMEOUT	TXOP Timeout Value For TXOP Truncation NOTE: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: 15 μ s, used for a 20 μ s slot time. (unit: 1 μ s)	0xF
15:8	RW	RX_ACK_TIMEOUT	Rx ACK/CTS Timeout Value For Tx Procedure NOTE: It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT) Default: 10 μ s, used for a 20 μ s slot time. (unit: 1 μ s)	0xA
7:4	RW	MPDU_LIFE_TIME	Tx MPDU Expiration Time Expiration time = $2^{(9+MPDU_LIFE_TIME)}$ μ s Default value is $2^{(9+9)}$ $\approx$ 256 ms	0x9
3:0	-	-	Reserved	0x0

576. TX_RETRY_CFG: (offset: 0x134C)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
30	RW	TX_AUTOFB_EN	Tx Auto-Fallback Enable Enables auto-fallback of the PHY rate for retry Tx. 0: Disable 1: Enable	0x1
29	RW	AGG_RTY_MODE	A-MPDU Retry Mode Sets expiration of the A-MPDU retry mode. 0: Expired by retry limit 1: Expired by MPDU life timer	0x1
28	RW	NAG_RTY_MODE	Non-Aggregate MPDU Retry Mode Sets expiration of the non-aggregate MPDU retry mode. 0: Expired by retry limit 1: Expired by MPDU life timer	0x0
27:16	RW	LONG_RTY_THRES	Long retry threshold MPDU with length over this threshold is applied with long retry limit.	0xBB8
15:8	RW	LONG_RTY_LIMIT	Long retry limit	0x4
7:0	RW	SHORT_RTY_LIMIT	Short retry limit	0x7

577. TX_LINK_CFG: (offset: 0x1350)

Bits	Type	Name	Description	Initial Value
31:24	RO	REMOTE_MFS	Remote MCS feedback sequence number	-
23:16	RO	REMOTE_MFB	Remote MCS feedback	0x7F
15:13	-	-	Reserved	0x0
12	RW	TX_CFACK_EN	Enables Piggyback CF-ACK.	0x0
11	RW	TX_RDG_EN	Enables RDG Tx.	0x0
10	RW	TX_MRQ_EN	Enables MCS request Tx.	0x0
9	RW	REMOTE_UMFS_EN	Enables remote unsolicited MFB. 0: Do not apply remote unsolicited MFB (MFS=7) 1: Apply unsolicited MFB.	0x0
8	RW	TX_MFB_EN	Enables Tx apply remote MFB.	0x0
7:0	RW	REMOTE_MFB_LITETIME	Remote MFB lifetime (unit: 32 μ s)	0x20

NOTE: Where applicable,
0: Disable
1: Enable

578. HT_FBK_CFG0: (offset: 0x1354)

Bits	Type	Name	Description	Initial Value
31:28	RW	HT_MCS7_FBK	Auto-fallback MCS when HT MCS =7	0x6
27:24	RW	HT_MCS6_FBK	Auto-fallback MCS when HT MCS =6	0x5

Bits	Type	Name	Description	Initial Value
23:20	RW	HT_MCS5_FBK	Auto-fallback MCS when HT MCS =5	0x4
19:16	RW	HT_MCS4_FBK	Auto-fallback MCS when HT MCS =4	0x3
15:12	RW	HT_MCS3_FBK	Auto-fallback MCS when HT MCS =3	0x2
11:8	RW	HT_MCS2_FBK	Auto-fallback MCS when HT MCS =2	0x1
7:4	RW	HT_MCS1_FBK	Auto-fallback MCS when HT MCS =1	0x0
3:0	RW	HT_MCS0_FBK	Auto-fallback MCS when HT MCS =0	0x0

579. HT_FBK_CFG1: (offset: 0x1358)

Bits	Type	Name	Description	Initial Value
31:28	RW	HT_MCS15_FBK	Auto-fallback MCS when HT MCS =15	0xE
27:24	RW	HT_MCS14_FBK	Auto-fallback MCS when HT MCS =14	0xD
23:20	RW	HT_MCS13_FBK	Auto-fallback MCS when HT MCS =13	0xC
19:16	RW	HT_MCS12_FBK	Auto-fallback MCS when HT MCS =12	0xB
15:12	RW	HT_MCS11_FBK	Auto-fallback MCS when HT MCS =11	0xA
11:8	RW	HT_MCS10_FBK	Auto-fallback MCS when HT MCS =10	0x9
7:4	RW	HT_MCS9_FBK	Auto-fallback MCS when HT MCS =9	0x8
3:0	RW	HT_MCS8_FBK	Auto-fallback MCS when HT MCS =8	0x8

NOTE:

1. The MCS is a fallback stopping state, when the fallback MCS is the same as the current MCS.
2. HT Tx PHY rates will not fall back to legacy PHY rates.

580. LG_FBK_CFG0: (offset: 0x135C)

Bits	Type	Name	Description	Initial Value
31:28	RW	OFDM7_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 54 Mbps.	0xE
27:24	RW	OFDM6_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 48 Mbps.	0xD
23:20	RW	OFDM5_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 36 Mbps.	0xC
19:16	RW	OFDM4_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 24 Mbps.	0xB
15:12	RW	OFDM3_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 18 Mbps.	0xA
11:8	RW	OFDM2_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 12 Mbps.	0x9
7:4	RW	OFDM1_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 9 Mbps.	0x8
3:0	RW	OFDM0_FBK	Auto-fallback MCS when the previous Tx rate is OFDM 6 Mbps.	0x8

581. LG_FBK_CFG1: (offset: 0x1360)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:12	RW	CCK3_FBK	Auto-fallback MCS when the previous Tx rate is CCK 11 Mbps.	0x2
11:8	RW	CCK2_FBK	Auto-fallback MCS when the previous Tx rate is CCK 5.5 Mbps.	0x1
7:4	RW	CCK1_FBK	Auto-fallback MCS when the previous Tx rate is CCK 2 Mbps.	0x0
3:0	RW	CCK0_FBK	Auto-fallback MCS when the previous Tx rate is CCK 1 Mbps.	0x0

NOTE. Set CCK or OFDM by setting bit3 of each legacy fallback rate.

0: Enable CCK

1: Enable OFDM

582. CCK_PROT_CFG: (offset: 0x1364)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	CCK_RTSTH_EN	CCK RTS Threshold Enable Enables RTS threshold on CCK Tx. 0: Disable 1: Enable	0x0
25:20	RW	CCK_TXOP_ALLOW	CCK Protection TXOP Sets the transmission mode for CCK TXOP. Bit25: Allow GF 40 MHz Tx Bit24: Allow GF 20 MHz Tx Bit23: Allow MM 40 MHz Tx Bit22: Allow MM 20 MHz Tx Bit21: Allow OFDM Tx Bit20: Allow CCK Tx 0: Disallow 1: Allow	0x1
19:18	RW	CCK_PROT_NAV	CCK Protection NAV Sets the TXOP protection type for CCK Tx. 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	CCK_PROT_CTRL	CCK Protection Control Sets the protection control frame type for CCK TX Tx. 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0

Bits	Type	Name	Description	Initial Value
15:0	RW	CCK_PROT_RATE	CCK Protection Rate Sets the protection control frame rate for CCK Tx, including RTS, CTS-to-self, and CF-END. Default: CCK 11 Mbps	0x3

583. OFDM_PROT_CFG: (offset: 0x1368)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	OFDM_RTSTH_EN	OFDM RTS Threshold Enable Enables RTS threshold on OFDM Tx. 0: Disable 1: Enable	0x0
25:20	RW	OFDM_PROT_TXOP	OFDM Protection TXOP Sets the transmission mode for OFDM TXOP. Bit25: Allow GF 40 MHz Tx. Bit24: Allow GF 20 MHz Tx. Bit23: Allow MM 40 MHz Tx. Bit22: Allow MM 20 MHz Tx. Bit21: Allow OFDM Tx. Bit20: Allow CCK Tx. 0: Disallow 1: Allow	0x2
19:18	RW	OFDM_PROT_NAV	OFDM Protection NAV Sets the TXOP protection type for OFDM Tx. 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	OFDM_PROT_CTRL	OFDM Protection Control Sets the protection control frame type for OFDM Tx. 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	OFDM_PROT_RATE	OFDM Protection Rate Sets the protection control frame rate for OFDM Tx, including RTS, CTS-to-self, and CF-END. Default: CCK 11 Mbps	0x3

584. MM20_PROT_CFG: (offset: 0x136C)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
26	RW	MM20_RTSTH_EN	Mixed Mode 20 MHz RTS Threshold Enable Enables RTS threshold in 20 MHz mixed mode Tx. 0: Disable 1: Enable	0x0
25:20	RW	MM20_PROT_TXOP	Mixed Mode 20 MHz Protection TXOP Sets the transmission mode for MM-20 TXOP. Bit25: Allow GF 40 MHz Tx. Bit24: Allow GF 20 MHz Tx. Bit23: Allow MM 40 MHz Tx. Bit22: Allow MM 20 MHz Tx. Bit21: Allow OFDM Tx. Bit20: Allow CCK Tx. 0: Disallow 1: Allow	0x4
19:18	RW	MM20_PROT_NAV	Mixed Mode 20 MHz Protection NAV Sets the TXOP protection type for MM 20 MHz Tx. 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	MM20_PROT_CTRL	Mixed Mode 20 MHz Protection Control Sets the protection control frame type for MM 20 MHz Tx. 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	MM20_PROT_RATE	Mixed Mode 20 MHz Protection Rate Sets the protection control frame rate for MM 20 MHz Tx, including RTS, CTS-to-self, and CF-END. Default: OFDM 24 Mbps	0x4004

585. MM40_PROT_CFG: (offset: 0x1370)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	MM40_RTSTH_EN	Mixed Mode 40 MHz RTS Threshold Enable Enables RTS threshold on MM 40 MHz Tx. 0: Disable 1: Enable	0x0

Bits	Type	Name	Description	Initial Value
25:20	RW	MM40_PROT_TXOP	Mixed Mode 40 MHz Protection TXOP Sets the transmission mode for MM40 TXOP. Bit25: Allow GF 40 MHz Tx. Bit24: Allow GF 20 MHz Tx. Bit23: Allow MM 40 MHz Tx. Bit22: Allow MM 20 MHz Tx. Bit21: Allow OFDM Tx. Bit20: Allow CCK Tx. 0: Disallow 1: Allow	0x8
19:18	RW	MM40_PROT_NAV	Mixed Mode 40 MHz Protection NAV Sets the TXOP protection type for MM 40 MHz Tx. 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	MM40_PROT_CTRL	Mixed Mode 40 MHz Protection Control Sets the protection control frame type for MM 40 MHz Tx. 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	MM40_PROT_RATE	Mixed Mode 40 MHz Protection Rate Protection control frame rate for MM40 Tx (Including RTS/CTS-to-self/CF-END) Default: Duplicate OFDM 24 Mbps	0x4084

586. GF20_PROT_CFG: (offset: 0x1374)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	GF20_RTSTH_EN	Green Field 20 MHz RTS Threshold Enable Enables RTS threshold on GF 20 MHz Tx. 0: Disable 1: Enable	0x0
25:20	RW	GF20_PROT_TXOP	Green Field 20 MHz Protection TXOP Sets the transmission mode for GF20 TXOP. Bit25: Allow GF 40 MHz Tx. Bit24: Allow GF 20 MHz Tx. Bit23: Allow MM 40 MHz Tx. Bit22: Allow MM 20 MHz Tx. Bit21: Allow OFDM Tx. Bit20: Allow CCK Tx. 0: Disallow 1: Allow	0x10

Bits	Type	Name	Description	Initial Value
19:18	RW	GF20_PROT_NAV	Green Field 20 MHz Protection NAV Sets the TXOP protection type for GF 20 MHz Tx. 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0
17:16	RW	GF20_PROT_CTRL	Green Field 20 MHz Protection Control Sets the protection control frame type for GF 20 MHz Tx. 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	GF20_PROT_RATE	Green Field 20 MHz Protection Rate Sets the protection control frame rate for GF20 Tx, including RTS, CTS-to-self, and CF-END. Default: OFDM 24 Mbps	0x4004

587. GF40_PROT_CFG: (offset: 0x1378)

Bits	Type	Name	Description	Initial Value
31:27	-	-	Reserved	0x0
26	RW	GF40_RTSTH_EN	Green Field 40 MHz RTS Threshold Enable Enables RTS threshold on GF 40 MHz Tx. 0: Disable 1: Enable	0x0
25:20	RW	GF40_PROT_TXOP	Green Field 40 MHz Protection TXOP Sets the transmission mode for GF40 TXOP. Bit25: Allow GF 40 MHz Tx. Bit24: Allow GF 20 MHz Tx. Bit23: Allow MM 40 MHz Tx. Bit22: Allow MM 20 MHz Tx. Bit21: Allow OFDM Tx. Bit20: Allow CCK Tx. 0: Disallow 1: Allow	0x20
19:18	RW	GF40_PROT_NAV	Green Field 40 MHz Protection NAV Sets the TXOP protection type for GF 40 MHz Tx. 0: None 1: Short NAV protection 2: Long NAV protection 3: Reserved (None)	0x0

Bits	Type	Name	Description	Initial Value
17:16	RW	GF40_PROT_CTRL	Green Field 40 MHz Protection Control Sets the protection control frame type for GF 40 MHz Tx. 0: None 1: RTS/CTS 2: CTS-to-self 3: Reserved (None)	0x0
15:0	RW	GF40_PROT_RATE	Green Field 40 MHz Protection Rate Sets the protection control frame rate for GF 40 Tx, including RTS, CTS-to-self , and CF-END. Default: Duplicate OFDM 24 Mbps	0x4084

588. EXP_CTS_TIME: (offset: 0x137C)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30:16	RW	EXP_OFDM_CTS_TIME	Expected OFDM CTS Time Sets the expected time for OFDM CTS response. Used for outgoing NAV setting. Default: SIFS + 6 Mbps CTS (unit: 1 μ s)	0x38
15	-	-	Reserved	0x0
14:0	RW	EXP_CCK_CTS_TIME	Expected CCK CTS Time Sets the expected time for CCK CTS response. Used for outgoing NAV setting. Default: SIFS + 1 Mbps CTS (unit: 1 μ s)	0x13A

589. EXP_ACK_TIME: (offset: 0x1380)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x0
30:16	RW	EXP_OFDM_ACK_TIME	Expected OFDM ACK Time Sets the expected time for OFDM ACK response. Used for outgoing NAV setting. Default: SIFS + 6 Mbps ACK preamble (unit: 1 μ s)	0x24
15	-	-	Reserved	0x0
14:0	RW	EXP_CCK_ACK_TIME	Expected CCK ACK Time Sets the expected time for OFDM ACK response. Used for outgoing NAV setting. Default: SIFS + 1 Mbps ACK preamble (unit: 1 μ s)	0xCA

590. HT_FBK_TO_LEGACY: (offset: 0x1384)

Bits	Type	Name	Description	Initial Value
31:13	-	-	Reserved	0x0

Bits	Type	Name	Description	Initial Value
12	RW	RTS_FBK_TO_LEGACY_EN	RTS Fallback To Legacy Enable Enables RTS Tx rate fallback to legacy OFDM/CCK. 0: Disable 1: Enable	0x0
11:8	RW	RTS_FBK_TO_LEGACY_RATE	RTS Fallback To Legacy Rate Sets the target legacy OFDM/CCK rate for RTS when a fallback from MCS0 occurs. Bit3: 0: CCK, 1, OFDM Bit[2:0]: Legacy MCS	0x0
7:5	-	-	Reserved	0x0
4	RW	HT_FBK_TO_LEGACY_EN	HT Fallback To Legacy Enable Enables Tx rate fallback from HT/VHT to legacy OFDM/CCK. 0: Disable 1: Enable	0x0
3:0	RW	HT_FBK_TO_LEGACY_RATE	HT Fallback To Legacy Rate Sets the target legacy OFDM/CCK rate for HT/VHT when a fallback from MCS0 occurs. Bit3: 0: CCK, 1, OFDM Bit[2:0]: Legacy MCS	0x0

591. TX_MPDU_ADJ_INT: (offset: 0x1388)

Bits	Type	Name	Description	Initial Value
31:24	RW	TX_MPDU_ADJ_INT3	MPDU Tx Rate Adjustment Interval at Tx Fallback Level 3 (unit: number of MPDU)	0x1
23:16	RW	TX_MPDU_ADJ_INT2	MPDU Tx Rate Adjustment Interval at Tx Fallback Level 2 (unit: number of MPDU)	0x1
15:8	RW	TX_MPDU_ADJ_INT1	MPDU Tx Rate Adjustment Interval at Tx Fallback Level 1 (unit: number of MPDU)	0x1
7:0	RW	TX_MPDU_ADJ_INT0	MPDU Tx Rate Adjustment Interval at Tx Fallback Level 0 (unit: number of MPDU)	0x1

592. TX_AMPDU_ADJ_INT: (offset: 0x138C)

Bits	Type	Name	Description	Initial Value
31:24	RW	TX_AMPDU_ADJ_INT3	AMPDU Tx Rate Adjustment Interval at Tx Fallback Level 3 (unit: number of MPDU)	0x1
23:16	RW	TX_AMPDU_ADJ_INT2	AMPDU Tx Rate Adjustment Interval at Tx Fallback Level 2 (unit: number of MPDU)	0x1

Bits	Type	Name	Description	Initial Value
15:8	RW	TX_AMPDU_ADJ_INT1	AMPDU Tx Rate Adjustment Interval at Tx Fallback Level 1 (unit: number of MPDU)	0x1
7:0	RW	TX_AMPDU_ADJ_INT0	AMPDU Tx Rate Adjustment Interval at Tx Fallback Level 0 (unit: number of MPDU)	0x1

593. TX_MPDU_UP_DOWN_THRES: (offset: 0x1390)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24:16	RW	TX_MPDU_UP_THRES	Tx AMPDU Upgrade Threshold Sets the MPDU Tx fallback level upgrade threshold, based on the packet error rate. (unit: 1/256 % of total Tx packets)	0x100
15:9	-	-	Reserved	0x0
8:0	RW	TX_MPDU_DOWN_THRES	Tx AMPDU Downgrade Threshold MPDU TX fallback level downgrade threshold, based on the packet error rate. (unit: 1/256 % of total Tx packets)	0x0

594. TX_AMPDU_UP_DOWN_THRES: (offset: 0x1394)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24:16	RW	TX_AMPDU_UP_THRES	Tx AMPDU Upgrade Threshold Sets the AMPDU Tx fallback level upgrade threshold threshold, based on the packet error rate. (unit: 1/256 % of total Tx packets)	0x1
15:9	-	-	Reserved	0x0
8:0	RW	TX_AMPDU_DOWN_THRES	Tx AMPDU Downgrade Threshold Sets the AMPDU TX fallback level downgrade threshold, based on the packet error rate.(unit: 1/256 % of total Tx packets)	0x0

595. TX_FBK_LIMIT: (offset: 0x1398)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RW	MULTI_MAC_ADDRESS	Multiple MAC Addresses Use per WCID lookup table WCID112-WCID127 for 16 additional MAC addresses. 0: Disable 1: Enable	0x0

Bits	Type	Name	Description	Initial Value
18	RW	TX_RATE_LUT_EN	Tx Rate Lookup Table Enable Copies the Tx rate from per WCID lookup table when TXWI.TXLUT is also set to 1. 0: Disable 1: Enable	0x0
17	RW	TX_AMPDU_UP_CLEAR	Tx A-MPDU Upgrade Clear Sets A-MPDU to directly upgrade to level 0. 0: Disable 1: Enable	0x1
16	RW	TX_MPDU_UP_CLEAR	Tx MPDU Upgrade Clear Sets MPDU to directly upgrade to level 0. 0: Disable 1: Enable	0x1
15:8	RW	TX_AMPDU_FBK_LIMIT	AMPDU Tx Fallback Level Limit (unit: # of levels)	0x10
7:0	RW	TX_MPDU_FBK_LIMIT	MPDU Tx Fallback Level Limit (unit: # of levels)	0x10

596. TX0_RF_GAIN_CORRECT: (offset: 0x13A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x00
29:24	RW	GAIN_CORR_3	Gain Correction 3 Tx0 Gain Correction when RF_ALC[3:2]==3. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00
23:22	-	-	Reserved	0x00
21:16	RW	GAIN_CORR_2	Gain Correction 2 Tx0 Gain Correction when RF_ALC[3:2]==2. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00
15:14	-	-	Reserved	0x00
13:8	RW	GAIN_CORR_1	Gain Correction 1 Tx0 Gain Correction when RF_ALC[3:2]==1. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00
7:6	-	-	Reserved	0x00
5:0	RW	GAIN_CORR_0	Gain Correction 0 Tx0 Gain Correction when RF_ALC[3:2]==0. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00

597. TX1_RF_GAIN_CORRECT: (offset: 0x13A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x00
29:24	RW	GAIN_CORR_3	Gain Correction 3 Tx1 Gain Correction when RF_ALC[3:2]==3. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00
23:22	-	-	Reserved	0x00

Bits	Type	Name	Description	Initial Value
21:16	RW	GAIN_CORR_2	Gain Correction 2 Tx1 Gain Correction when RF_ALC[3:2]==2. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00
15:14	-	-	Reserved	0x00
13:8	RW	GAIN_CORR_1	Gain Correction 1 Tx1 Gain Correction when RF_ALC[3:2]==1. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00
7:6	-	-	Reserved	0x00
5:0	RW	GAIN_CORR_0	Gain Correction 0 Tx1 Gain Correction when RF_ALC[3:2]==0. Unit: 0.1 dB, Range: -3.2 dB to 3.1 dB	0x00

598. TX0_RF_GAIN_ATTEN: (offset: 0x13A8, default: 0x6C6C_6C6C)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x00
30:24	RW	RF_GAIN_ATTEN_3	Tx0 RF Gain Attenuation Level 3 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C
23	-	-	Reserved	0x00
22:16	RW	RF_GAIN_ATTEN_2	Tx0 RF Gain Attenuation Level 2 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C
15	-	-	Reserved	0x00
14:8	RW	RF_GAIN_ATTEN_1	Tx0 RF Gain Attenuation Level 1 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C
7	-	-	Reserved	0x00
6:0	RW	RF_GAIN_ATTEN_0	Tx0 RF Gain Attenuation Level 0 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C

599. TX1_RF_GAIN_ATTEN: (offset: 0x13AC, default: 0x6C6C_6C6C)

Bits	Type	Name	Description	Initial Value
31	-	-	Reserved	0x00
30:24	RW	RF_GAIN_ATTEN_3	Tx1 RF Gain Attenuation Level 3 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C
23	-	-	Reserved	0x00
22:16	RW	RF_GAIN_ATTEN_2	Tx1 RF Gain Attenuation Level 2 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C
15	-	-	Reserved	0x00

Bits	Type	Name	Description	Initial Value
14:8	RW	RF_GAIN_ATTEN_1	Tx1 RF Gain Attenuation Level 1 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C
7	-	-	Reserved	0x00
6:0	RW	RF_GAIN_ATTEN_0	Tx1 RF Gain Attenuation Level 0 Format: 7-bit, signed value Unit: 0.5 dB, Range: -20 dB to -5 dB	0x6C

600. TX_ALC_CFG_0: (offset: 0x13B0, default: 0x2F2F_1B1B)

Bits	Type	Name	Description	Initial Value
31:30	-	-	Reserved	0x00
29:24	RW	TX_ALC_LIMIT_1	Tx1 ALC Upper limit Format: 6-bit, unsigned value Unit: 0.5 dB, Range: 0 to 23.5 dB	0x2F
23:22	-	-	Reserved	0x00
21:16	RW	TX_ALC_LIMIT_0	Tx0 ALC Upper limit Format: 6-bit, unsigned value Unit: 0.5 dB, Range: 0 to 23.5 dB	0x2F
15:14	-	-	Reserved	0x00
13:8	RW	TX_ALC_CH_INIT_1	Tx1 channel initial transmission gain Format: 6-bit, unsigned value Unit: 0.5 dB, Range: 0 to 23.5 dB	0x1B
7:6	-	-	Reserved	0x00
5:0	RW	TX_ALC_CH_INIT_0	Tx0 channel initial transmission gain Format: 6-bit, unsigned value Unit: 0.5 dB, Range: 0 to 23.5 dB	0x1B

601. TX_ALC_CFG_1: (offset: 0x13B4, default: 0xC954_0000)

Bits	Type	Name	Description	Initial Value
31	RW	ROS_BUSY_EN	Rx Offset (ROS) Calibration Busy Enable Defers the Tx procedure if ROS calibration is busy. 0: Disable 1: Enable	0x01
30	RW	RF_TOS_ENABLE	RF Tx Offset (TOS) Calibration Enable 0: Disable 1: Enable	0x01
29:24	RW	RF_TOS_TIMEOUT	RF TOS Timeout Sets the time-out value for RF_TOS_ENABLE de-assertion if RF_TOS_DONE is missing. (unit: 0.25 μ sec)	0x09

Bits	Type	Name	Description	Initial Value
23:22	RW	TX1_RF_GAIN_ATTEN	Tx1 RF Gain Attenuation Mode Sets the Tx1 RF gain attenuation according to settings available in the TX1_RF_GAIN_ATTEN (offset: 0x13A8) register. 0: Applies RF_GAIN_ATTEN_0 (bit[6:0]) settings. 1: Applies RF_GAIN_ATTEN_1 (bit[14:8]) settings. 2: Applies RF_GAIN_ATTEN_2 (bit[22:16]) settings. 3: Applies RF_GAIN_ATTEN_3 (bit[30:24]) settings.	0x1
21:20	RW	TX0_RF_GAIN_ATTEN	Tx0 RF Gain Attenuation Mode Sets the Tx0 RF gain attenuation according to settings available in the TX0_RF_GAIN_ATTEN (offset: 0x13AC) register. 0: Applies RF_GAIN_ATTEN_0 (bit[6:0]) settings. 1: Applies RF_GAIN_ATTEN_1 (bit[14:8]) settings. 2: Applies RF_GAIN_ATTEN_2 (bit[22:16]) settings. 3: Applies RF_GAIN_ATTEN_3 (bit[30:24]) settings.	0x1
19	-	-	Reserved	0x0
18:16	RW	RF_TOS_DLY	RF TOS Enable Sets the RF_TOS_EN assertion delay after de-assertion of PA_PE. (unit: 0.25 μ sec)	0x04
15:12	RW	TX1_GAIN_FINE	TX1 Gain Fine Adjustment Format: 4-bit, signed value Unit: 0.1 dB, Range: -0.8 dB to 0.7 dB	0x00
11:8	RW	TX0_GAIN_FINE	TX0 Gain Fine Adjustment Format: 4-bit, signed value Unit: 0.1 dB, Range: -0.8 dB to 0.7 dB	0x00
7:6	-	-	Reserved	0x00
5:0	RW	TX_TEMP_COMP	Tx Power Temperature Compensation Format: 6-bit, signed value Unit: 0.5 dB, Range: -10 dB to 10 dB	0x00

602. TX_ALC_DBG_1: (offset: 0x13B8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
15	-	-	Reserved	0x00
14	RW	TX_ALC_ADJ_DBG_EN	Tx ALC Adjustment Debug Enable 0: Disable 1: Enable	0x00
13:8	RW	TX_ALC_ADJ_DBG	Tx ALC Adjustment Debug Value	0x00
7:6	-	-	Reserved	0x00

Bits	Type	Name	Description	Initial Value
5	RW	RF_GAINATT_DBG	Tx ALC RF Gain Attenuation Debug Value Applied to RF when TX_ALC_RF_DBG_EN is set to 1.	0x00
4	RW	TX_ALC_RF_DBG_EN	Tx ALC RF Control Pin Debug Enable 0: Disable 1: Enable	0x00
3:0	RW	TX_ALC_RF_DBG	Tx ALC RF TX Power Debug Value Applied to RF when TX_ALC_RF_DBG_EN is set to 1.	0x00

603. TX0_BB_GAIN_ATTEN: (offset: 0x13C0, default: 0x1818_1818)

Bits	Type	Name	Description	Initial Value
31:29	-	-	Reserved	0x00
28:24	RW	BB_GAIN_ATTEN_3	Tx0 Baseband Gain Attenuation Level 3 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18
23:21	-	-	Reserved	0x00
20:16	RW	BB_GAIN_ATTEN_2	Tx0 Baseband Gain Attenuation Level 2 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18
15:13	-	-	Reserved	0x00
12:8	RW	BB_GAIN_ATTEN_1	Tx0 Baseband Gain Attenuation Level 1 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18
7:5	-	-	Reserved	0x00
4:0	RW	BB_GAIN_ATTEN_0	Tx0 Baseband Gain Attenuation Level 0 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18

604. TX1_BB_GAIN_ATTEN: (offset: 0x13C4, default: 0x1818_1818)

Bits	Type	Name	Description	Initial Value
31:29	-	-	Reserved	0x00
28:24	RW	BB_GAIN_ATTEN_3	Tx1 Baseband Gain Attenuation Level 3 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18
23:21	-	-	Reserved	0x00
20:16	RW	BB_GAIN_ATTEN_2	Tx1 Baseband Gain Attenuation Level 2 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18
15:13	-	-	Reserved	0x00
12:8	RW	BB_GAIN_ATTEN_1	Tx1 Baseband Gain Attenuation Level 1 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18
7:5	-	-	Reserved	0x00

Bits	Type	Name	Description	Initial Value
4:0	RW	BB_GAIN_ATTEN_0	Tx1 Baseband Gain Attenuation Level 0 Format: 5-bit, signed value Unit: 0.5 dB, Range: -8 dB to 7 dB	0x18

605. TX_ALC_VGA3: (offset: 0x13C8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:29	-	-	Reserved	0x00
28:24	RW	TX1_ALC_VGA2	Tx1 ALC VGA 2 Gain reduction from 6 dB for TX1.ALC[3:2] = 2 Format: 5-bit, un-signed value Unit: 0.5 dB, Range: 0-6 dB	0x00
23:21	-	-	Reserved	0x00
20:16	RW	TX0_ALC_VGA2	Tx0 ALC VGA 2 Gain reduction from 6 dB for TX0.ALC[3:2] = 2 Format: 5-bit, un-signed value Unit: 0.5 dB, Range: 0-6 dB	0x00
15:13	-	-	Reserved	0x00
12:8	RW	TX1_ALC_VGA3	Tx1 ALC VGA 3 Gain reduction from 6 dB for TX1.ALC[3:2] = 3 Format: 5-bit, un-signed value Unit: 0.5 dB, Range: 0-6 dB	0x00
7:5	-	-	Reserved	0x00
4:0	RW	TX0_ALC_VGA3	Tx0 ALC VGA 3 Gain reduction from 6 dB for TX0.ALC[3:2] = 3 Format: 5-bit, un-signed value Unit: 0.5 dB, Range: 0-6 dB	0x00

606. TX_AC_RTY_LIMIT: (offset: 0x13CC)

Bits	Type	Name	Description	Initial Value
31:24	RW	TX_AC3_RTY_LIMIT	AC3 OoS-Data Frame Tx Retry Limit	0x7
23:16	RW	TX_AC2_RTY_LIMIT	AC2 OoS-Data Frame Tx Retry Limit	0x7
15:8	RW	TX_AC1_RTY_LIMIT	AC1 OoS-Data Frame Tx Retry Limit	0x7
7:0	RW	TX_AC0_RTY_LIMIT	AC0 OoS-Data Frame Tx Retry Limit	0x7

607. TX_AC_FBK_SPEED: (offset: 0x13D0)

Bits	Type	Name	Description	Initial Value
31:2	-	-	Reserved	0x0
1	RW	TX_AC_FBK_SPEED_EN	Tx AC Fallback Speed Enable Applies per AC Tx fallback speed parameters. 0: Disable 1: Enable	0x0

Bits	Type	Name	Description	Initial Value
0	RW	TX_AC_RETRY_LIMIT_EN	Tx AC Retry Limit Enable Applies per AC Tx retry limit parameters. 0: Disable 1: Enable	0x0

608. PIFS_TX_CFG: (offset: 0x13EC)

Bits	Type	Name	Description	Initial Value
31:20	-	-	Reserved	0x0
19	RW	PIFS_REV_TX_FORCE	Force PIFS Reverse Tx Forces per packet PIFS reverse Tx mode, and ignores the TXWI.PIFSTX bit. 0: Disable 1: Enable	0x0
18	RW	PIFS_REV_TX_EN	Enable PIFS Reverse Tx Mode 0: Disable 1: Enable	0x1
17:16	RW	PIFS_REV_TX_SLOT	PIFS Reverse Tx Slot Count	0x2
15:0	RW	PIFS_REV_TX_THRES	PIFS Reverse Tx Threshold Only AMPDU/MPDU with length less than this threshold is able to do PIFS reverse direction Tx after a successful ACK transmission.	0x7D0

2.22.11 MAC Rx Configuration Registers (base: 0x1018_0000)

2.22.11.1 List of Registers

No.	Offset	Register Name	Description	Page
609	0x1400	RX_FILTR_CFG	Receive Filter Configuration	450
610	0x1404	AUTO_RSP_CFG	Auto-Respond Configuration	450
611	0x1408	LEGACY_BASIC_RATE	Legacy Basic Rate	451
612	0x140C	HT_BASIC_RATE	High Throughput Basic Rate	451
613	0x1410	HT_CTRL_CFG	High Throughput Control Configuration	451
614	0x1414	SIFS_COST_CFG	Short Inter-Frame Space Configuration	452
615	0x1418	RX_PARSER_CFG	Receive Parser Configuration	452
616	0x147C	MAC_ADDR_EXT_EN	Extended MAC Address Enable	452
617	0x1480	MAC_ADDR_EXT0_31_0	Extended MAC Address0 bit[31:0]	453
618	0x1484	MAC_ADDR_EXT0_47_32	Extended MAC Address0 bit[47:32]	453
...	...	...	...	
647	0x14F8	MAC_ADDR_EXT15_31_0	Extended MAC Address15 bit[31:0]	456
648	0x14FC	MAC_ADDR_EXT15_47_32	Extended MAC Address15 bit[47:32]	456

2.22.11.2 Register Descriptions

609. RX_FILTR_CFG: (offset: 0x1400)

Bits	Type	Name	Description	Initial Value
31:17	-	-	Reserved	0x0
16	RW	DROP_CTRL_RSV	Drops reserve control subtype.	0x1
15	RW	DROP_BAR	Drops BAR frames.	0x0
14	RW	DROP_BA	Drops BA frames.	0x1
13	RW	DROP_PSPOLL	Drops PS-Poll frames.	0x0
12	RW	DROP_RTS	Drops RTS frames.	0x1
11	RW	DROP_CTS	Drops CTS frames.	0x1
10	RW	DROP_ACK	Drops ACK frames.	0x1
9	RW	DROP_CFEND	Drops CF-END frames.	0x1
8	RW	DROP_CFACK	Drops CF-END + CF-ACK frames.	0x1
7	RW	DROP_DUPL	Drops duplicated frames.	0x1
6	RW	DROP_BC	Drops broadcast frames.	0x0
5	RW	DROP_MC	Drops multicast frames.	0x0
4	RW	DROP_VER_ERR	Drops frames with 802.11 version errors.	0x1
3	RW	DROP_NOT_MYBSS	Drops frames that are not my BSSID	0x1
2	RW	DROP_UC_NOME	Drops not to me unicast frames	0x1
1	RW	DROP_PHY_ERR	Drops frames with physical errors.	0x1
0	RW	DROP_CRC_ERR	Drops frames with CRC errors.	0x1

NOTE:

0: Disable

1: Enable

610. AUTO_RSP_CFG: (offset: 0x1404)

Bits	Type	Name	Description	Initial Value
31:9	-	-	Reserved	0x0
8	RW	CTS_BYPASS_EXTCCA	Duplicate legacy CTS response bypass extension CCA check	0x0
7	RW	CTRL_PWR_BIT	Control Power Bit Sets the power bit value in the control frame.	0x0
6	RW	BAC_ACK_POLICY	BAC ACK Policy BA frame → BAC → ACK policy bit value	0x0
5	RW	CTRL_WRAP_EN	Control Wrapper Enable Enables an ACK/CTS control wrapper frame auto-response.	0x0
4	RW	CCK_SHORT_EN	CCK Short Preamble Enable Enables a CCK short preamble auto-response.	0x0

Bits	Type	Name	Description	Initial Value
3	RW	CTS_40M_REF	CTS Legacy Reference When in duplicate legacy CTS response mode, this bit enables the use of the extension CCA signal to decide whether to duplicate or not.	0x0
2	RW	CTS_40M_MODE	CTS Legacy Response Enable Enables duplicate legacy CTS response mode.	0x0
1	RW	BAC_ACKPOLICY_EN	BAC ACK Policy Enable Enables the BAC ACK policy bit. When enabled, there is no BA auto response upon receiving a BAR with no ACK policy.	0x1
0	RW	AUTO_RSP_EN	Auto responder Enable	0x1

NOTE: Where applicable,
0: Disable
1: Enable

611. LEGACY_BASIC_RATE: (offset: 0x1408)

Bits	Type	Name	Description	Initial Value
31:12	-	-	Reserved	0x0
11:0	RW	LEGACY_BASIC_RATE	Legacy Basic Rate Enables the legacy basic rate bit mask. Bit0: 1 Mbps is the basic rate. Bit1: 2 Mbps is the basic rate. Bit2: 5.5 Mbps is the basic rate. Bit3: 11 Mbps is the basic rate. Bit4: 6 Mbps is the basic rate. Bit5: 9 Mbps is the basic rate. Bit6: 12 Mbps is the basic rate. Bit7: 18 Mbps is the basic rate. Bit8: 24 Mbps is the basic rate. Bit9: 36 Mbps is the basic rate. Bit10: 48 Mbps is the basic rate. Bit11: 54 Mbps is the basic rate. 0: Disable 1: Enable	0x0

612. HT_BASIC_RATE: (offset: 0x140C)

Bits	Type	Name	Description	Initial Value
31: 16	R/W	STBC_BASIC_RATE	The definition is the same as that in PHY rate format.	0x8200
15:0	R/W	HT_BASIC_RATE	The definition is the same as that in PHY rate format.	0x8000

613. HT_CTRL_CFG: (offset: 0x1410)

Bits	Type	Name	Description	Initial Value
31:9	-	-	Reserved	-

Bits	Type	Name	Description	Initial Value
8:0	RW	HT_CTRL_THRES	HT Control Threshold Sets the remaining TXOP threshold for HT control frame auto-response. (unit: 1 μ s)	0x100

614. SIFS_COST_CFG: (offset: 0x1414)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RW	OFDM_SIFS_COST	OFDM SIFS Time Applied after OFDM Tx/Rx. (unit: 1 μ s)	0x10
7:0	RW	CCK_SIFS_COST	CCK SIFS Time Applied after CCK Tx/Rx. (unit: 1 μ s)	0xA

NOTE: The OFDM_SIFS_COST and CCK_SIFS_COST are used only for duration field calculation. They will not affect the response timing.

615. RX_PARSER_CFG: (offset: 0x1418)

Bits	Type	Name	Description	Initial Value
31:28	-	-	Reserved	0x0
27:16	RW	LSIG_LEN_THRES	L-SIG Length Threshold When the length in L-SIG is longer than this threshold, the L-SIG TXOP is not applied as NAV channel reservation. (unit: bytes)	0xFFFF
15:02	-	-	Reserved	0x0
1	RW	RX_LSIG_TXOP_EN	Rx L-SIG TXOP Enable Complies with channel reservations made by other stations using LSIG-TXOP. 0: Disable 1: Enable	0x0
0	RW	NAV_ALL_EN	NAV All Frames Enable Sets the NAV for all received frames. When disabled, unicast to me frames will not set the NAV. 0: Disable 1: Enable	0x0

616. MAC_ADDR_EXT_EN (offset: 0x147C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:1	-	-	Reserved	0x0
0	R/W	MAC_ADDR_EXT_EN	Enable Extended MAC Address	0x0

617. MAC_ADDR_EXT0_31_0 (offset: 0x1480, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT0_31_0	Extended MAC Address0 bit[31:0]	0x0

618. MAC_ADDR_EXT0_47_32 (offset: 0x1484, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT0_47_32	Extended MAC Address0 bit[47:32]	0x0

619. MAC_ADDR_EXT1_31_0 (offset: 0x1488, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT1_31_0	Extended MAC Address1 bit[31:0]	0x0

620. MAC_ADDR_EXT1_47_32 (offset: 0x148C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT1_47_32	Extended MAC Address1 bit[47:32]	0x0

621. MAC_ADDR_EXT2_31_0 (offset: 0x1490, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT2_31_0	Extended MAC Address2 bit[31:0]	0x0

622. MAC_ADDR_EXT2_47_32 (offset: 0x1494, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT2_47_32	Extended MAC Address2 bit[47:32]	0x0

623. MAC_ADDR_EXT3_31_0 (offset: 0x1498, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT3_31_0	Extended MAC Address3 bit[31:0]	0x0

624. MAC_ADDR_EXT3_47_32 (offset: 0x149C, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT3_47_32	Extended MAC Address3 bit[47:32]	0x0

625. MAC_ADDR_EXT4_31_0 (offset: 0x14A0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT4_31_0	Extended MAC Address4 bit[31:0]	0x0

626. MAC_ADDR_EXT4_47_32 (offset: 0x14A4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT4_47_32	Extended MAC Address4 bit[47:32]	0x0

627. MAC_ADDR_EXT5_31_0 (offset: 0x14A8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT5_31_0	Extended MAC Address5 bit[31:0]	0x0

628. MAC_ADDR_EXT5_47_32 (offset: 0x14AC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT5_47_32	Extended MAC Address5 bit[47:32]	0x0

629. MAC_ADDR_EXT6_31_0 (offset: 0x14B0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT6_31_0	Extended MAC Address6 bit[31:0]	0x0

630. MAC_ADDR_EXT6_47_32 (offset: 0x14B4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT6_47_32	Extended MAC Address6 bit[47:32]	0x0

631. MAC_ADDR_EXT7_31_0 (offset: 0x14B8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT7_31_0	Extended MAC Address7 bit[31:0]	0x0

632. MAC_ADDR_EXT7_47_32 (offset: 0x14BC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT7_47_32	Extended MAC Address7 bit[47:32]	0x0

633. MAC_ADDR_EXT8_31_0 (offset: 0x14C0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT8_31_0	Extended MAC Address8 bit[31:0]	0x0

634. MAC_ADDR_EXT8_47_32 (offset: 0x14C4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT8_47_32	Extended MAC Address8 bit[47:32]	0x0

635. MAC_ADDR_EXT9_31_0 (offset: 0x14C8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT9_31_0	Extended MAC Address9 bit[31:0]	0x0

636. MAC_ADDR_EXT9_47_32 (offset: 0x14CC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0

Bits	Type	Name	Description	Initial Value
15:0	R/W	MAC_ADDR_EXT9_47_32	Extended MAC Address9 bit[47:32]	0x0

637. MAC_ADDR_EXT10_31_0 (offset: 0x14D0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT10_1_0	Extended MAC Address10 bit[31:0]	0x0

638. MAC_ADDR_EXT10_47_32 (offset: 0x14D4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT10_47_32	Extended MAC Address10 bit[47:32]	0x0

639. MAC_ADDR_EXT11_31_0 (offset: 0x14D8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT11_31_0	Extended MAC Address11 bit[31:0]	0x0

640. MAC_ADDR_EXT11_47_32 (offset: 0x14DC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT11_47_32	Extended MAC Address11 bit[47:32]	0x0

641. MAC_ADDR_EXT12_31_0 (offset: 0x14E0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT12_31_0	Extended MAC Address12 bit[31:0]	0x0

642. MAC_ADDR_EXT12_47_32 (offset: 0x14E4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT12_47_32	Extended MAC Address12 bit[47:32]	0x0

643. MAC_ADDR_EXT13_31_0 (offset: 0x14E8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT13_31_0	Extended MAC Address13 bit[31:0]	0x0

644. MAC_ADDR_EXT13_47_32 (offset: 0x14EC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT13_47_32	Extended MAC Address13 bit[47:32]	0x0

645. MAC_ADDR_EXT14_31_0 (offset: 0x14F0, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT14_31_0	Extended MAC Address14 bit[31:0]	0x0

646. MAC_ADDR_EXT14_47_32 (offset: 0x14F4, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT14_47_32	Extended MAC Address14 bit[47:32]	0x0

647. MAC_ADDR_EXT15_31_0 (offset: 0x14F8, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:0	R/W	MAC_ADDR_EXT15_31_0	Extended MAC Address15 bit[31:0]	0x0

648. MAC_ADDR_EXT15_47_32 (offset: 0x14FC, default: 0x0000_0000)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0
15:0	R/W	MAC_ADDR_EXT15_47_32	Extended MAC Address15 bit[47:32]	0x0

2.22.12 MAC Security Configuration Registers (base: 0x1018_0000)

649. TX_SEC_CNT0: (offset: 0x1500)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_SEC_ERR_CNT	Tx Security Error Count Counts the number of transmitted frames that do not successfully pass the security engine.	0x0
15:0	RC	TX_SEC_CPL_CNT	Tx Security Engine Complete Count Counts the number of transmitted frames that successfully pass the security engine.	0x0

650. RX_SEC_CNT0: (offset: 0x1504)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RC	RX_SEC_CPL_CNT	Rx Security Complete Count Counts the number of received frames that successfully pass the security engine.	0x0

651. CCMP_FC_MUTE: (offset: 0x1508)

Bits	Type	Name	Description	Initial Value
31:16	RW	HT_CCMP_FC_MUTE	HT CCMP Frame Control Bit Mute Mutes the frame control bit when using CCMP encryption for HT transmission.	0xC78F
15:0	RW	LG_CCMP_FC_MUTE	LG CCMP Frame Control Bit Mute Mutes the frame control bit when using CCMP encryption for legacy transmission.	0xC78F

2.22.13 MAC HCCA/PSMP Control Status Registers (base: 0x1018_0000)

2.22.13.1 List of Registers

No.	Offset	Register Name	Description	Page
652	0x1600	TXOP_HLDR_ADDR0	Transmit Opportunity Holder Address 0	459
653	0x1604	TXOP_HLDR_ADDR1	Transmit Opportunity Holder Address 1	459
654	0x1608	TXRX_MICS_CTRL	Tx/Rx MICS Control	459
655	0x160C	QOS_CFPOLL_RA_DW0	QoS Contention Free Poll (CF-Poll) DWORD A 0	460
656	0x1610	QOS_CFPOLL_A1_DW1	QoS CF-Poll DWORD A 1	460
657	0x1614	QOS_CFPOLL_QC	QoS CF-Poll QoS Control	460

2.22.13.2 Register Descriptions

652. TXOP_HLDR_ADDR0: (offset: 0x1600)

Bits	Type	Name	Description	Initial Value
31:24	RW	TXOP_HOL_3	TXOP holder MAC address byte3	0x0
23:16	RW	TXOP_HOL_2	TXOP holder MAC address byte2	0x0
15:8	RW	TXOP_HOL_1	TXOP holder MAC address byte1	0x0
7:0	RW	TXOP_HOL_0	TXOP holder MAC address byte0	0x0

653. TXOP_HLDR_ADDR1: (offset: 0x1604)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RW	TXOP_HOL_5	TXOP holder MAC address byte5	0x0
7:0	RW	TXOP_HOL_4	TXOP holder MAC address byte4	0x0

NOTE: Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

654. TXRX_MICS_CTRL: (offset: 0x1608)

Bits	Type	Name	Description	Initial Value
31:25	-	-	Reserved	0x0
24	RW	AMPDU_ACC_EN	Enables AMPDU accumulation.	0x0
23:19	RW	TX_DMA_TIMEOUT	Tx DMA Timeout When AMPDU_ACC_EN is enabled, the AMPDU is held for at most (TX_DMA_TIMEOUT * 32) µsec in which time additional MPDUs are added to the AMPDU.	0x0
18	RW	TX_FBK_THRES_EN	Enables the Tx MCS fallback threshold.	0x0
17:16	RW	TX_FBK_THRES	Tx Fallback Threshold When TX_FBK_THRES_EN is enabled, MCS fallback occurs when: 0: Less than 25% of MPDUs in an A-MPDU are successfully ACKed. 1: Less than 50% of MPDUs in an A-MPDU are successfully ACKed. 2: Less than 75% of MPDUs in an A-MPDU are successfully ACKed. 3: Less than 100% of MPDUs in an A-MPDU are successfully ACKed.	0x0
15:5	-	-	Reserved	0x0
4	RW	PAPE_MAP	Power Amplifier Power Enable Mapping When PAPE_MAP1S_EN is enabled: 0: Only turn on PAPE0 for 1S transmission. 1: Only turn on PAPE1 for 1S transmission.	0x0

Bits	Type	Name	Description	Initial Value
3	RW	PAPE_MAP1S_EN	Power Amplifier Power Enable 1 Stream Mapping Enable Sets PAPE to turn on only in 1S transmission.	0x0
2	RW	TX_BCN_HIPRI_DIS	Tx Beacon High Priority Disable Disables high priority beacon transmission.	0x0
1	RW	TX40M_BLK_EN	Tx 40 MHz Block Enable Enables blocking of 40 Mhz transmission when extension CCA is busy.	0x0
0	RW	PER_RX_RST_EN	Per Packet Receive Reset Enable Enables reset of the baseband RX_PE after receiving a packet.	0x0

NOTE: Where applicable,
0: Disable
1: Enable

655. QOS_CFPOLL_RA_DW0: (offset: 0x160C)

Bits	Type	Name	Description	Initial Value
31:24	RO	CFPOLL_A1_BYTE3	Byte3 of A1 of received QoS Data (+) CF-Poll frame	-
23:16	RO	CFPOLL_A1_BYTE2	Byte2 of A1 of received QoS Data (+) CF-Poll frame	-
15:8	RO	CFPOLL_A1_BYTE1	Byte1 of A1 of received QoS Data (+) CF-Poll frame	-
7:0	RO	CFPOLL_A1_BYTE0	Byte0 of A1 of received QoS Data (+) CF-Poll frame	-

656. QOS_CFPOLL_A1_DW1: (offset: 0x1610)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
16	RO	CFPOLL_A1_TOME	0: QoS CF-Poll not to me 1: QoS CF-Poll to me	-
15:8	RO	CFPOLL_A1_BYTE5	Byte5 of A1 of received QoS Data (+) CF-Poll frame	-
7:0	RO	CFPOLL_A1_BYTE4	Byte4 of A1 of received QoS Data (+) CF-Poll frame	-

657. QOS_CFPOLL_QC: (offset: 0x1614)

Bits	Type	Name	Description	Initial Value
31:24	-	-	Reserved	0x0
15:8	RO	CFPOLL_QC_BYTE1	Byte1 of QC of received QoS Data (+) CF-Poll frame	-
7:0	RO	CFPOLL_QC_BYTE0	Byte0 of QC of received QoS Data (+) CF-Poll frame	-

NOTE: CFPOLL_RA_DW0, CFPOLL_RA_DW1, and CFPOLL_QC are updated after receiving a QoS Data (+)CF-Poll frame. An Rx QoS CF-Poll interrupt (RX_QOS_CFPOLL_INT) is then launched.

2.22.14 MAC Statistic Counters (base: 0x1018_0000)

2.22.14.1 List of Registers

No.	Offset	Register Name	Description	Page
658	0x1700	RX_STA_CNT0	Receive Status Counter 0	463
659	0x1704	RX_STA_CNT1	Receive Status Counter 1	463
660	0x1708	RX_STA_CNT2	Receive Status Counter 2	463
661	0x170C	TX_STA_CNT0	Transmit Status Counter 0	463
662	0x1710	TX_STA_CNT1	Transmit Status Counter 1	464
663	0x1714	TX_STA_CNT2	Transmit Status Counter 2	464
664	0x1718	TX_STAT_FIFO	Transmit Status FIFO	464
665	0x171C	TX_NAG_AGG_CNT	Transmit Unaggregated/Aggregated MPDU Count	464
666	0x1720	TX_AGG_CNT0	Transmit A-MPDU Count 0	465
667	0x1724	TX_AGG_CNT1	Transmit A-MPDU Count 1	465
...	...	...	...	
673	0x173C	TX_AGG_CNT7	Transmit A-MPDU Count 7	466
674	0x1740	MPDU_DENSITY_CNT	MPDU Density Count	466
675	0x1744	RTS_TX_CNT	Request to Send Transmit Count	466
676	0x1748	CTS_TX_CNT	Clear to Send Transmit Count	467
677	0x174C	TX_AGG_CNT8	Transmit A-MPDU Count 8	467
...	...	...	...	
684	0x1768	TX_AGG_CNT15	Transmit A-MPDU Count 15	468
685	0x176C	WCID_A_TX_CNT	Wireless Client ID A Tx Counter	468
...	...	...	...	
692	0x1788	WCID_H_TX_CNT	Wireless Client ID H Tx Counter	470
693	0x178C	WCID_X_SELECT	Wireless Client ID X Select	470
694	0x1790	WCID_X_SELECT	Wireless Client ID X Select	470
695	0x1794	TX_REPORT_CNT	Tx Report Counter	470
696	0x1798	TX_STAT_FIFO_EXT	Tx Status FIFO Extension	470

2.22.14.2 Register Descriptions

658. RX_STA_CNT0: (offset: 0x1700)

Bits	Type	Name	Description	Initial Value
31:16	RC	PHY_ERRCNT	PHY Error Count Counts the number of frames with Rx PHY errors.	0x0
15:0	RC	CRC_ERRCNT	CRC Error Count Counts the number of frames with Rx CRC errors.	0x0

NOTE:

1. An Rx PHY error means the PSDU length is shorter than the length indicated by PLCP.
2. An Rx PHY error is also treated as a CRC error.

659. RX_STA_CNT1: (offset: 0x1704)

Bits	Type	Name	Description	Initial Value
31:16	RC	PLPC_ERRCNT	Rx PLPC Error Count Counts the number of frames with Rx PLCP errors.	0x0
15:0	RC	CCA_ERRCNT	CCA Error Count Counts the number of CCA false alarms.	0x0

NOTE:

- 1: A CCA false alarm means there is no PLCP after CCA indication.
- 2: An Rx PLCP error means there is no PSDU after PLCP indication.

660. RX_STA_CNT2: (offset: 0x1708)

Bits	Type	Name	Description	Initial Value
31:16	RC	RX_OVFL_CNT	Rx Overflow Count Counts the number of frames in an Rx FIFO overflow.	0x0
15:0	RC	RX_DUPL_CNT	Rx Duplicate Count Counts the number of Rx duplicated filtered frames.	0x0

NOTE: MAC does NOT auto-respond ACK/BA to the frame originator when a frame is lost due to an RXFIFO overflow. However, the MAC responds when a frame is duplicate filtered.

661. TX_STA_CNT0: (offset: 0x170C)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_BCN_CNT	Tx Beacon Frame Count Counts the number of Beacon frames transmitted.	0x0
15:0	RC	TX_FAIL_CNT	Tx Fail Count Counts the number of frames that are not successfully delivered.	0x0

662. TX_STA_CNT1: (offset: 0x1710)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_RTY_CNT	Tx Retry Count Counts the number of times delivery of a frame was reattempted after initial failure.	0x0
15:0	RC	TX_SUCC_CNT	Tx Successful Count Counts the number of frames successfully transmitted.	0x0

663. TX_STA_CNT2: (offset: 0x1714)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_UDFL_CNT	Tx Underflow Count Counts the number of frames missing in a transmission queue.	0x0
15:0	RC	TX_ZERO_CNT	Tx Zero Length Count Counts the number of frames transmitted with zero length.	0x0

664. TX_STAT_FIFO: (offset: 0x1718)

Bits	Type	Name	Description	Initial Value
31:16	RO	TXQ_RATE	Tx success rate	-
15:8	RO	TXQ_WCID	Tx WCID	-
7	RO	TXQ_ACKREQ	Tx Acknowledgement Required Indicates whether Tx acknowledgement is required. 0: Not required 1: Required	-
6	RO	TXQ_AGG	Tx Aggregated Indicates whether a Tx MPDU is aggregated. 0: Not aggregated 1: Aggregated	-
5	RO	TXQ_OK	Tx Success Indicates the Tx of an MPDU is successful. 0: Failed 1: Successful	-
4:1	-	-	Reserved	-
0	RC	TXQ_VLD	Tx Queue Valid Indicates the status of a Tx queue. 0: Queue empty 1: Valid	0x0

NOTE: Tx status FIFO size = 16.

665. TX_NAG_AGG_CNT: (offset: 0x171C)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_CNT	A-MPDUs Tx Count Counts the number of A-MPDUs transmitted.	0x0

Bits	Type	Name	Description	Initial Value
15:0	RC	TX_NAG_CNT	Tx Unaggregated Count Counts the number of unaggregated MPDUs transmitted.	0x0

666. TX_AGG_CNT0: (offset: 0x1720)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_2_CNT	A-MPDU Size 2 Tx Count Counts the number of A-MPDUs with aggregate size = 2.	0x0
15:0	RC	TX_AGG_1_CNT	A-MPDU Size 1 Tx Count Counts the number of A-MPDUs with aggregate size = 1.	0x0

667. TX_AGG_CNT1: (offset: 0x1724)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_4_CNT	A-MPDU Size 4 Tx Count Counts the number of A-MPDUs with aggregate size = 4.	0x0
15:0	RC	TX_AGG_3_CNT	A-MPDU Size 3 Tx Count Counts the number of A-MPDUs with aggregate size = 3.	0x0

668. TX_AGG_CNT2: (offset: 0x1728)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_6_CNT	A-MPDU Size 6 Tx Count Counts the number of A-MPDUs with aggregate size = 6.	0x0
15:0	RC	TX_AGG_5_CNT	A-MPDU Size 5 Tx Count Counts the number of A-MPDUs with aggregate size = 5.	0x0

669. TX_AGG_CNT3: (offset: 0x172C)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_8_CNT	A-MPDU Size 8 Tx Count Counts the number of A-MPDUs with aggregate size = 8.	0x0
15:0	RC	TX_AGG_7_CNT	A-MPDU Size 7 Tx Count Counts the number of A-MPDUs with aggregate size = 7.	0x0

670. TX_AGG_CNT4: (offset: 0x1730)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_10_CNT	A-MPDU Size 10 Tx Count Counts the number of A-MPDUs with aggregate size = 10.	0x0

Bits	Type	Name	Description	Initial Value
15:0	RC	TX_AGG_9_CNT	A-MPDU Size 9 Tx Count Counts the number of A-MPDUs with aggregate size = 9.	0x0

671. TX_AGG_CNT5: (offset: 0x1734)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_12_CNT	A-MPDU Size 12 Tx Count Counts the number of A-MPDUs with aggregate size = 12.	0x0
15:0	RC	TX_AGG_11_CNT	A-MPDU Size 11 Tx Count Counts the number of A-MPDUs with aggregate size = 11.	0x0

672. TX_AGG_CNT6: (offset: 0x1738)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_14_CNT	A-MPDU Size 14 Tx Count Counts the number of A-MPDUs with aggregate size = 14.	0x0
15:0	RC	TX_AGG_13_CNT	A-MPDU Size 13 Tx Count Counts the number of A-MPDUs with aggregate size = 13.	0x0

673. TX_AGG_CNT7: (offset: 0x173C)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_16_CNT	A-MPDU Size 16 Tx Count Counts the number of A-MPDUs with aggregate size = 16.	0x0
15:0	RC	TX_AGG_15_CNT	A-MPDU Size 15 Tx Count Counts the number of A-MPDUs with aggregate size = 15.	0x0

674. MPDU_DENSITY_CNT: (offset: 0x1740)

Bits	Type	Name	Description	Initial Value
31:16	RC	RX_ZERO_DEL_CNT	Rx Zero Delimiters Count Counts the number of zero length delimiters received.	0x0
15:0	RC	TX_ZERO_DEL_CNT	Tx Zero Delimiters Count Counts the number of zero length delimiters transmitted.	0x0

675. RTS_TX_CNT: (offset: 0x1744)

Bits	Type	Name	Description	Initial Value
31:16	RC	RTS_TX_FAIL_CNT	RTS Frames Tx Failed Count Counts the number of transmitted RTS frames that failed.	0x0

Bits	Type	Name	Description	Initial Value
15:0	RC	RTS_TX_OK_CNT	RTS Frames Tx Succeeded Count Counts the number of successful RTS frames transmitted.	0x0

676. CTS_TX_CNT: (offset: 0x1748)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RC	CTSTS_TX_CNT	CTS-to-Self Frames Tx Count Counts the number of CTS-to-self frames transmitted.	0x0

677. TX_AGG_CNT8: (offset: 0x174C)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_18_CNT	A-MPDU Size 18 Tx Count Counts the number of A-MPDUs with aggregate size = 18.	0x0
15:0	RC	TX_AGG_17_CNT	A-MPDU Size 17 Tx Count Counts the number of A-MPDUs with aggregate size = 17.	0x0

678. TX_AGG_CNT9: (offset: 0x1750)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_20_CNT	A-MPDU Size 20 Tx Count Counts the number of A-MPDUs with aggregate size = 20.	0x0
15:0	RC	TX_AGG_19_CNT	A-MPDU Size 19 Tx Count Counts the number of A-MPDUs with aggregate size = 19.	0x0

679. TX_AGG_CNT10: (offset: 0x1754)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_22_CNT	A-MPDU Size 22 Tx Count Counts the number of A-MPDUs with aggregate size = 22.	0x0
15:0	RC	TX_AGG_21_CNT	A-MPDU Size 21 Tx Count Counts the number of A-MPDUs with aggregate size = 21.	0x0

680. TX_AGG_CNT11: (offset: 0x1758)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_24_CNT	A-MPDU Size 24 Tx Count Counts the number of A-MPDUs with aggregate size = 24.	0x0

Bits	Type	Name	Description	Initial Value
15:0	RC	TX_AGG_23_CNT	A-MPDU Size 23 Tx Count Counts the number of A-MPDUs with aggregate size = 24.	0x0

681. TX_AGG_CNT12: (offset: 0x175C)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_26_CNT	A-MPDU Size 26 Tx Count Counts the number of A-MPDUs with aggregate size = 26.	0x0
15:0	RC	TX_AGG_25_CNT	A-MPDU Size 25 Tx Count Counts the number of A-MPDUs with aggregate size = 25.	0x0

682. TX_AGG_CNT13: (offset: 0x1760)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_28_CNT	A-MPDU Size 28 Tx Count Counts the number of A-MPDUs with aggregate size = 28.	0x0
15:0	RC	TX_AGG_27_CNT	A-MPDU Size 27 Tx Count Counts the number of A-MPDUs with aggregate size = 27.	0x0

683. TX_AGG_CNT14: (offset: 0x1764)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_30_CNT	A-MPDU Size 30 Tx Count Counts the number of A-MPDUs with aggregate size = 28.	0x0
15:0	RC	TX_AGG_29_CNT	A-MPDU Size 29 Tx Count Counts the number of A-MPDUs with aggregate size = 29.	0x0

684. TX_AGG_CNT15: (offset: 0x1768)

Bits	Type	Name	Description	Initial Value
31:16	RC	TX_AGG_32_CNT	A-MPDU Size 32 Tx Count Counts the number of A-MPDUs with aggregate size = 32.	0x0
15:0	RC	TX_AGG_31_CNT	A-MPDU Size 31 Tx Count Counts the number of A-MPDUs with aggregate size = 31.	0x0

685. WCID_A_TX_CNT: (offset: 0x176C)

Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_A_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_A.	0x0

Bits	Type	Name	Description	Initial Value
15:0	RC	WCID_A_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_A.	0x0

686. WCID_B_TX_CNT: (offset: 0x1770)

Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_B_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_B.	0x0
15:0	RC	WCID_B_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_B	0x0

687. WCID_C_TX_CNT: (offset: 0x1774)

Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_C_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_C.	0x0
15:0	RC	WCID_C_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_C.	0x0

688. WCID_D_TX_CNT: (offset: 0x1778)

Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_D_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_D.	0x0
15:0	RC	WCID_D_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_D	0x0

689. WCID_E_TX_CNT: (offset: 0x177C)

Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_E_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_E.	0x0
15:0	RC	WCID_E_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_E.	0x0

690. WCID_F_TX_CNT: (offset: 0x1780)

Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_F_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_F.	0x0
15:0	RC	WCID_F_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_F.	0x0

691. WCID_G_TX_CNT: (offset: 0x1784)

Bits	Type	Name	Description	Initial Value
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Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_G_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_G.	0x0
15:0	RC	WCID_G_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_G.	0x0

692. WCID_H_TX_CNT: (offset: 0x1788)

Bits	Type	Name	Description	Initial Value
31:16	RC	WCID_H_TXRTY_CNT	WCID Tx Retry Count 0 Counts the number of Tx retries for WCID_H.	0x0
15:0	RC	WCID_H_TXOK_CNT	WCID Tx OK Count 0 Counts the number of successful Tx for WCID_H.	0x0

693. WCID_X_SELECT: (offset: 0x178C)

Bits	Type	Name	Description	Initial Value
31:24	RW	WCID_D_SELECT	WCID selection for WCID_D Tx counters	0x0
23:16	RW	WCID_C_SELECT	WCID selection for WCID_C Tx counters	0x0
15:8	RW	WCID_B_SELECT	WCID selection for WCID_B Tx counters	0x0
7:0	RW	WCID_A_SELECT	WCID selection for WCID_A Tx counters	0x0

694. WCID_X_SELECT: (offset: 0x1790)

Bits	Type	Name	Description	Initial Value
31:24	RW	WCID_H_SELECT	WCID selection for WCID_H Tx counters	0xFF
23:16	RW	WCID_G_SELECT	WCID selection for WCID_G Tx counters	0xFF
15:8	RW	WCID_F_SELECT	WCID selection for WCID_F Tx counters	0xFF
7:0	RW	WCID_E_SELECT	WCID selection for WCID_E Tx counters	0xFF

695. TX_REPORT_CNT: (offset: 0x1794)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:0	RC	TX_REPORT_CNT	Tx Report Count Counts the number of successful Tx frames with TXWI.REPORT bit =1.	0x0

696. TX_STAT_FIFO_EXT: (offset: 0x1798)

Bits	Type	Name	Description	Initial Value
31:16	-	-	Reserved	0x0
15:8	RO	TX_PKT_ID	Tx Packet ID (copied from per packet TXWI)	-
7:0	RO	TX_RTY_CNT	Tx Retry Count Counts the number of retries for each Tx frame (read before reading 0x1718).	-

2.22.15 MAC Search Table (base: 0x1018_1800)

2.22.15.1 Rx WCID Search Entry Format (8 bytes)

Offset	Type	Name	Description	Initial Value
0x00	RW	WC_MAC_ADDR0	Client MAC address byte0	0x0
0x01	RW	WC_MAC_ADDR1	Client MAC address byte1	0x0
0x02	RW	WC_MAC_ADDR2	Client MAC address byte2	0x0
0x03	RW	WC_MAC_ADDR3	Client MAC address byte3	0x0
0x04	RW	WC_MAC_ADDR4	Client MAC address byte4	0x0
0x05	RW	WC_MAC_ADDR5	Client MAC address byte5	0x0
0x06	RW	BA_SESS_MASK0	BA session mask (lower) Bit0 for TID0 Bit7 for TID7	0x0
0x07	RW	BA_SESS_MASK1	BA session mask (upper) Bit8 for TID8 Bit15 for TID15	0x0

2.22.15.2 Rx WCID Search Table (offset: 0x1800)

Table 2-27: 0x1398 TX_RATE_LUT_EN = 0 and MULTI_MAC_ADDRESS = 0

Offset	Type	Name	Description	Initial Value
0x1800	RW	WC_ENTRY_0	WC MAC address with WCID=0	0x0
0x1808	RW	WC_ENTRY_1	WC MAC address with WCID=1	0x0
....	RW		WC MAC address with WCID=2 to 253	0x0
0x1BF8	RW	WC_ENTRY_127	WC MAC address with WCID=127	0x0
0x1C00	RW	WC_ENTRY_128	WC MAC address with WCID=128	0x0
0x1C08	RW	WC_ENTRY_129	WC MAC address with WCID=129	0x0
....	RW		WC MAC address with WCID=130 to 254	0x0
0x1FF8	RW	WC_ENTRY_255	WC MAC address with WCID=255	0x0

Table 2-28: 0x1398 TX_RATE_LUT_EN = 1 and MULTI_MAC_ADDRESS = 0

Offset	Type	Name	Description	Initial Value
0x1800	RW	WC_ENTRY_0	WC MAC address with WCID=0	0x0
0x1808	RW	WC_ENTRY_1	WC MAC address with WCID=1	0x0
....	RW		WC MAC address with WCID=2 to 126	0x0
0x1BF8	RW	WC_ENTRY_127	WC MAC address with WCID=127	0x0
0x1C00	RW	WCID0_TX_RATE	Bit[15:0]: WCID0 Tx Rate	0x0
0x1C08	RW	WCID1_TX_RATE	Bit[15:0]: WCID1 Tx Rate	0x0
....	RW		Bit[15:0]: WCID=2 to 126 Tx Rate	0x0
0x1FF8	RW	WCID127_TX_RATE	Bit[15:0]: WCID127 Tx Rate	0x0

Table 2-29: 0x1398 TX_RATE_LUT_EN = 1 and MULTI_MAC_ADDRESS = 1

Offset	Type	Name	Description	Initial Value
0x1800	RW	WC_ENTRY_0	WC MAC address with WCID=0	0x0
0x1808	RW	WC_ENTRY_1	WC MAC address with WCID=1	0x0
....	RW		WC MAC address with WCID=2 to 110	0x0
0x1B78	RW	WC_ENTRY_111	WC MAC address with WCID=111	0x0
0x1B80	RW	MULTI_MAC_ADDR0	Multiple MAC address 0	0x0
0x1B88	RW	MULTI_MAC_ADDR1	Multiple MAC address 1	0x0
....	RW		Multiple MAC address 2 to 14	0x0
0x1BF8	RW	MULTI_MAC_ADDR15	Multiple MAC address 15	0x0
0x1C00	RW	WCID0_TX_RATE	Bit[15:0]: WCID0 Tx Rate	0x0
0x1C08	RW	WCID1_TX_RATE	Bit[15:0]: WCID1 Tx Rate	0x0
....	RW		Bit[15:0]: WCID=2 to 126 Tx Rate	0x0
0x1FF8	RW	WCID127_TX_RATE	Bit[15:0]: WCID127 Tx Rate	0x0

3. Security Entry Formats and Key Tables

3.1 Security Entry Format Tables (base: 1018.0000, offset: 0x4000)

Table Name	Description
Security Key Format (8DW)	The location and format of the security key.
IV/EIV/WAPI_PN Format (4DW)	The location and format of the (Extend) Initialization Vector and WAPI packet number.
WCID Attribute Entry Format (1DW)	The location and format of the wireless client attributes.
Shared Key Mode Entry Format (1DW)	The location and format of the shared keys for different security methods.

3.1.1 Security Key Format (8DW)

Offset	Type	Name	Description	Initial Value
0x00	RW	SECKEY_DW0	Security key byte3 to byte0	*
0x04	RW	SECKEY_DW1	Security key byte7 to byte4	*
0x08	RW	SECKEY_DW2	Security key byte11 to byte8	*
0x0C	RW	SECKEY_DW3	Security key byte15 to byte12	*
0x10	RW	TXMIC_DW0	Tx MIC key byte3 to byte0	*
0x14	RW	TXMIC_DW1	Tx MIC key byte7 to byte4	*
0x18	RW	RXMIC_DW0	Rx MIC key byte3 to byte0	*
0x1C	RW	RXMIC_DW1	Rx MIC key byte7 to byte4	*

NOTE:

1. For WEP40 and CKIP40, only byte4 to byte0 of a security key are valid.
2. For WEP104 and CKIP104, only byte12 to byte0 of a security key are valid.
3. For TKIP and AES, all the bytes of a security key are valid.
4. The Tx/Rx MIC key is used only for TKIP MIC calculation.
5. The 128-byte space at 0x10/0x14/0x18/0x1C may be used for either the Tx/Rx MIC key, or the WAPI MIC key. The WAPI MIC key will use all this space, but the Tx/Rx MIC key will only use some of this space.

3.1.2 IV/EIV/WAPI_PN Format (4DW)

When TXINFO.WIV=0, hardware auto-looks up IV/EIV/WAPI_PN from this table and updates IV/EIVWAPI_PN after encryption is finished.

3.1.2.1 IV/EIV Format

Offset	Type	Name	Description	Initial Value
0x00	RW	IV_FIELED	IV field	*
0x04	RW	EIV_FIELED	EIV field	*

Table 3-1 IV/EIV Format

3.1.2.2 WAPI_PN Format

Offset	Type	Name	Description	Initial Value
0x00	RW	WAPI_PN_MSB	WAPI PN byte11 to byte8	*
0x04	RW	WAPI_PN_MSB	WAPI PN byte15 to byte12	*

Table 3-2 WAPI_PN Format

NOTE:

1. The key index and extension IV bit are initialized by software. The MSB octet of IV is not modified by hardware.
2. IV/EIV packet number (PN) counter modes:
 - For WEP40, WEP104, CKIP40, CKIP104, CKIP128 mode, PN=IV[23:0]. EIV[31:0] is not used.
 - For TKIP mode, PN = {EIV[31:0], IV[7:0], IV[23:16]}, IV[15:8]=(IV[7:0] | 0x20) & 0x7F) is generated by hardware.
 - For AES-CCMP, PN = {EIV[31:0], IV[15:0]}.
 - For non-WAPI mode, PN = PN + 1 after each encryption.
 - For WAPI mode, PN={WAPI_PN_MSB_1[31:0], WAPI_PN_MSB_0[31:0], EIV[31:0], IV[31:0]}.
 - For WAPI mode, PN=PN+2 when WAPI_MC_BC=0 in WCID attribute.
 - For WAPI mode, PN=PN+1 when WAPI_MC_BC=1 in WCID attribute.
- 3: Software may initialize the PN counter to any value.

3.1.3 WCID Attribute Entry Format (1DW)

Offset	Type	Name	Description	Initial Value
31:24	RW	WAPI_KEYID_BYTE	WAPI KeyID Byte 0-1: WAPI Key ID 2-255: reserved	*
23:16	RW	WAPI_RSV_BYTE	WAPI Reserved Byte (set to 0)	*
15	RW	WAPI_MCBC	WAPI Broadcast/Multicast Packet Number (PN) Increment 0: Unicast, PN = PN + 2 1: Multicast/broadcast, PN = PN + 1	*
14:12	RW	-	Reserved	*
11	RW	BSS_IDX_MBS	Use together with BSS_IDX(bit[6:4]), (BSS_IDX_MSB * 8 + BSS_IDX) = BSS Index of the WCID	*
10	RW	RX_PKEY_MODE_MSB	Use together with RX_PKEY_MODE(bit[3:1]), (RX_PKEY_MODE_MSB * 8 + RX_PKEY_MODE) = 0:7: As listed in RX_PKEY_MODE 8: WAPI 9:15: Reserved	*
9:7	RW	RXWI_UDF	RXWI User Defined Field This field is tagged in the RXWI.UDF fields for the WCID.	*
6:4	RW	BSS_IDX	Multiple-BSS index for the WCID	*

Offset	Type	Name	Description	Initial Value
3:1	RW	RX_PKEY_MODE	Pairwise Key Security Mode 0: No security 1: WEP40 2: WEP104 3: TKIP 4: AES-CCMP 5: CKIP40 6: CKIP104 7: CKIP128	*
0	RW	RX_PKEY_EN	Key Table Selection 0: Shared key table 1: Pairwise key table	*

Table 3-3 WCID Attribute Entry Format

3.1.4 Shared Key Mode Entry Format (1DW)

Bits	Type	Name	Description	Initial Value
31:28	RW	SKEY_MODE_7+	Shared key7+(8x) mode, x=0 to 3	*
27:24	RW	SKEY_MODE_6+	Shared key6+(8x) mode, x=0 to 3	*
23:20	RW	SKEY_MODE_5+	Shared key5+(8x) mode, x=0 to 3	*
19:16	RW	SKEY_MODE_4+	Shared key4+(8x) mode, x=0 to 3	*
15:12	RW	SKEY_MODE_3+	Shared key3+(8x) mode, x=0 to 3	*
11:8	RW	SKEY_MODE_2+	Shared key2+(8x) mode, x=0 to 3	*
7:4	RW	SKEY_MODE_1+	Shared key1+(8x) mode, x=0 to 3	*
3:0	RW	SKEY_MODE_0+	Shared key0+(8x) mode, x=0 to 3	*

Table 3-4 Shared Key Mode Entry Format (1DW)

Key mode definition:

0: No security	5: CKIP40
1: WEP40	6: CKIP104
2: WEP104	7: CKIP128
3: TKIP	8: WAPI
4: AES-CCMP	9 to 15: Reserved

3.2 Security Tables (offset: 0x4000)

The following security tables are found in this section.

Table Name and Offset	Description
Pairwise Key Table (offset: 0x4000)	The location and format of the pairwise keys.
IV/EIV Table (offset: 0x6000)	The location and format of the (Extended) Initialization Vectors.
WCID Attribute Table (offset: 0x6800)	The location and format of the wireless client attributes.
Shared Key Table (offset: 0x6C00)	The location and format of the shared keys.
Shared Key Mode (offset: 0x7000)	The location and format of the shared key security method.
Shared Key Mode Extension (for BSS_IDX=8 to 15) (offset: 0x73F0)	The location and format of additional shared key security methods.
Shared Key Table Extension (for BSS_IDX=8 to 15) (offset: 0x7400)	The location and format of additional shared key security methods.
WAPI PN Table (Extension of IV/EIV Table) (offset: 0x7800)	The location and format of the WAPI packet numbers.

3.3 Security Table Map

The following table shows the memory locations of the security key tables.

0x4000	Pairwise Key Table (8 KB)
0x6000	IV/EIV Table (2 KB)
0x6800	WCID Attribute Table (1 KB)
0x6C00	Shared Key Table (1 KB)
0x7000	Shared Key Mode + Spare memory space (1 KB not fully used)
0x7400	Shared Key Extension Table (1 KB)
0x7800	WAPI PN Table (2 KB)

Figure 3-1 Security Key Memory Locations

3.3.1 Pairwise Key Table (offset: 0x4000)

Offset	Type	Name	Description	Initial Value
0x4000	RW	PKEY_0	Pairwise key for WCID0	*
0x4020	RW	PKEY_1	Pairwise key for WCID1	*
....	RW		Pairwise key for WCID2 to 253	*
0x5FC0	RW	PKEY_254	Pairwise key for WCID254	*
0x5FE0	RW	PKEY_255	Pairwise key for WCID255 (not used)	*

Table 3-5 Pairwise Key Table (offset: 0x4000)

3.3.2 IV/EIV Table (offset: 0x6000)

Offset	Type	Name	Description	Initial Value
0x6000	RW	IVEIV_0	IV/EIV for WCID0	*
0x6008	RW	IVEIV_1	IV/EIV for WCID1	*
....	RW		IV/EIV for WCID2 to WCID253	*
0x67F0	RW	IVEIV_254	IV/EIV for WCID254	*
0x67F8	RW	IVEIV_255	IV/EIV for WCID255 (not used)	*

Table 3-6 IV/EIV Table (offset: 0x6000)

3.3.3 WCID Attribute Table (offset: 0x6800)

Offset	Type	Name	Description	Initial Value
0x6800	RW	WCID_ATTR_0	WCID attribute for WCID0	*
0x6804	RW	WCID_ATTR_1	WCID attribute for WCID1	*
....	RW		WCID attribute for WCID2 to WCID253	*
0x6BF8	RW	WCID_ATTR_254	WCID attribute for WCID254	*
0x6BFC	RW	WCID_ATTR_255	WCID attribute for WCID255	*

Table 3-7 WCID Attribute Table (offset: 0x6800)

3.3.4 Shared Key Table (offset: 0x6C00)

Offset	Type	Name	Description	Initial Value
0x6C00	RW	SKEY_0	Shared key for BSS_IDX=0, KEY_IDX=0	*
0x6C20	RW	SKEY_1	Shared key for BSS_IDX=0, KEY_IDX=1	*
0x6C40	RW	SKEY_2	Shared key for BSS_IDX=0, KEY_IDX=2	*
0x6C60	RW	SKEY_3	Shared key for BSS_IDX=0, KEY_IDX=3	*
0x6C80	RW	SKEY_4	Shared key for BSS_IDX=1, KEY_IDX=0	*
0x6CA0	RW	SKEY_5	Shared key for BSS_IDX=1, KEY_IDX=1	*
0x6CC0	RW	SKEY_6	Shared key for BSS_IDX=1, KEY_IDX=2	*
0x6CE0	RW	SKEY_7	Shared key for BSS_IDX=1, KEY_IDX=3	*
0x6D00	RW	SKEY_8	Shared key for BSS_IDX=2, KEY_IDX=0	*
0x6D20	RW	SKEY_9	Shared key for BSS_IDX=2, KEY_IDX=1	*
0x6D40	RW	SKEY_10	Shared key for BSS_IDX=2, KEY_IDX=2	*

Offset	Type	Name	Description	Initial Value
0x6D60	RW	SKEY_11	Shared key for BSS_IDX=2, KEY_IDX=3	*
0x6D80	RW	SKEY_12	Shared key for BSS_IDX=3, KEY_IDX=0	*
0x6DA0	RW	SKEY_13	Shared key for BSS_IDX=3, KEY_IDX=1	*
0x6DC0	RW	SKEY_14	Shared key for BSS_IDX=3, KEY_IDX=2	*
0x6DE0	RW	SKEY_15	Shared key for BSS_IDX=3, KEY_IDX=3	*
0x6E00	RW	SKEY_16	Shared key for BSS_IDX=4, KEY_IDX=0	*
0x6E20	RW	SKEY_17	Shared key for BSS_IDX=4, KEY_IDX=1	*
0x6E40	RW	SKEY_18	Shared key for BSS_IDX=4, KEY_IDX=2	*
0x6E60	RW	SKEY_19	Shared key for BSS_IDX=4, KEY_IDX=3	*
0x6E80	RW	SKEY_20	Shared key for BSS_IDX=5, KEY_IDX=0	*
0x6EA0	RW	SKEY_21	Shared key for BSS_IDX=5, KEY_IDX=1	*
0x6EC0	RW	SKEY_22	Shared key for BSS_IDX=5, KEY_IDX=2	*
0x6EE0	RW	SKEY_23	Shared key for BSS_IDX=5, KEY_IDX=3	*
0x6F00	RW	SKEY_24	Shared key for BSS_IDX=6, KEY_IDX=0	*
0x6F20	RW	SKEY_25	Shared key for BSS_IDX=6, KEY_IDX=1	*
0x6F40	RW	SKEY_26	Shared key for BSS_IDX=6, KEY_IDX=2	*
0x6F60	RW	SKEY_27	Shared key for BSS_IDX=6, KEY_IDX=3	*
0x6F80	RW	SKEY_28	Shared key for BSS_IDX=7, KEY_IDX=0	*
0x6FA0	RW	SKEY_29	Shared key for BSS_IDX=7, KEY_IDX=1	*
0x6FC0	RW	SKEY_30	Shared key for BSS_IDX=7, KEY_IDX=2	*
0x6FE0	RW	SKEY_31	Shared key for BSS_IDX=7, KEY_IDX=3	*

Table 3-8 Shared Key Table (offset: 0x6C00)

3.3.5 Shared Key Mode (offset: 0x7000)

Offset	Type	Name	Description	Initial Value
0x7000	RW	SKEY_MODE_0_7	Shared mode for SKEY0 to SKEY7	*
0x7004	RW	SKEY_MODE_8_15	Shared mode for SKEY8 to SKEY15	*
0x7008	RW	SKEY_MODE_16_23	Shared mode for SKEY16 to SKEY23	*
0x700C	RW	SKEY_MODE_24_31	Shared mode for SKEY24 to SKEY31	*

Table 3-9 Shared Key Mode (offset: 0x7000)

3.3.6 Spare Memory Space Mode (offset: 0x7010 to 0x73EC)

3.3.7 Shared Key Mode Extension (for BSS_IDX=8 to 15) (offset: 0x73F0)

Offset	Type	Name	Description	Initial Value
0x73F0	RW	SKEY_MODE_32_39	Shared mode for SKEY32 to SKEY39	*
0x73F4	RW	SKEY_MODE_40_47	Shared mode for SKEY40 to SKEY47	*
0x73F8	RW	SKEY_MODE_48_55	Shared mode for SKEY48 to SKEY55	*
0x73FC	RW	SKEY_MODE_56_63	Shared mode for SKEY56 to SKEY63	*

Table 3-10 Shared Key Mode Extension (for BSS_IDX=8 to 15) (offset: 0x73F0)

3.3.8 Shared Key Table Extension (for BSS_IDX=8 to 15) (offset: 0x7400)

Offset	Type	Name	Description	Initial Value
0x7400	RW	SKEY_32	Shared key for BSS_IDX=8, KEY_IDX=0	*
0x7420	RW	SKEY_33	Shared key for BSS_IDX=8, KEY_IDX=1	*
0x7440	RW	SKEY_34	Shared key for BSS_IDX=8, KEY_IDX=2	*
0x7460	RW	SKEY_35	Shared key for BSS_IDX=8, KEY_IDX=3	*
0x7480	RW	SKEY_36	Shared key for BSS_IDX=9, KEY_IDX=0	*
0x74A0	RW	SKEY_37	Shared key for BSS_IDX=9, KEY_IDX=1	*
0x74C0	RW	SKEY_38	Shared key for BSS_IDX=9, KEY_IDX=2	*
0x74E0	RW	SKEY_39	Shared key for BSS_IDX=9, KEY_IDX=3	*
0x7500	RW	SKEY_40	Shared key for BSS_IDX=10, KEY_IDX=0	*
0x7520	RW	SKEY_41	Shared key for BSS_IDX=10, KEY_IDX=1	*
0x7540	RW	SKEY_42	Shared key for BSS_IDX=10, KEY_IDX=2	*
0x7560	RW	SKEY_43	Shared key for BSS_IDX=10, KEY_IDX=3	*
0x7580	RW	SKEY_44	Shared key for BSS_IDX=11, KEY_IDX=0	*
0x75A0	RW	SKEY_45	Shared key for BSS_IDX=11, KEY_IDX=1	*
0x75C0	RW	SKEY_46	Shared key for BSS_IDX=11, KEY_IDX=2	*
0x75E0	RW	SKEY_47	Shared key for BSS_IDX=11, KEY_IDX=3	*
0x7600	RW	SKEY_48	Shared key for BSS_IDX=12, KEY_IDX=0	*
0x7620	RW	SKEY_49	Shared key for BSS_IDX=12, KEY_IDX=1	*
0x7640	RW	SKEY_50	Shared key for BSS_IDX=12, KEY_IDX=2	*
0x7660	RW	SKEY_51	Shared key for BSS_IDX=12, KEY_IDX=3	*
0x7680	RW	SKEY_52	Shared key for BSS_IDX=13, KEY_IDX=0	*
0x76A0	RW	SKEY_53	Shared key for BSS_IDX=13, KEY_IDX=1	*
0x76C0	RW	SKEY_54	Shared key for BSS_IDX=13, KEY_IDX=2	*
0x76E0	RW	SKEY_55	Shared key for BSS_IDX=13, KEY_IDX=3	*
0x7700	RW	SKEY_56	Shared key for BSS_IDX=14, KEY_IDX=0	*
0x7720	RW	SKEY_57	Shared key for BSS_IDX=14, KEY_IDX=1	*
0x7740	RW	SKEY_58	Shared key for BSS_IDX=14, KEY_IDX=2	*
0x7760	RW	SKEY_59	Shared key for BSS_IDX=14, KEY_IDX=3	*

Offset	Type	Name	Description	Initial Value
0x7780	RW	SKEY_60	Shared key for BSS_IDX=15, KEY_IDX=0	*
0x77A0	RW	SKEY_61	Shared key for BSS_IDX=15, KEY_IDX=1	*
0x77C0	RW	SKEY_62	Shared key for BSS_IDX=15, KEY_IDX=2	*
0x77E0	RW	SKEY_63	Shared key for BSS_IDX=15, KEY_IDX=3	*

Table 3-11 Shared Key Table Extension (for BSS_IDX=8 to15) (offset: 0x7400)

3.3.9 WAPI PN Table (Extension of IV/EIV Table) (offset: 0x7800)

Offset	Type	Name	Description	Initial Value
0x7800	RW	WAPI_PN_MSB_0	Extension byte11 to byte8 of WAPI PN for WCID0	*
0x7804	RW	WAPI_PN_MSB_0	Extension byte15 to byte12 of WAPI PN for WCID0	*
0x7808	RW	WAPI_PN_MSB_1	Extension byte11 to byte8 of WAPI PN for WCID1	*
0x780C	RW	WAPI_PN_MSB_1	Extension byte15 to byte12 of WAPI PN for WCID1	*
....	RW		Extension byte11 to byte8 of WAPI PN for WCID2 to WCID254	*
....	RW		Extension byte15 to byte12 of WAPI PN for WCID2 to WCID254	*
0x7FF8	RW	WAPI_PN_MSB_255	Extension byte11 to byte8 of WAPI PN for WCID255	*
0x7FFC	RW	WAPI_PN_MSB_255	Extension byte15 to byte12 of WAPI PN for WCID255	*

Table 3-12 WAPI PN Table (Extension of IV/EIV Table) (offset: 0x73F0)

NOTE: Do not set WIV bit to 1 when WAPI mode is turned on.

4. Tx/Rx Descriptors and Wireless Information

4.1 Tx Descriptors and Frame Information

To transmit a frame, the driver needs to prepare the Tx frame information for hardware. The Tx frame information contains the transmission control, the header, and the payload. The transmission control information (TXWI) is used by the MAC and BBP and is applied to the associated Tx frame on transmission. The header and payload is the content of an 802.11 packet.

The Tx information may be divided into several segments. The Tx descriptor (TXD) specifies the location and length of the Tx frame information segments. Tx frame information may be linked by use of several TXD. These TXD are arranged in a TXD ring in serial.

The diagram below illustrates the relationship between TXD and Tx frame information.

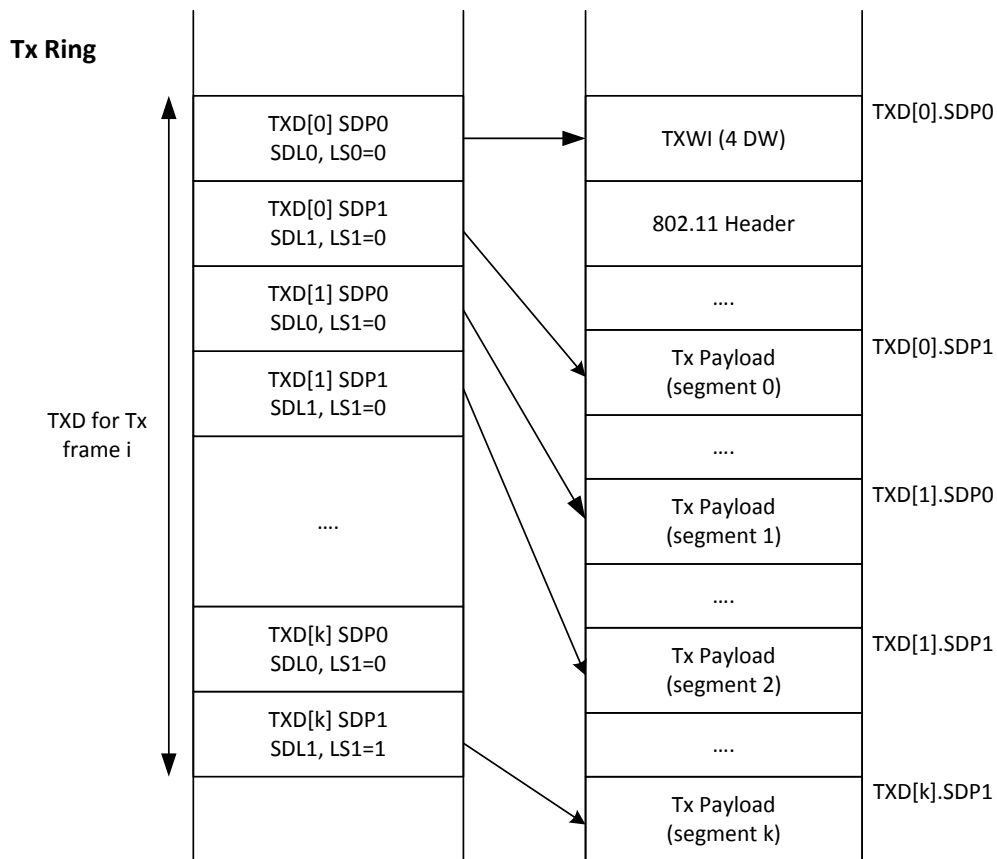


Figure 4-1 TXD and Tx Frame Information

4.1.1 TXD Format

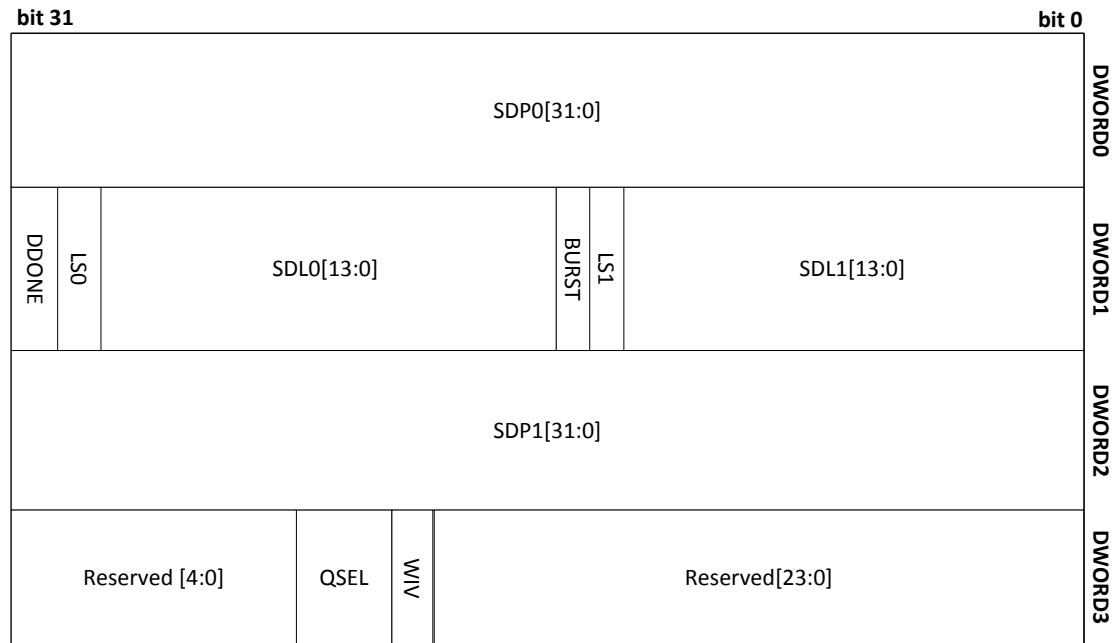


Figure 4-2 TXD Format

The following is a detailed description of each field in the TXD.

4.1.1.1 TXD Field Descriptions

Bits	Name	Description
DWORD0		
31:0	SDP0	Segment Data Pointer0
DWORD1		
31	DDONE	DMA Done: DMA has transferred the segments pointed to by this Tx descriptor.
30	LS0	Last Segment0: Data pointed to by SDP0 is the last segment.
29:16	SDL0	Segment Data Length0: Segment data length for the data pointed to by SDP0.
15	BURST	Forces the DMA to access the next Tx frame from the same queue.
14	LS1	Last Segment1: Data pointed to by SDP1 is the last segment.
13:0	SDL1	Segment Data Length0: Segment data length for the data pointed to by SDP1.
DWORD2		
31:0	SDP1	Segment Data Pointer1
DWORD3		
31:27	-	Reserved
26:25	QSEL	The ID of the on-chip queue that the Tx frame is moved into. 0: MGMT queue 1: HCCA queue 2: EDCA queue 3: Unused.
24	WIV	Wireless Information (WI) Valid 0: Driver prepared only the first 8-byte TXWI. 1: Driver prepared all 16-byte TXWI.
23:0	-	Reserved

Table 4-1 Tx Descriptor Format Field Descriptions

4.1.2 Tx Wireless Information

Tx wireless information (TXWI) is prepared by the host driver and used for passing information to the MAC. Its size is 4 DW and it is put at the head of each Tx frame.

bit 0																
DWORD0	DWORD1	DWORD2	DWORD3	DWORD4												
FRAG	ACK															
MMPS	NSEQ															
CFACK																
TS																
AMPDU																
MPDU density [2:0]		BAWinSize[5:0]			WCID[7:0]			MPDU total byte count[11:0]					Tx Packet ID[3:0]			
TXOP [1:0]																
Reserved [5:0]																
MCS[6:0]																
BW																
SGI																
STBC [1:0]																
Reserved [2:0]																
OFDM																
MIMO																
IV [31:0]																
EIV [31:0]																
Reserved[7:0]				STREAM_MODE[7:0]				Tx Power Adj[3:0]		RSV [1:0]		PIFS_REV_EN		Reserved[8:0]		

Table 4-2 TXWI Frame Format

The following is a detailed description of each field in TXWI.

4.1.2.1 TXWI Field Descriptions

Bits	Name	Description
DWORD0		
31	MIMO	Selects the PHY mode. Combine MIMO and OFDM bit values to select options. 00: CCK 01: OFDM
30	OFDM	10: Mixed mode 11: Green field For example, MIMO = 1, OFDM =0 → 10: Mixed mode
29:27	-	Reserved
26:25	STBC	Space-Time Block Code. For details see section 4.3.1 Modulation and Coding Scheme.
24	SGI	Short Guard Interval. For details see section 4.3.1 Modulation and Coding Scheme.
23	BW	Bandwidth. For details see section 4.3.1 Modulation and Coding Scheme.
22:16	MCS	Modulation and Coding Scheme. For details see section 4.3.1 Modulation and Coding Scheme.
15:10	-	Reserved
9:8	TXOP	Sets the Tx back off mode. 0: HT TXOP rule 1: PIFS Tx 2: SIFS (only when previous frame exchange is successful) 3: Back off.
7:5	MPDU density	1/4 μ sec - 16 μ sec per-peer parameter used in outgoing A-MPDU. This field complies with the “minimum MDPU Starting Spacing” of the A-MPDU parameter field of IEEE 802.11n draft 1.08. 000: No restriction 001: 1/4 μ sec 010: 1/2 μ sec 011: 1 μ sec 100: 2 μ sec 101: 4 μ sec 110: 8 μ sec 111: 16 μ sec
4	AMPDU	This frame is eligible for A-MPDU. MAC Tx aggregates subsequent outgoing frames with the same RA, same TID, and A-MPDU=1, whenever TXOP allows. Even if there is only one DATA frame to be sent, as long as the AMPDU bit in TXWI is ON, MAC still packages it as an AMPDU with an implicit BAR. This adds only a 4-byte A-MPDU delimiter overhead into the outgoing frame and implies the response frame is a BA instead of ACK. NOTE: The driver should set AMPDU=1 only after a BA session is successfully negotiated, because Block ACK is the only way to acknowledge when A-MPDU is used.

Bits	Name	Description
3	TS	Time Stamp Requests the MAC to insert an 8-byte timestamp after the 802.11 WLAN header in Beacon or ProbeResponse frames. 0: No timestamp 1: Inserts a timestamp
2	CFACK	Combines ACK and DATA frames. 0: No piggyback ACK is allowed for the RA of this frame. 1: If an ACK is required to the same peer as this outgoing DATA frame, then MAC Tx sends a single DATA+CFACK frame instead of separate ACK and DATA frames.
1	MMPS	MIMO Power Save Indicates whether the remote peer is in dynamic MIMO-PS (power save) mode. 0: Not in MIMO-PS mode 1: In MIMO-PS mode.
0	FRAG	Informs the TKIP engine and driver that this frame is a fragment. If set, the TKIP engine appends only IV/EIV and ICV to the final fragment, and the driver appends the TKIP MIC to the final fragment. For non-fragments, the TKIP engine is responsible for appending IV/EIV/ICV and TKIP MIC. 0: Not a fragment. 1: Is a fragment

DWORD1

31:28	Tx Packet ID	An ID specified by the driver for each Tx packet and latched onto the Tx result register stack. Driver uses this field to identify the successful transmission of a packet.
27:16	MPDU Total Byte Count	Total length of this frame.
15:8	WCID	Wireless Client Index. Lookup result of ADDR1 in the peer table (255=not found). This index is also used to find all the attributes of the wireless peer (e.g. Tx rate, Tx power, pairwise KEY, IV, EIV). This index has consistent meaning in both the driver and hardware.
7:2	BAWinSize	BA Window Size. Tells MAC the maximum number of frames (that will be BAed) allowed by the RA (RA's BA re-ordering buffer size)
1	NSEQ	1: Use the special HW SEQ number register in the MAC block.
0	ACK	This bit informs MAC whether to wait for ACK or not after transmission of the frame. Even though the QOD DATA frame has an ACK policy in its QOS CONTROL field, MAC Tx depends solely on this ACK bit to decide whether to wait for ACK or not. 0: Wait for ACK 1: Do not wait for ACK

DWORD2

31:0 IV Used by encryption engine.

DWORD3

31:0 EIV Used by encryption engine.

DWORD4

31:23 - Reserved

Bits	Name	Description
22	PIFS_REV_EN	After TxOP ACK, enable PIFS Time reversed direction Tx. 0: Disable 1: Enable
21:20	-	Reserved
19:16	Tx_Pwr_Adj	Transmit Power Adjustment Sets Tx power to a value from -16 dB to +7 dB. When negative, each unit represents 2 dB; when positive, each unit represents 1 dB.
15:8	TX_STREAM MODE	Transmit Stream Mode Control
7:0	-	Reserved

Table 4-3 TXWI Field Descriptions

4.2 Rx Descriptors and Wireless Information

The Rx descriptor (RXD) specifies the location to place the payload of the received frame (the Rx payload) and the associated receiving information (RXWI). One RXD serves for one receiving frame. Only SDP0 and SDL0 are useful in the RXD. The RXD is arranged in the RXD ring in serial. The hardware links the RXWI and Rx payload in serial and places it in the location specified in SDP0. See the diagram below.

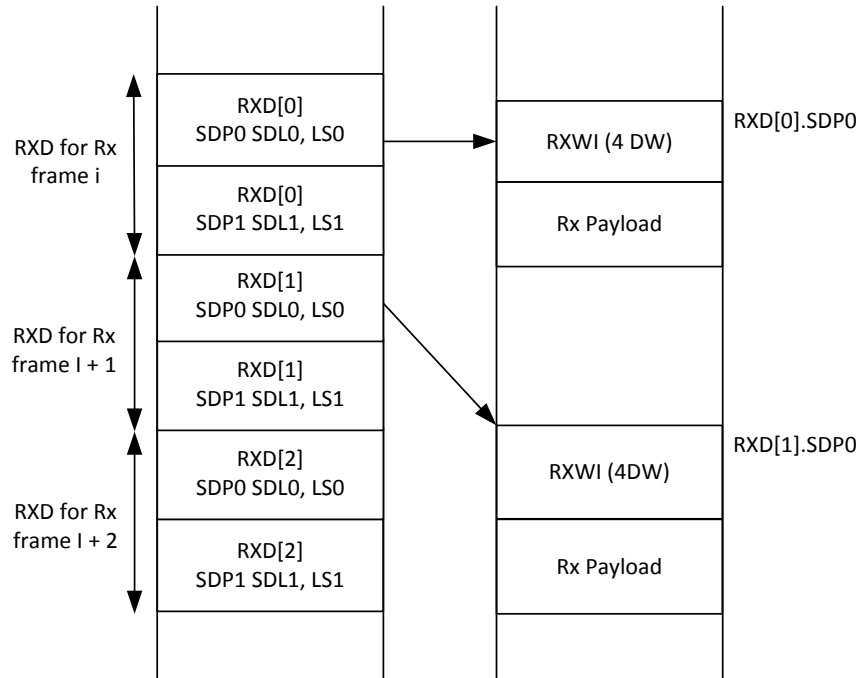


Figure 4-3 Rx Descriptor Ring

4.2.1 RXD Format

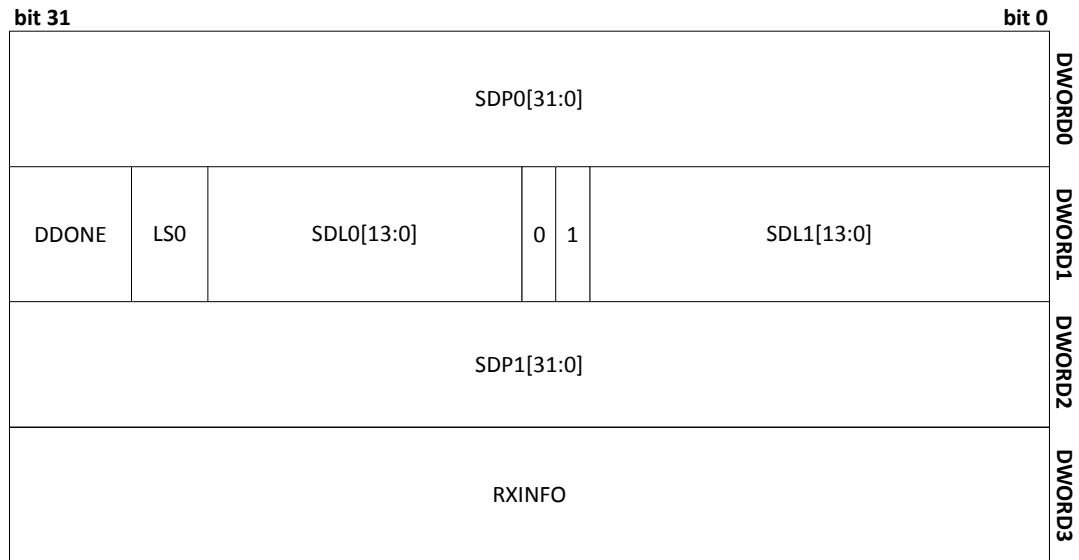


Figure 4-4 Rx Descriptor Format

The following is a detailed description of each field in the RXD.

4.2.1.1 RXD Field Descriptions

Bit	Name	Description
DWORD0		
31:0	SDP0	Segment data pointer 0
DWORD1		
31	DDONE	(DMA Done) DMA has moved the Rx frame to the specified location. This bit is set by hardware and cleared by driver.
30	LS0	Last segment pointed to by SDP0.
29:16	SDL0	Segment data length for data pointed to by SDP0.
15	0	(Padding)
14	1	(Padding)
13:0	SDL1	Segment data length for data pointed to by SDP1
DWORD2		
31:0	SDP1	Segment data pointer 1
DWORD3		
31:0	RXINFO	See description of RXINFO format in the next section.

NOTE: These fields are driver-specified.

4.2.2 RXINFO Format

RXINFO is prepared by the MAC and used for passing information to the host driver. Its size is 1 DW and it is put at the head of each Rx frame.

bit 0	BA
1	DATA
2	NULL
3	FRAG
4	UC2ME
5	MC
6	BC
7	MYBSS
8	CRCERR
9	ICVERR
10	MICERR
11	AMSDU
12	HTC
13	RSSI
14	L2PAD
15	AMPDU
16	DEC
17	BSSIDX_3
18	WAPIKID
19	PN_LEN[2:0]
21	
22	10'b0
bit 31	

Figure 4-5 RXINFO Format

The following is a detailed description of each field in RXINFO.

4.2.2.1 RXINFO Field Descriptions

Bit	Name	Description
31:22	-	Reserved
21:19	PN_LEN	IV/EIV/PN padding length (unit: DW)
18	WAPI_KID	WAPI Key ID
17	BSSIDX3	BSS index bit3, use together with BSS index bit[2:0] in RXWI
16	DEC	Indicates this frame is a decrypted frame
15	AMPDU	Indicates this frame has been de-aggregated from an AMPDU.
14	L2PAD	2 bytes are set to zero to act as padding after the MAC header (+ HTC)
13	RSSI	Indicates the validity of RSSI, SNR, and PHY rate. 0: All are not valid 1: All are valid
12	HTC	4 bytes are set to act as padding after the MAC header. 0: No padding 1: Set padding
11	AMSDU	This frame has been de-aggregated from an AMSDU.
10	MICERR	TKIP MIC error detected.
9	ICVERR	ICV/AES MIC error detected.
8	CRCERR	CRC error detected.
7	MYBSS	This frame is a my BSSID frame
6	BC	This frame is a broadcast frame.
5	MC	This frame is a multicast frame.
4	UC2ME	This frame is a unicast to me frame.
3	FRAG	This frame is a fragmented data frame.
2	NULL	This frame is a null data frame.
1	DATA	This frame is a data frame.
0	BA	BA session is under BA agreement (needs packet reordering)

NOTE:
0: False
1: True

4.2.3 RXWI Format

RXWI is prepared by the MAC and used for passing information to the host driver. Its size is 6 DW and it is put at the head of each Rx frame.

bit 31											bit 0										
TID [3:0]			MPDU total byte count[11:0]							UDF [2:0]		BSS idx [2:0]		Key idx [1:0]		WCID[7:0]					DWORD0
PHY mode [1:0]	RSV [2:0]		STBC [1:0]		SGI	BW	MCS[6:0]			SN[11:0]						FN[3:0]			DWORD1		
RSV[7:0]					RSSI_2[7:0]				RSSI_1[7:0]				RSSI_0[7:0]					DWORD2			
FREQ_OFFSET[7:0]					SNR_2[7:0]				SNR_1[7:0]				SNR_0[7:0]					DWORD3			
Reserved																DWORD4					
Reserved																DWORD5					

Figure 4-6 RXWI Frame Format

4.2.3.1 RXWI Field Descriptions

Bit	Name	Description
DWORD0		
31:28	TID	Traffic ID extracted from the 802.11 QoS control field.
27:16	MPDU total byte count	The entire MPDU length.
15:13	UDF	User defined field.
12:10	BSSID idx (index)	0 to 7 for BSSID0:7. Extracted from the 802.11 header (the last three bits of the BSSID field).
9:8	KEY idx (index)	0 to 3 extracted from IV field. For driver reference only, no particular usage so far.
7:0	WCID	Index of ADDR2 in the pairwise key table. This value uniquely identifies the TA. WCID=255 means not found.
DWORD1		
31:30	PHY mode	Rx data rate, obtained from the PLCP header. For details, see Brief PHY Rate Format and Definition
29:27	RSV	Reserved
26:25	STBC	Space–Time Block Code, obtained from the PLCP header. For details see Brief PHY Rate Format and Definition.
24	SGI	Short Guard Interval, obtained from the PLCP header. For details, see Brief PHY Rate Format and Definition.
23	BW	Bandwidth, obtained from the PLCP header. For details, see Brief PHY Rate Format and Definition.
22:16	MCS	Modulation and Coding Scheme, obtained from the PLCP header. For details, see Brief PHY Rate Format and Definition.
15:4	SN	The sequence number of the received MPDU. Used for BA re-ordering when AMSDU are auto-segregated by hardware and the 802.11 header is removed.
3:0	FN	The fragment number of the received MPDU. Extracted from the 802.11 header.
DWORD2		
31:24	RSV	Reserved
16:23	RSSI_2	The RSSI of the Rx frame from antenna 2, reported by BBP.
8:15	RSSI_1	The RSSI of the Rx frame from antenna 1, reported by BBP. Because RSSI_1 provides the same information as RX1_RSSI, it may be reprogrammed.
0:7	RSSI_0	The RSSI of the Rx frame from antenna 0, reported by BBP. Because RSSI_0 provides the same information as RX0_RSSI, it may be reprogrammed.
DWORD3		
31:24	FREQ_OFFSET	The frequency offset of the received frame, reported by BBP.
16:23	SNR_2	The SNR of the Rx frame from antenna 2, reported by BBP.
8:15	SNR_1	The SNR of the Rx frame from antenna 1, reported by BBP.
0:7	SNR_0	The SNR of the Rx frame from antenna 0, reported by BBP.

Table 4-4 RXWI Field Descriptions

4.3 Brief PHY Rate Format and Definition

A 16-bit brief PHY rate is used in MAC hardware. It is the same PHY rate field as that referred to in TXWI and RXWI sections.

Bit	Name	Description
15:14	PHY MODE	Preamble mode 0: Legacy CCK 1: Legacy OFDM 2: HT mixed mode 3: HT green field
13:10	-	Reserved
9	STBC	STBC only supported in HT mode 0: No STBC 1: STBC (Only supports STBC in HT mode MCS=0 to 7)
8	SGI	Short Guard Interval, only supported in HT mode. 0: 800 ns 1: 400 ns
7	BW	Bandwidth Supported in both legacy and HT modes. 40 Mhz in legacy mode means duplicate legacy . 0: 20 Mhz 1: 40 Mhz
6:0	MCS	Modulation and Coding Scheme (see below)

Table 4-5 Brief PHY Rate Format And Definition

4.3.1 Modulation and Coding Scheme

Modulation and Coding Scheme (MCS)	Description
MODE = Legacy CCK	
MCS = 0	Long Preamble CCK 1 Mbps
MCS = 1	Long Preamble CCK 2 Mbps
MCS = 2	Long Preamble CCK 5.5 Mbps
MCS = 3	Long Preamble CCK 11 Mbps
MCS = 8	Short Preamble CCK 1 Mbps (illegal rate)
MCS = 9	Short Preamble CCK 2 Mbps
MCS = 10	Short Preamble 5.5 Mbps
MCS = 11	Short Preamble 11 Mbps
Other MCS code in legacy CCK mode are reserved. When BW = 1, duplicate legacy OFDM is sent. SGI is reserved in legacy OFDM mode.	
MODE = Legacy OFDM	
MCS = 0	6 Mbps
MCS = 1	9 Mbps
MCS = 2	12 Mbps
MCS = 3	18 Mbps
MCS = 4	24 Mbps
MCS = 5	36 Mbps
MCS = 6	48 Mbps
MCS = 7	54 Mbps
Other MCS code in legacy CCK mode are reserved. When BW = 1, duplicate legacy OFDM is sent. SGI is reserved in legacy OFDM mode.	
MODE = HT mixed mode / HT greenfield	
MCS = 0 (1S)	(BW=0, SGI=0) 6.5 Mbps
MCS = 1	(BW=0, SGI=0) 13 Mbps
MCS = 2	(BW=0, SGI=0) 19.5 Mbps
MCS = 3	(BW=0, SGI=0) 26 Mbps
MCS = 4	(BW=0, SGI=0) 39 Mbps
MCS = 5	(BW=0, SGI=0) 52 Mbps
MCS = 6	(BW=0, SGI=0) 58.5 Mbps
MCS = 7	(BW=0, SGI=0) 65 Mbps
MCS = 8 (2S)	(BW=0, SGI=0) 13 Mbps
MCS = 9	(BW=0, SGI=0) 26 Mbps
MCS = 10	(BW=0, SGI=0) 39 Mbps
MCS = 11	(BW=0, SGI=0) 52 Mbps
MCS = 12	(BW=0, SGI=0) 78 Mbps

Modulation and Coding Scheme (MCS)	Description
MCS = 13	(BW=0, SGI=0) 104 Mbps
MCS = 14	(BW=0, SGI=0) 117 Mbps
MCS = 15	(BW=0, SGI=0) 130 Mbps
MCS = 32	(BW=1, SGI=0) HT duplicate 6 Mbps
When BW=1, $PHY_RATE = PHY_RATE * 2$. When SGI=1, $PHY_RATE = PHY_RATE * 10/9$. The effects of BW and SGI are accumulative. When MCS=0 to 7 (1S), SGI and BW options are supported. When MCS=8 to 15 (2S), SGI and BW options are supported. When MCS=32, only the SGI option is supported and BW is not supported. (BW =1) Other MCS codes in HT mode are reserved.	

Table 4-6 Modulation and Coding Scheme

5. SD Host Controller

5.1 Features

SD Host Controller contains:

- 32-bit access for control registers
- 8-bit/16-bit/32-bit access for FIFO in PIO mode
- Built-in 128-byte FIFO buffers for transmit and receive
- Built-in CRC circuit
- Supports Basic DMA mode, Basic Descriptor mode, and Enhanced Descriptor mode
- Interrupt capabilities
- SPI mode not supported for SD Memory Card
- Suspend/resume not supported for SD Memory Card
- Supports SD2.0 High Speed, data rate up to 196 Mbps with a 48 MHz SD clock
- Card detection capabilities

5.2 SD Host Block Diagram

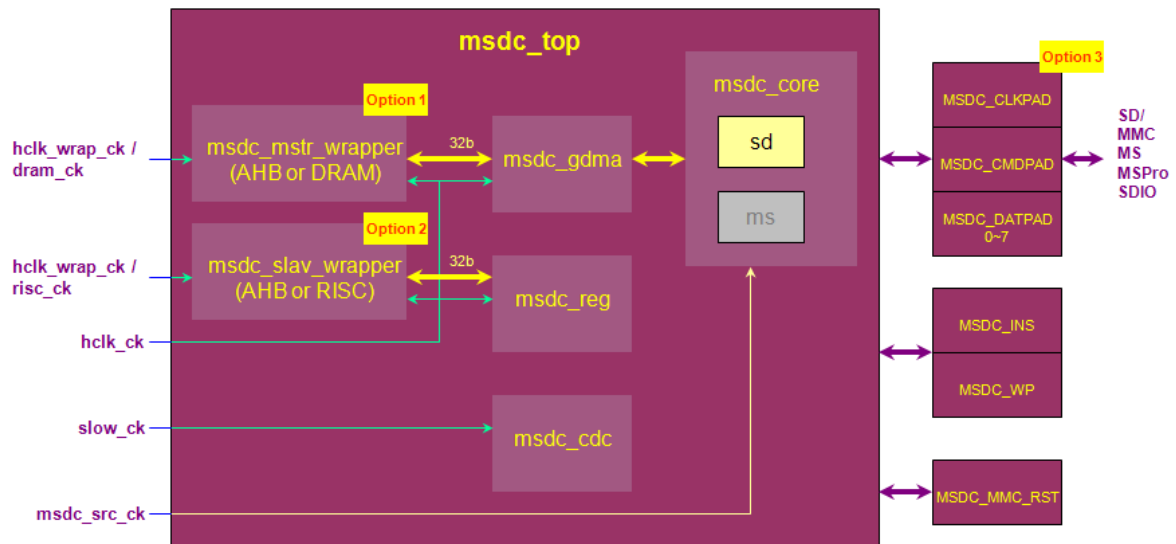


Figure 5-1 SD Host Block Diagram

5.2.1 Basic DMA Mode

The operation in basic DMA mode is the same as conventional DMA operation. In this mode, the DMA controller moves a bulk of data from the source to MSDC.

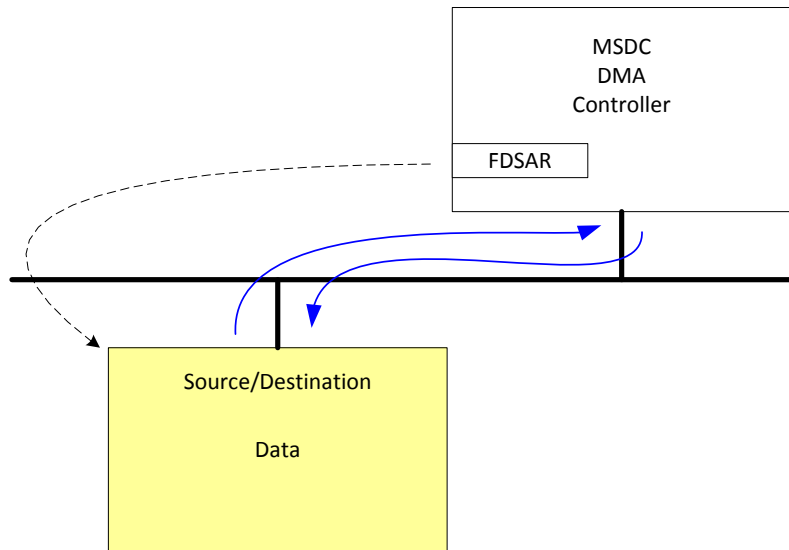


Figure 5-2 Basic DMA

5.2.2 Linked-List Based DMA Mode

The linked-list based DMA utilizes the descriptor structure to describe the data. Two types of DMA descriptors are defined for the purpose: General Packet Descriptors (GPD) and Buffer Descriptors (BD). For fragmented data, one or more BDs are included to describe the discrete data. One GPD descriptor link can generate one SD command transaction.

For the flexibility of the descriptor structure, the linked-list DMA mode provides the hardware merging function to copy fragmented source data to a continuous destination data buffer.

For multiple source data buffers, as shown in the following figure, each data buffer at the source is pointed to by a DMA BD. All the DMA BDs associated with the multiple source data buffers are linked together as a list and the list is pointed to by a DMA GPD. The DMA control copies the fragmented source data into a single destination data buffer. It provides the hardware-implemented data merging function to reduce the computation power consumption of the embedded processor on the data copying.

The following figure shows the example of the linked-list based DMA mode on the DMA channel. Multiple destination data buffers are allowed in this mode. Each time the DMA controller finishes the DMA transfer operation for the data which belongs to one DMA GPD/BD, the controller will use the INT bit in GPD/BD to generate an interrupt to inform the firmware.

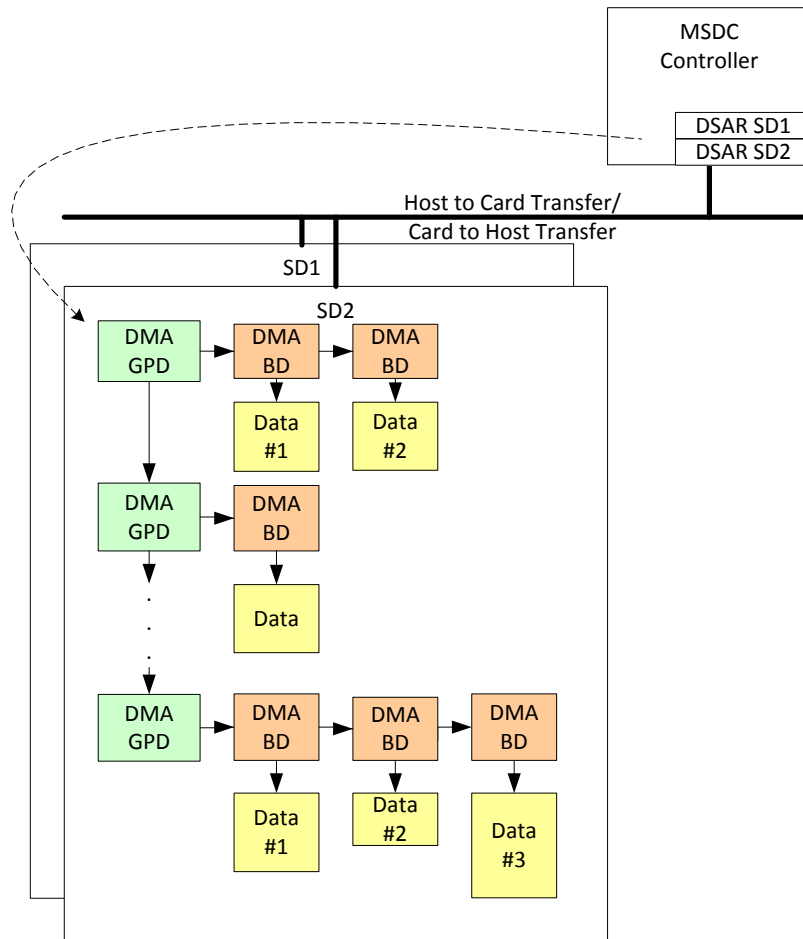


Figure 5-3 Descriptor DMA

5.2.3 DMA Generic Packet Descriptor (GPD) Format

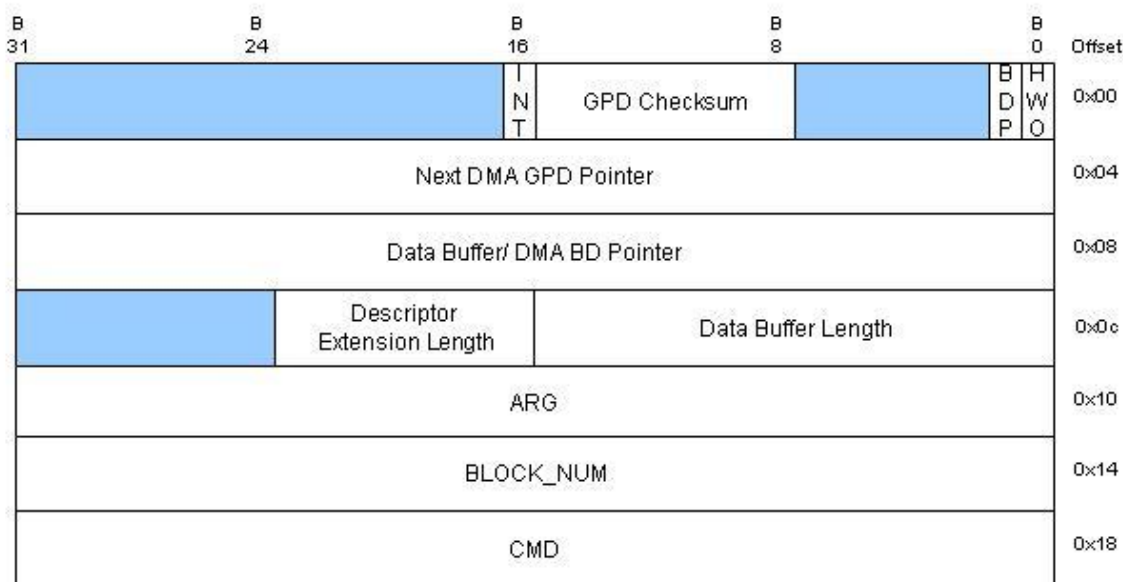


Figure 5-4 GPD Format

The structure of a DMA Generic Packet Descriptor (GPD) is defined in the following table.
Please note that the start address of a descriptor should be 4 B alignment.

Offset	Field	Description
0x00	HWO	Bit 0: Hardware Own This bit is used to specify the current ownership of this DMA GPD and its associated data buffer(s) and DMA BDs, if present. 0: The firmware has ownership of this DMA GPD and its associated data buffer(s) / DMA BDs and it can change the contents as desired. After the firmware has finished preparation of the linked list of the DMA GPDs for transmission, firmware sets this bit in each DMA GPD to 1 to specify the ownership of the DMA GPD changed to the DMA hardware and then starts or resume the Tx burst queues. 1: Indicates this descriptor and its associated data buffer(s) / DMA BDs are being processed or are waiting for service by the DMA hardware. The firmware does not try to access them at this time. After the DMA HW finishes or aborts processing of this descriptor, it changes the value of this bit to 0 to indicate the release of ownership to the firmware.

	BDP	Bit 1: Buffer Descriptor Present This bit is set according to the following conditions: 0: A data buffer is directly pointed to by the DATA_BUFF_PTR field in this descriptor. In this case, only one data buffer is associated with this DMA GPD. 1: The DATA_BUFF_PTR field does not directly point to a data buffer, but a linked list of DMA Buffer Descriptors instead. The associated data buffer is pointed to by the DATA_BUFF_PTR field in the DMA Buffer Descriptor(s). Therefore, more than one data buffer can be associated with this DMA GPD.
0x01	GPD Checksum	GPD Checksum This field is used to validate the contents of this DMA GPD by the DMA HW. Before accessing this descriptor, the DMA HW calculates an 8-bit checksum over the first 16 bytes of the DMA GPD and expects the final checksum value to be 0xFF. If the checksum verification fails, the DMA HW issues an interrupt to inform the firmware of a DMA GPD checksum error.
0x02	INT	Bit 0: Interrupt Generation Mask Only for Enhanced mode. Other modes should keep this bit to 0. 0: No mask of the MSDC_INT.DMA_DONE interrupt. 1: Masks the MSDC_INT.DMA_DONE interrupt.
0x04 to 0x07	Next DMA GPD Pointer	Next DMA GPD Pointer For the descriptor-based DMA mode, this field is reserved. The DMA HW ignores this field. For the linked-list based DMA mode, this field shall be set to the address of the next DMA GPD. When the DMA HW reads a DMA GPD with the HWO bit set to 0, it ignores this field.
0x08 to 0x0B	Data Buffer / DMA BD Pointer	Data Buffer Pointer/ DMA BD pointer This field shall be set to the starting address of the associated data buffer if the BDP bit is set to 0. Otherwise, it is set to the address of a DMA Buffer Descriptor when the BDP bit is 1. When the DMA HW reads a DMA GPD with the HWO bit set to 0, it ignores this field.
0x0C to 0x0D	Data Buffer Length	Data Buffer Length This field shall be set to the total length of the data in the associated data buffer(s) pointed to by the Data Buffer. The field is ignored when BDP=1. (unit: bytes)
0x0E	Descriptor Extension length	Descriptor Extension Length For SD enhance mode, if the software driver wants to enqueue the GPD before previous command is complete, then this field should be set to 0xC for the new GPD. When the MSDC controller fetches GPD and finds this field is not zero, the setting of register SDC_ARG, SDC_BLOCK_NUM, and SDC_CMD will be replaced by the following 3 DW. (0x13 to 0x1B) If the software driver hopes to use the original control through register, it needs to wait for all the enqueued descriptor transfers to complete to program for the new command.
0x10 to 0x13	ARG	Enhance Mode SD Command Argument This field defines SDC_ARG.

0x14 to 0x17	BLOCK_NUMBER	Enhance Mode SD Block Number This field defines SDC_BLOCK_NUMBER.
0x18 to 0x1B	CMD	Enhance Mode SD Command This field defines SDC_CMD.

5.2.4 DMA Buffer Descriptor (BD) Format

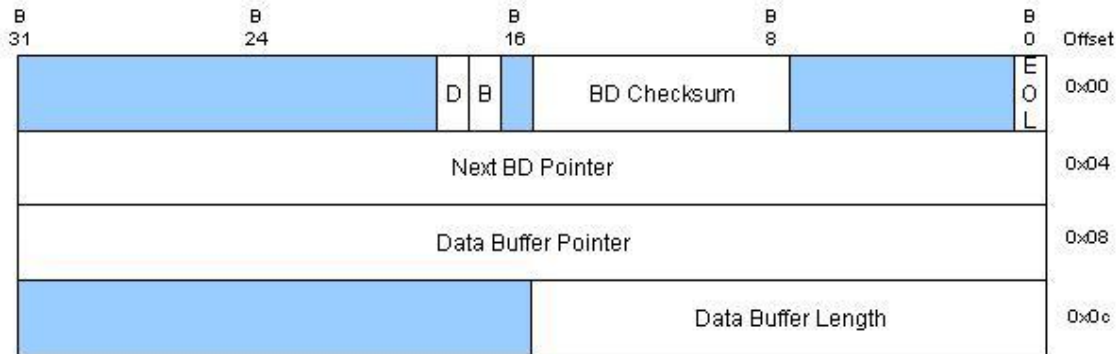


Figure 5-5 BD Format

The structure of a DMA Buffer Descriptor (BD) is defined in the following table.

Offset	Field	Description
0x00	EOL	Bit 0: End of List (EOL) 0: Indicates there is at least one DMA Buffer Descriptor following. 1: This descriptor is the last one in the linked list of DMA Buffer Descriptors.
0x01	BD Checksum	Buffer Descriptor Checksum This field is used to validate the contents of this DMA BD by the DMA HW. Before accessing this descriptor, the DMA HW calculates an 8-bit checksum over the first 16 bytes of this DMA BD and expects the final checksum value shall be 0xFF. If the checksum verification fails, the DMA HW issues an interrupt to inform the firmware of DMA BD checksum error. Then it stops the DMA transfer operation immediately.
0x02	B	Bit 1: Block Padding Set to 1 to let the controller pad zeroes up to the block size boundary. The total padding bytes are calculated by (block size * block number) – (the total accumulated bytes of all BDs). If the last byte of this BD is at the block boundary, then there will be no padding bytes. If controller needs to send the auto command, the auto command will be sent after the padding bytes. Please note that this bit can only be set in the last BD of MSDC write transfer. S/W should not set B=1 if block padding is not required.

Offset	Field	Description
	B	Bit 1: Block Padding Set to 1 to let the controller padding 0 till the block size boundary. The total padding bytes are calculated by (block size * block number) – (the total accumulated bytes of all BDs). If the last byte of this BD is at the block boundary, then there will be no padding bytes. If controller needs to send the auto command, the auto command will be sent after the padding bytes. Please note that this bit can only be set in the last BD of MSDC write transfer. S/W should not set B=1 if block padding is needless.
0x04 to 0x07	Next BD Pointer	Next Buffer Descriptor Pointer Set to the address of the next DMA BD if this DMA BD is not the last one in the linked list of the DMA Buffer Descriptors (EOL=0). This field is ignored by the DMA HW when the EOL bit is set to 1.
0x08 to 0x0B	Data Buffer Pointer	Data Buffer Pointer Set to the starting address of the data buffer.
0x0C to 0x0D	Data Buffer Length	Data Buffer Length The length of the data buffer that is pointed to by the Data Buffer Pointer field, (unit: bytes)

5.2.5 Register Description (base: 0x1013_0000)

These registers are used for the SD driver. For more information on these registers, please contact MediaTek.

6. List of Registers

1. CHIPID0_3: CHIP ID ASCII CHARACTER 0-3 (OFFSET: 0x0000)	19
2. CHIPID4_7: CHIP NAME ASCII CHARACTER 4-7 (OFFSET: 0x0004)	19
3. REVID: CHIP REVISION IDENTIFICATION (OFFSET: 0x000C)	19
4. SYSCFG0: SYSTEM CONFIGURATION REGISTER 0 (OFFSET: 0x0010)	19
5. SYSCFG1: SYSTEM CONFIGURATION REGISTER 0 (OFFSET: 0x0014)	20
6. TESTSTAT: FIRMWARE TEST STATUS REGISTER (OFFSET: 0x0018)	22
7. TESTSTAT2: FIRMWARE TEST STATUS REGISTER 2 (OFFSET: 0x001C)	22
8. RESERVED (OFFSET: 0x0020)	22
9. RESERVED (OFFSET: 0x0024)	23
10. RESERVED (OFFSET: 0x0028)	23
11. CLKCFG0: CLOCK CONFIGURATION REGISTER 0 (OFFSET: 0x002C)	23
12. CLKCFG1: CLOCK CONFIGURATION REGISTER 1 (OFFSET: 0x0030)	24
13. RSTCTRL: RESET CONTROL REGISTER (OFFSET: 0x0034)	25
14. RSTSTAT: RESET STATUS REGISTER (OFFSET: 0x0038)	26
15. CPU_SYS_CLKCFG: CPU AND SYS CLOCK CONTROL (OFFSET: 0x003C)	27
16. CLK_LUT_CFG: CPU AND SYS CLOCK AUTO CONTROL (OFFSET: 0x0040)	29
17. CUR_CLK_STS: CURRENT CLOCK STATUS (OFFSET: 0x0044)	30
18. BPLL_CFG0: BB PLL CONFIGURATION 0 (OFFSET: 0x0048)	31
19. BPLL_CFG1: BB PLL CONFIGURATION 0 (OFFSET: 0x004C)	31
20. CPLL_CFG0: CPU PLL CONFIGURATION 0 (OFFSET: 0x0054)	33
21. CPLL_CFG1: CPU PLL CONFIGURATION 1 (OFFSET: 0x0058)	36
22. USB_PHY_CFG: USB PHY CONTROL (OFFSET: 0x005C)	36
23. GPIOMODE: GPIO PURPOSE SELECT (OFFSET: 0x0060)	36
24. PCIPDMA_STAT: CONTROL AND STATUS OF PDMA IN PCIe DEVICE (OFFSET: 0x0064)	39
25. PMU0_CFG: (OFFSET: 0x0088)	39
26. PMU1_CFG: (OFFSET: 0x008C)	40
27. PPLL_CFG0: PCIe PLL CONFIGURATION 0 (OFFSET: 0x0098)	41
28. PPLL_CFG1: PCIe PLL CONFIGURATION 1 (OFFSET: 0x009C)	43
29. PPLL_DRV: PCIe DRIVER CONFIGURATION (OFFSET: 0x00A0)	44
30. TMRSTAT: TIMER STATUS REGISTER (OFFSET: 0x0000)	49
31. TMROLOAD: TIMER 0 LOAD VALUE (OFFSET: 0x0010)	50
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7. Abbreviations

Abbrev.	Description	Abbrev.	Description
AC	Access Category	CRC	Cyclic Redundancy Check
ACK	Acknowledge/ Acknowledgement	CSR	Control Status Register
ACL	Access Control List	CTS	Clear to Send
ACPR	Adjacent Channel Power Ratio	CW	Contention Window
AD/DA	Analog to Digital/Digital to Analog converter	CWmax	Maximum Contention Window
ADC	Analog-to-Digital Converter	CWmin	Minimum Contention Window
AES	Advanced Encryption Standard	DAC	Digital-To-Analog Converter
AFC	Automatic Frequency Calibration	DCF	Distributed Coordination Function
AGC	Auto Gain Control	DDONE	DMA Done
AIFS	Arbitration Inter-Frame Space	DDR	Double Data Rate
AIFSN	Arbitration Inter-Frame Spacing Number	DFT	Discrete Fourier Transform
ALC	Automatic Level Control	DIFS	DCF Inter-Frame Space
A-MPDU	Aggregate MAC Protocol Data Unit	DMA	Direct Memory Access
A-MSDU	Aggregation of MAC Service Data Units	DQ	DRAM Data
AP	Access Point	DQS	Data Strobe
ASIC	Application-Specific Integrated Circuit	DSCP	Differentiated Services Code Point
ASME	American Society of Mechanical Engineers	DSP	Digital Signal Processor
ASYNCR	Asynchronous	DW	DWORD
BA	Block Acknowledgement	EAP	Expert Antenna Processor
BAC	Block Acknowledgement Control	ED	Energy Detection
BAR	Base Address Register	EDCA	Enhanced Distributed Channel Access
BBP	Baseband Processor	EECS	EEPROM chip select
BGSEL	Band Gap Select	EEDI	EEPROM data input
BIST	Built-In Self-Test	EEDO	EEPROM data output
BSC	Basic Spacing between Centers	EEPROM	Electrically Erasable Programmable Read-Only Memory
BJT	Bipolar Junction Transistor	eFUSE	electrical Fuse
BSSID	Basic Service Set Identifier	EESK	EEPROM source clock
BW	Bandwidth	EIFS	Extended Inter-Frame Space
CAS	Column Address Strobe	EIV	Extend Initialization Vector
CCA	Clear Channel Assessment	EVM	Error Vector Magnitude
CCK	Complementary Code Keying	FDS	Frequency Domain Spreading
CCMP	Counter Mode with Cipher Block Chaining Message Authentication Code Protocol	FEM	Front-End Module
CCX	Cisco Compatible Extensions	FEQ	Frequency Equalization
CF-END	Control Frame End	FIFO	First In First Out
CF-ACK	Control Frame Acknowledgement	FSM	Finite-State Machine
CLK	Clock	GDM	GTP Director Module
CPU	Central Processing Unit	GEM	GPON Encapsulation Method
		GF	Green Field
		GND	Ground
		GP	General Purpose

Abbrev.	Description
GPO	General Purpose Output
GPON	Gigabit Passive Optical Network
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GTP	GPRS Tunneling Protocol
HCCA	HCF Controlled Channel Access
HCF	Hybrid Coordination Function
HT	High Throughput
HTC	High Throughput Control
I	In phase
ICV	Integrity Check Value
IFS	Inter-Frame Space
iNIC	Intelligent Network Interface Card
IV	Initialization Vector
I ² C	Inter-Integrated Circuit
I ² S	Integrated Inter-Chip Sound
I/O	Input/Output
IPI	Idle Power Indicator
IQ	In phase/Quadrature phase
JEDEC	Joint Electron Devices Engineering Council
JTAG	Joint Test Action Group
kbps	kilo (1000) bits per second
KB	Kilo (1024) Bytes
LCP	Linear Complementarity Problem
LDO	Low-Dropout Regulator
LDODIG	LDO for DIGital part output voltage
LED	Light-Emitting Diode
LTSSM	Link Training and Status State Machine
LNA	Low Noise Amplifier
LO	Local Oscillator
L-SIG	Legacy Signal Field
MAC	Medium Access Control
MCU	Microcontroller Unit
MCS	Modulation and Coding Scheme
MDC	Management Data Clock
MDIO	Management Data Input/Output
MEM	Memory
MFB	MCS Feedback
MFS	MFB Sequence
MIC	Message Integrity Code
MIMO	Multiple-Input Multiple-Output
MLD	Multicast Listener Discovery

Abbrev.	Description
MLNA	Monolithic Low Noise Amplifier
MM	Mixed Mode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPDU	MAC Protocol Data Units
MSB	Most Significant Bit
NAV	Network Allocation Vector
NAS	Network-Attached Server
NAT	Network Address Translation
NDP	Null Data Packet
NVM	Non-Volatile Memory
OCP	Open Core Protocol
ODT	On-die Termination
Oen	Output Enable
OFDM	Orthogonal Frequency-Division Multiplexing
OoS	Out-of-Service
OSC	Open Sound Control
PA	Power Amplifier
PAPE	Provider Authentication Policy Extension
PBC	Push Button Configuration
PBF	Packet Buffer
PCB	Printed Circuit Board
PCF	Point Coordination Function
PCM	Pulse-Code Modulation
PD	Preamble Detection
PFD	Phase-Frequency Detector
PHY	Physical Layer
PIFS	PCF Interframe Space
PLCP	Physical Layer Convergence Protocol
PLL	Phase-Locked Loop
PME	Physical Medium Entities
PMU	Power Management Unit
PN	Packet Number
PPLL	Programmable PLL
PROM	Programmable Read-Only Memory
PSDU	Physical layer Service Data Unit
PSI	Power supply Strength Indication
PSM	Power Save Mode
PTN	Packet Transport Network
QoS	Quality of Service
Q	Quadrature

Abbrev.	Description
R2P	Rbus to Pbus
RDG	Reverse Direction Grant
RAM	Random Access Memory
RC	Root Complex
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RH	Relative Humidity
RoHS	Restriction on Hazardous Substances
ROM	Read-Only Memory
ROS	Rx Offset
RSSI	Received Signal Strength Indication (Indicator)
RTS	Request to Send
RvMII	Reverse Media Independent Interface
Rx	Receive
RXD	Received Data
RXINFO	Receive Information
RXWI	Receive Wireless Information
S	Stream
SDHC	Secure Digital High Capacity
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SEC	Security
SGI	Short Guard Interval
SIFS	Short Inter-Frame Space
SoC	System-on-a-Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSCG	Spread Spectrum Clock Generator
STBC	Space-Time Block Code
SW	Switch Regulator

Abbrev.	Description
TA	Transmitter Address
TBTT	Target Beacon Transmission Time
TDLS	Tunnel Direct Link Setup
TKIP	Temporal Key Integrity Protocol
TOS	Tx Offset
TRSW	Tx/Rx Switch
TSF	Timing Synchronization Function
TSSI	Transmit Signal Strength Indication
Tx	Transmit
TxBF	Transmit Beamforming
TXD	Transmitted Data
TXDAC	Transmit Digital-Analog Converter
TXINFO	Transmit Information
TXOP	Opportunity to Transmit
TXWI	Tx Wireless Information
UART	Universal Asynchronous Rx/ Tx
USB	Universal Serial Bus
UTIF	Universal Test Interface
VGA	Variable Gain Amplifier
VCO	Voltage Controlled Oscillator
VIH	High Level Input Voltage
VIL	Low Level Input Voltage
VoIP	Voice over IP
VPID	Virtual Path Identifier
WCID	Wireless Client Identification
WEP	Wired Equivalent
WI	Wireless Information
WIV	Wireless Information Valid
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPDMA	Wireless Polarization Division Multiple Access
WS	Word Select

8. Revision History

Rev	Date	From	Description
1.0	2012/01/18	Lancelot Lin	Initial Release (Split programming guide from original spec)

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